SAMSUNG ELECTRONICS

1140-9041
April 1999

SAMSUNG Semiconductor

DRAM Module

EDO & Fast Page Mode

1999 Data Book

PRINTED IN KOREA

TABLE OF CONTENTS

I. General Information

II. Single In-Line Memory Module (SIMM)

II-I. 4 Byte SIMM (5V)

III. Small Out-Line Dual In-Line Memory Module (SODIMM)

III-I. 8 Byte SODIMM (3.3V)

IV. Dual In-Line Memory Module (DIMM)

IV-I. 8 Byte Buffered DIMM (3.3V)

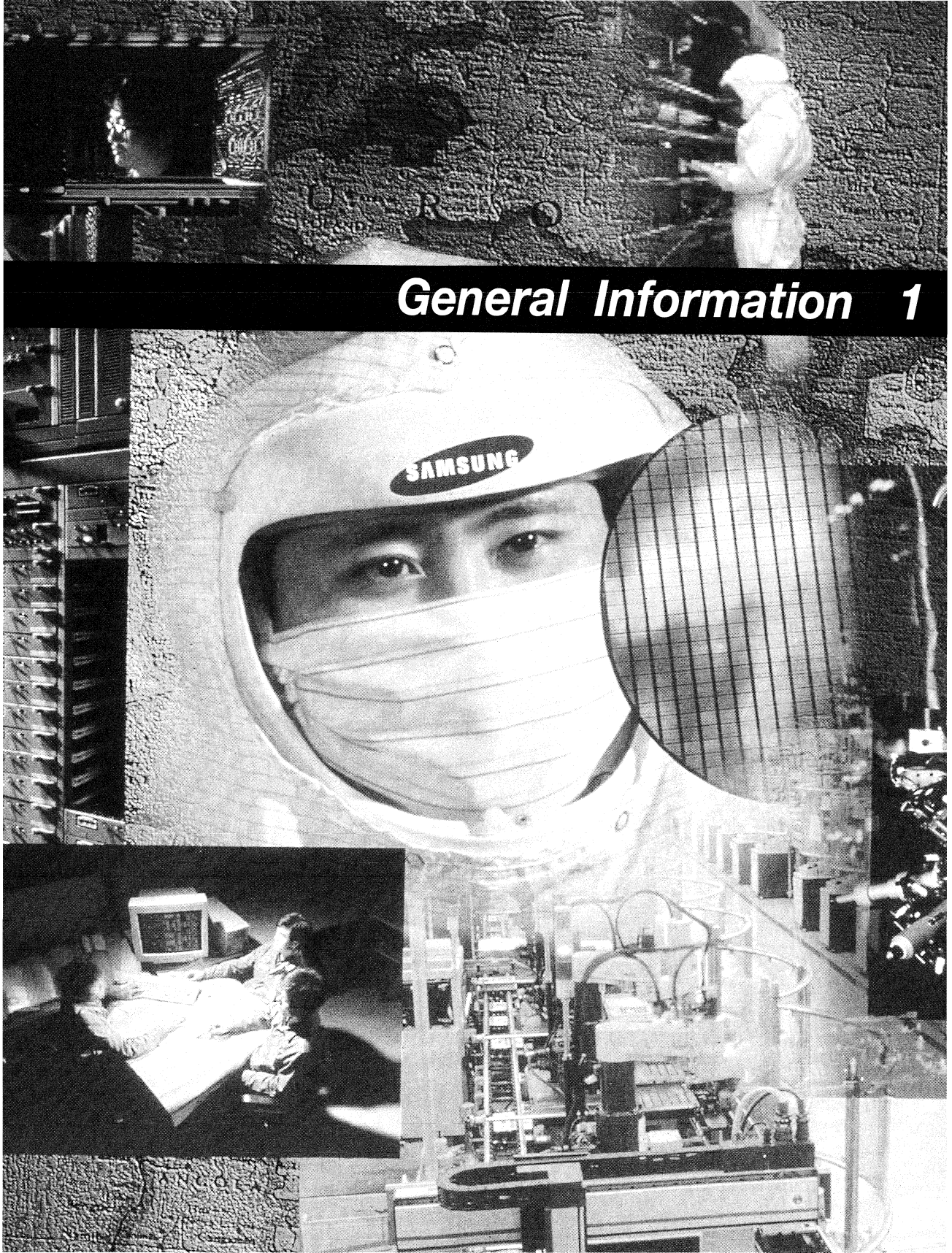
IV-II. 8 Byte Buffered DIMM (5V)

IV-III. 8 Byte Unbuffered DIMM (3.3V)

V. Timing Diagram

VI. Serial Presence Detect(SPD) Specification

VII. Sales Offices and Manufacturer Representatives



General Information 1

DRAM Module

1. Introduction

I. Single In-Line Memory Module (SIMM)

I-I. Fast Page(FP) Mode(5V)

64M based	4Mx32	KMM5324000BSW/BSWG-5	KMM5324000BSW/BSWG-6
	4Mx36	KMM5364003BSW/BSWG-5	KMM5364003BSW/BSWG-6
	8Mx32	KMM5328000BSW/BSWG-5	KMM5328000BSW/BSWG-6
	8Mx36	KMM5368003BSW/BSWG-5	KMM5368003BSW/BSWG-6
	16Mx32	KMM53216000BK/BKG-5	KMM53216000BK/BKG-6
		KMM53216000BV/BVG-5	KMM53216000BV/BVG-6
	16Mx36	KMM53616000BK/BKG-5	KMM53616000BK/BKG-6
	32Mx32	KMM53232000BK/BKG-5	KMM53232000BK/BKG-6
		KMM53232000BV/BVG-5	KMM53232000BV/BVG-6
	32Mx36	KMM53632000BK/BKG-5	KMM53632000BK/BKG-6

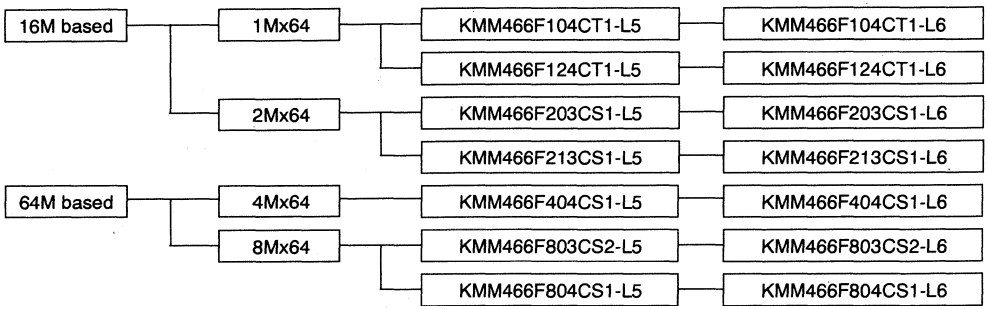
I-II. Extended Data-Out (EDO) Mode(5V)

64M based	4Mx32	KMM5324004BSW/BSWG-5	KMM5324004BSW/BSWG-6
	4Mx36	KMM5364005BSW/BSWG-5	KMM5364005BSW/BSWG-6
	8Mx32	KMM5328004BSW/BSWG-5	KMM5328004BSW/BSWG-6
	8Mx36	KMM5368005BSW/BSWG-5	KMM5368005BSW/BSWG-6
	16Mx32	KMM53216004BK/BKG-5	KMM53216004BK/BKG-6
		KMM53216004BV/BVG-5	KMM53216004BV/BVG-6
	16Mx36	KMM53616004BK/BKG-5	KMM53616004BK/BKG-6
	32Mx32	KMM53232004BK/BKG-5	KMM53232004BK/BKG-6
		KMM53232004BV/BVG-5	KMM53232004BV/BVG-6
	32Mx36	KMM53632004BK/BKG-5	KMM53632004BK/BKG-6

II. Small Out -Line In Line Memory Module(SODIMM)

II-I. Extended Data-Out (EDO) Mode

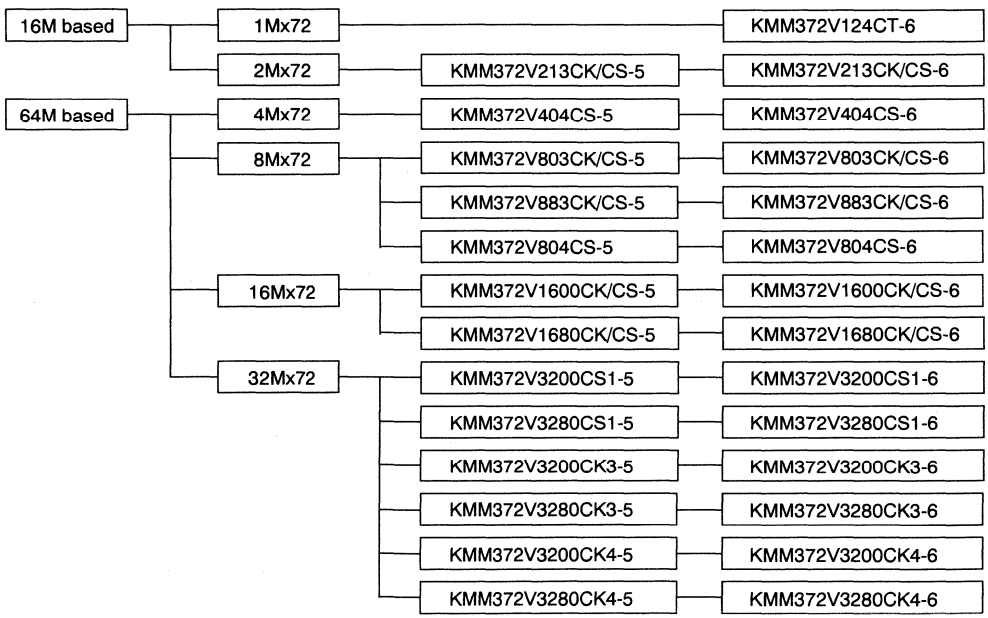
8 Byte SODIMM(3.3V)



III. Dual In-Line Memory Module (DIMM)

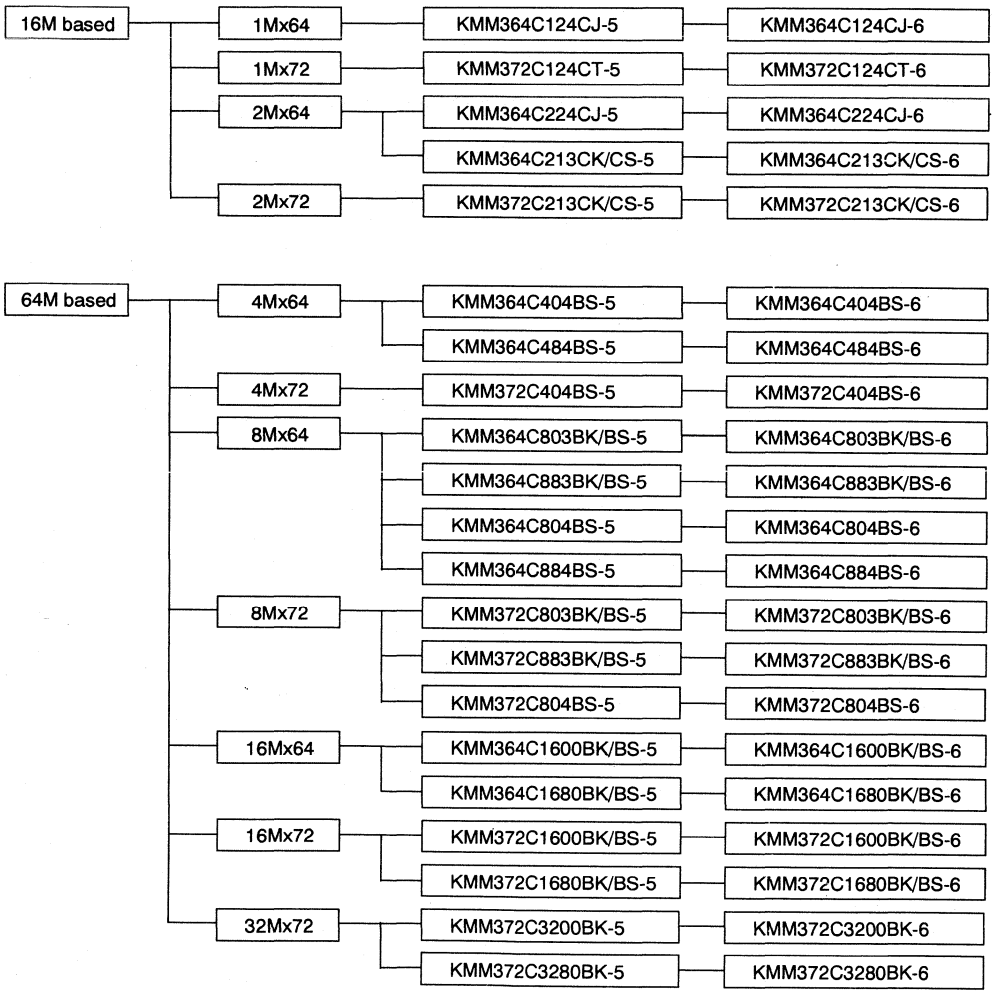
III-I. Fast Page (FP) Mode

Buffered DIMM(3.3V)



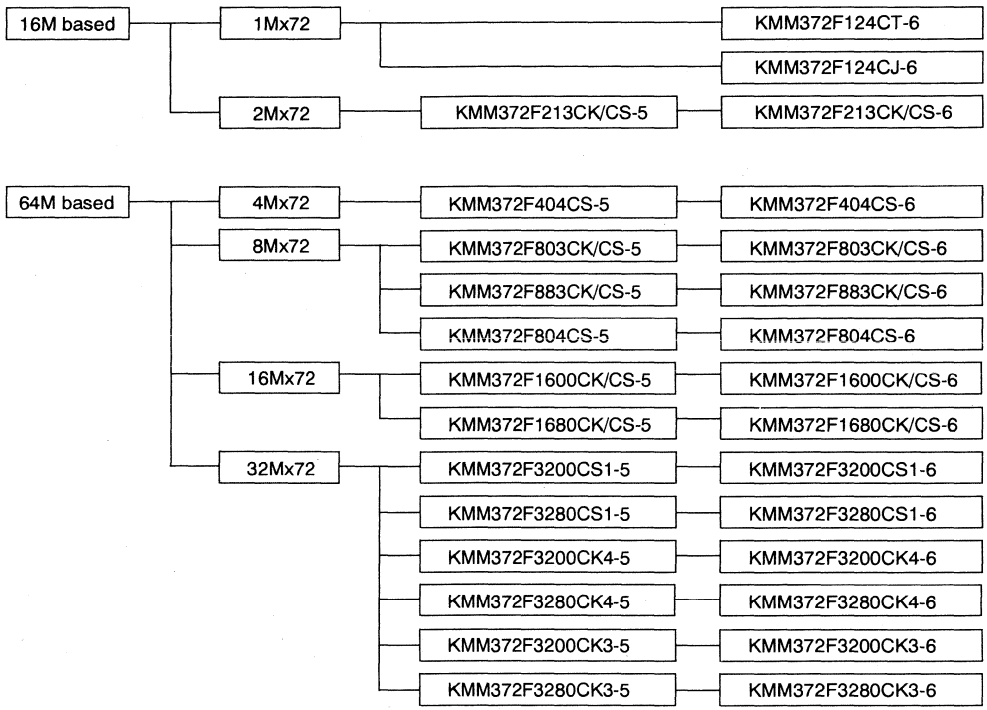
III-I. Fast Page (FP) Mode -- Continued

Buffered DIMM(5V)



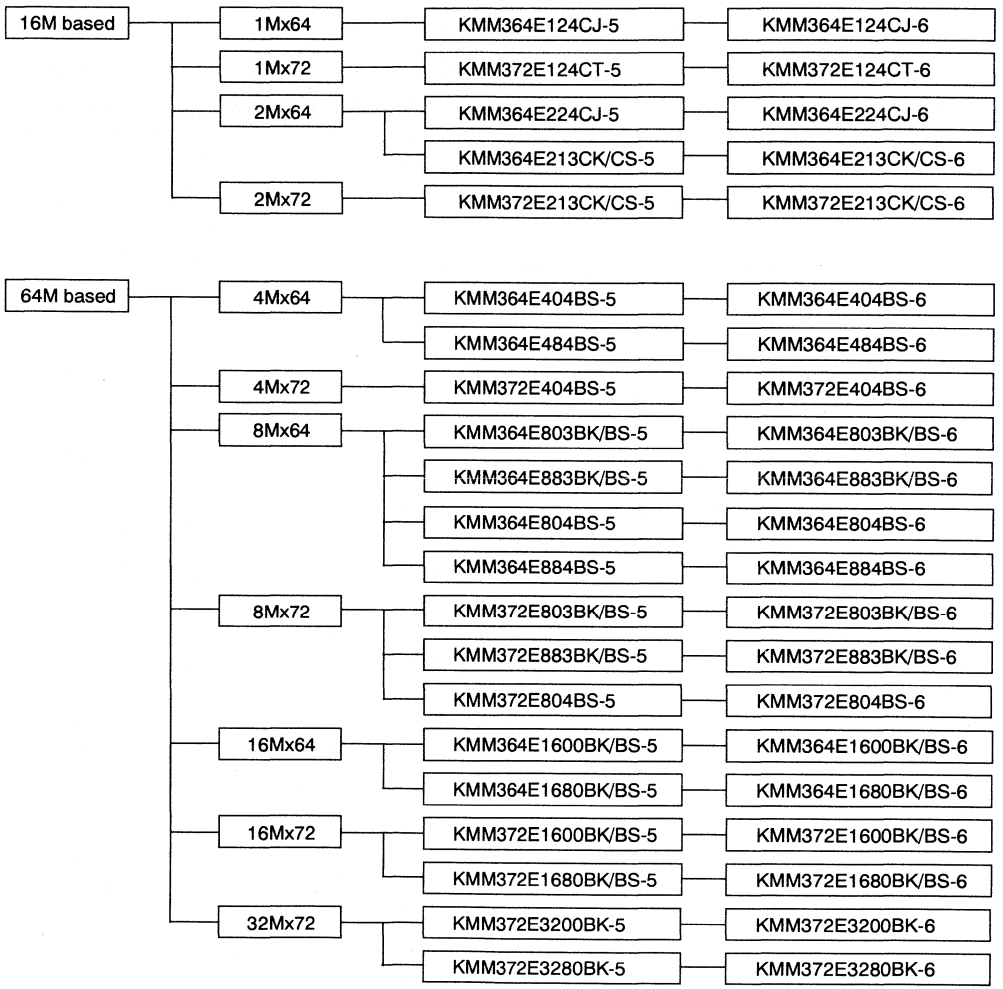
III-II. Extended Data-Out (EDO) Mode

Buffered DIMM(3.3V)



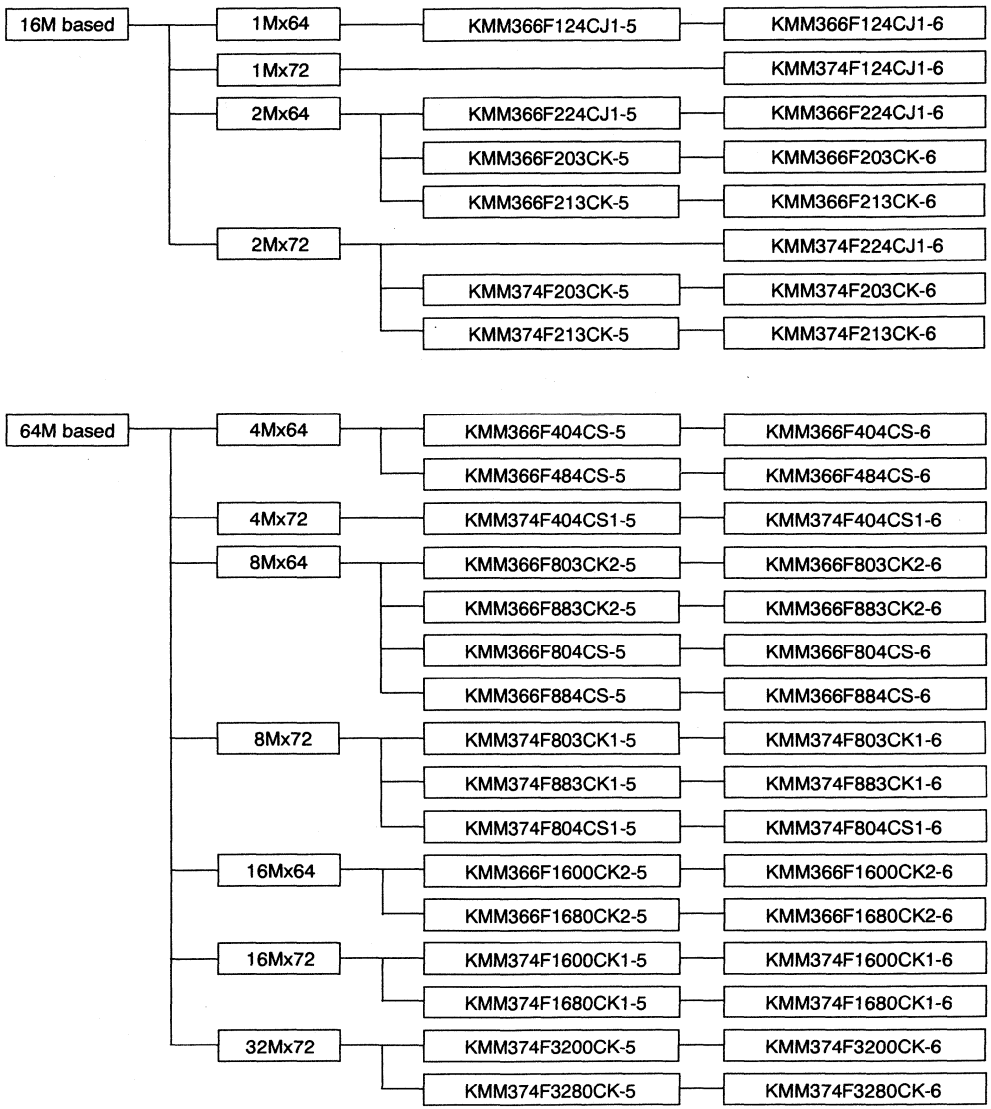
III-II. Extended Data-Out (EDO) Mode -- Continued

Buffered DIMM(5V)



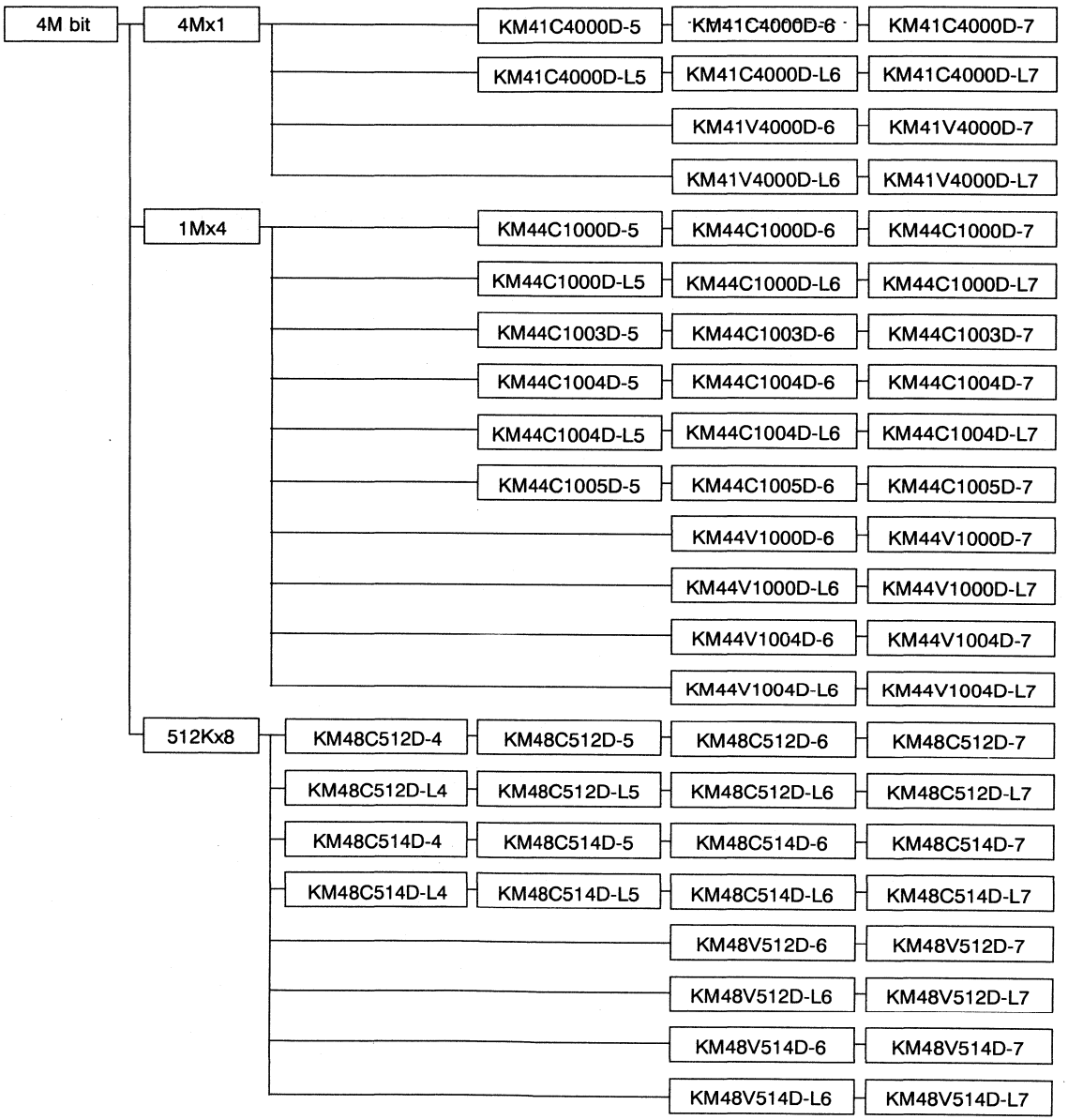
III-II. Extended Data-Out (EDO) Mode -- Continued

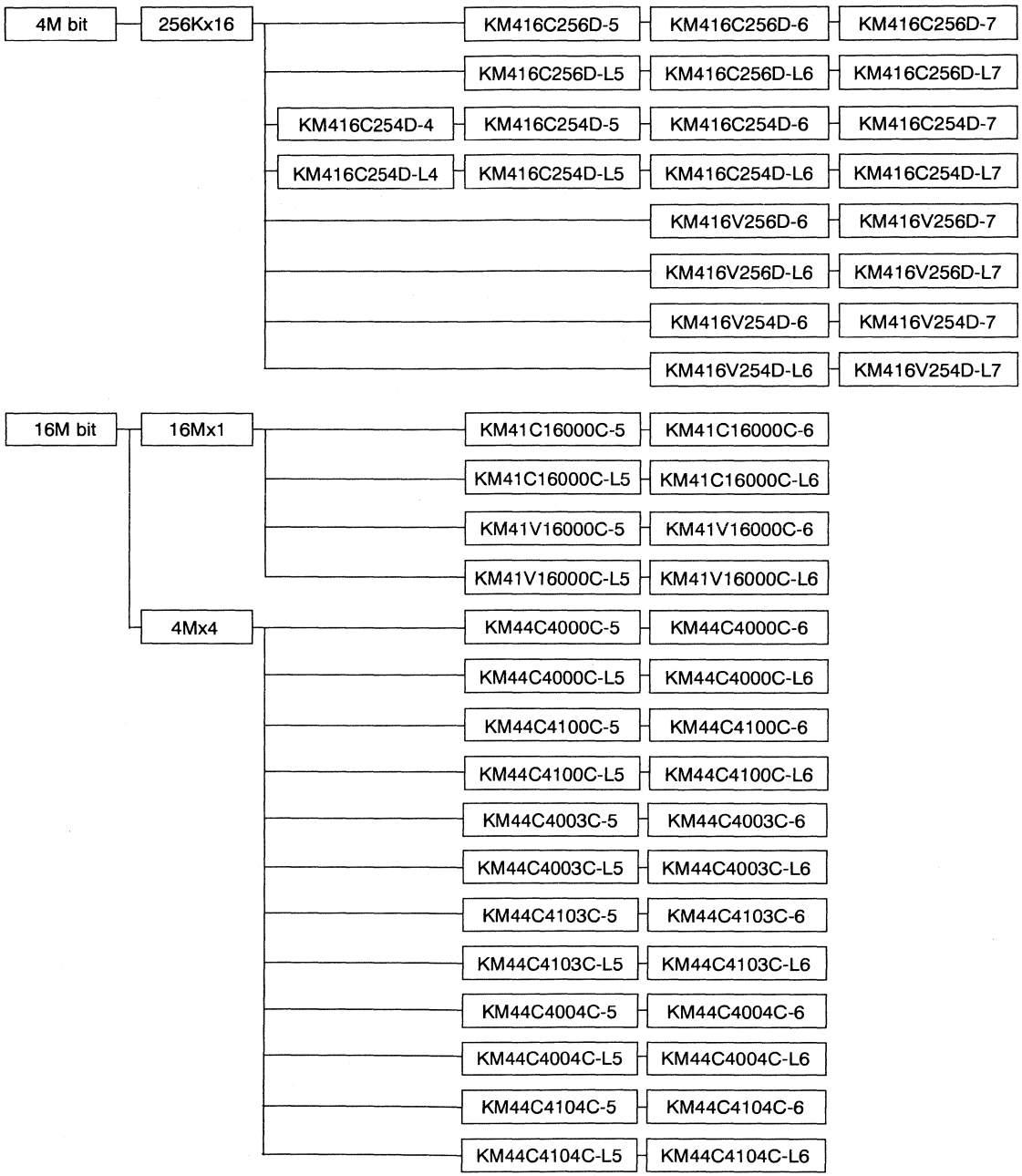
Unbuffered DIMM(3.3V)

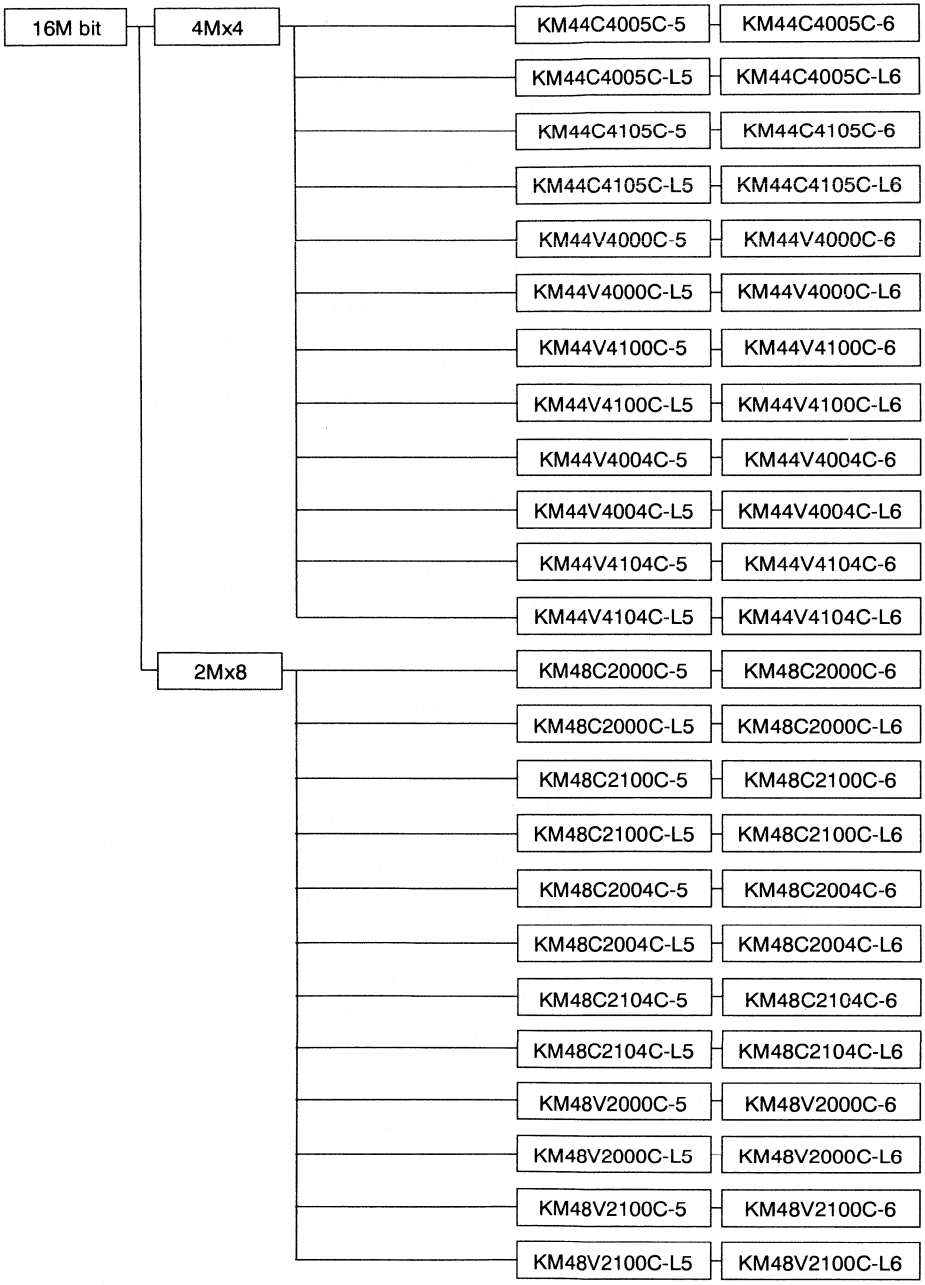


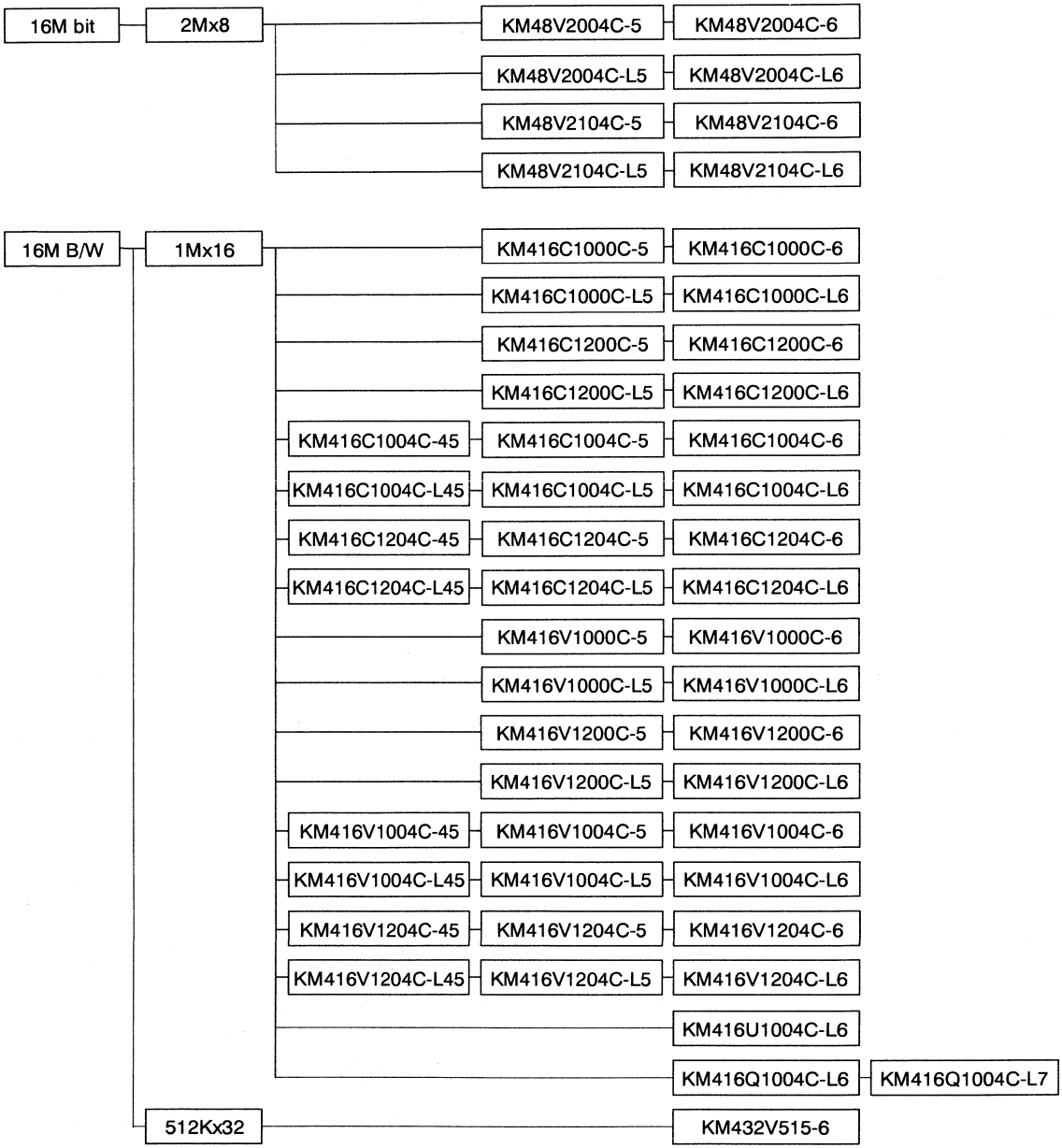
DRAM (for reference)

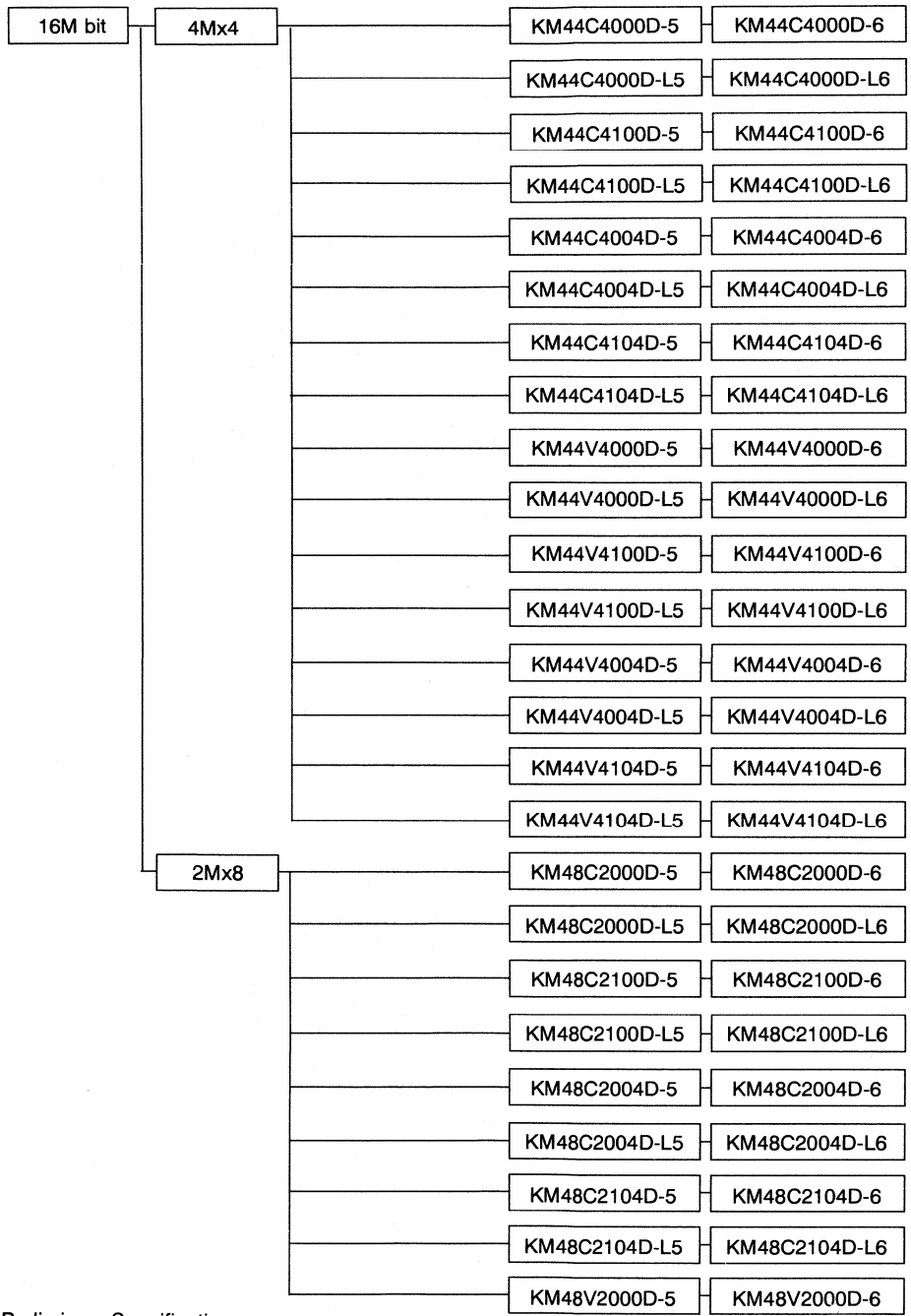
1. Introduction



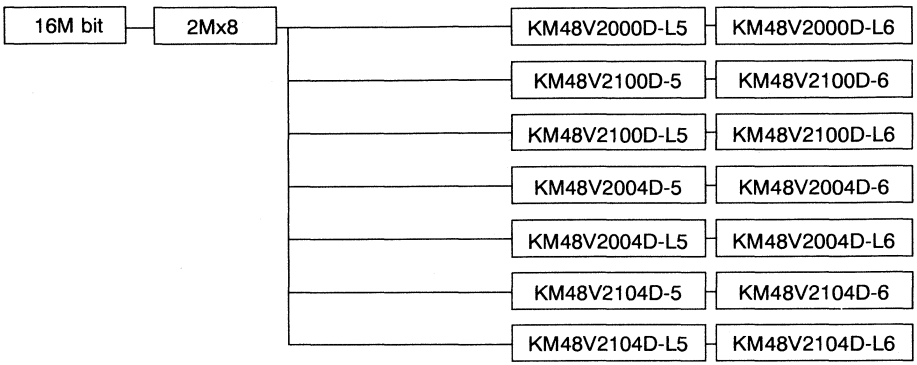

4M bit
256Kx16
KM416C256D-5
KM416C256D-6
KM416C256D-7
KM416C256D-L5
KM416C256D-L6
KM416C256D-L7
KM416C254D-4
KM416C254D-5
KM416C254D-6
KM416C254D-7
KM416C254D-L4
KM416C254D-L5
KM416C254D-L6
KM416C254D-L7
KM416V256D-6
KM416V256D-7
KM416V256D-L6
KM416V256D-L7
KM416V254D-6
KM416V254D-7
KM416V254D-L6
KM416V254D-L7
16M bit
16Mx1
KM41C16000C-5
KM41C16000C-6
KM41C16000C-L5
KM41C16000C-L6
KM41V16000C-5
KM41V16000C-6
KM41V16000C-L5
KM41V16000C-L6
4Mx4
KM44C4000C-5
KM44C4000C-6
KM44C4000C-L5
KM44C4000C-L6
KM44C4100C-5
KM44C4100C-6
KM44C4100C-L5
KM44C4100C-L6
KM44C4003C-5
KM44C4003C-6
KM44C4003C-L5
KM44C4003C-L6
KM44C4103C-5
KM44C4103C-6
KM44C4103C-L5
KM44C4103C-L6
KM44C4004C-5
KM44C4004C-6
KM44C4004C-L5
KM44C4004C-L6
KM44C4104C-5
KM44C4104C-6
KM44C4104C-L5
KM44C4104C-L6

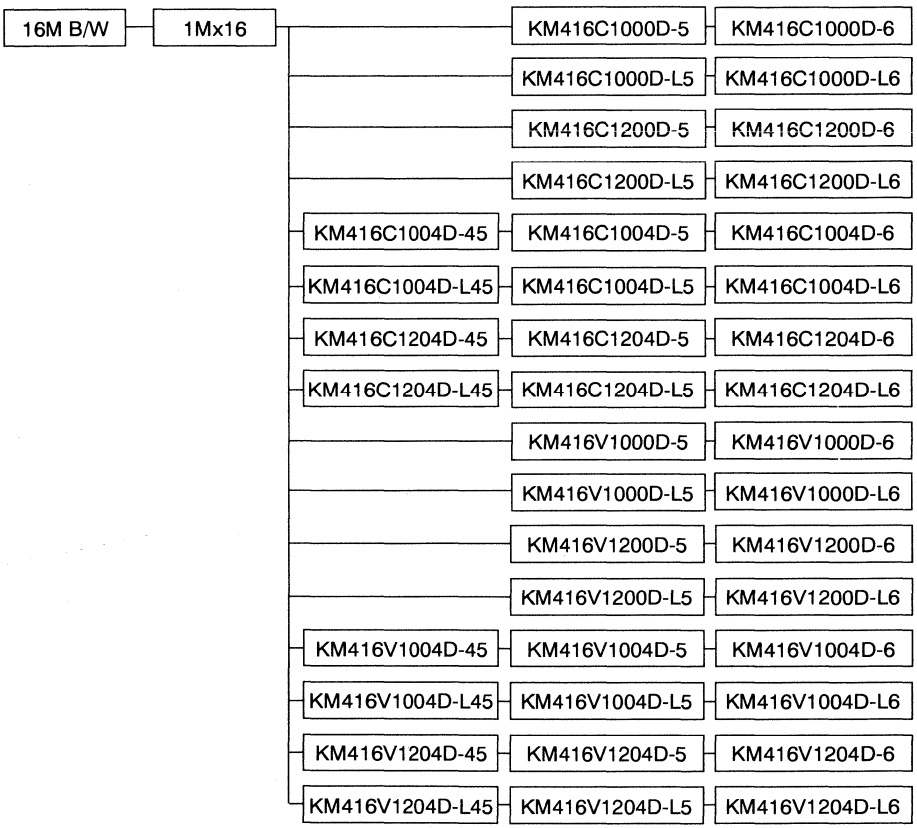

16M bit
4Mx4
KM44C4005C-5
KM44C4005C-6
KM44C4005C-L5
KM44C4005C-L6
KM44C4105C-5
KM44C4105C-6
KM44C4105C-L5
KM44C4105C-L6
KM44V4000C-5
KM44V4000C-6
KM44V4000C-L5
KM44V4000C-L6
KM44V4100C-5
KM44V4100C-6
KM44V4100C-L5
KM44V4100C-L6
KM44V4004C-5
KM44V4004C-6
KM44V4004C-L5
KM44V4004C-L6
KM44V4104C-5
KM44V4104C-6
KM44V4104C-L5
KM44V4104C-L6
2Mx8
KM48C2000C-5
KM48C2000C-6
KM48C2000C-L5
KM48C2000C-L6
KM48C2100C-5
KM48C2100C-6
KM48C2100C-L5
KM48C2100C-L6
KM48C2004C-5
KM48C2004C-6
KM48C2004C-L5
KM48C2004C-L6
KM48C2104C-5
KM48C2104C-6
KM48C2104C-L5
KM48C2104C-L6
KM48V2000C-5
KM48V2000C-6
KM48V2000C-L5
KM48V2000C-L6
KM48V2100C-5
KM48V2100C-6
KM48V2100C-L5
KM48V2100C-L6


16M bit
2Mx8
KM48V2004C-5
KM48V2004C-6
KM48V2004C-L5
KM48V2004C-L6
KM48V2104C-5
KM48V2104C-6
KM48V2104C-L5
KM48V2104C-L6
16M B/W
1Mx16
KM416C1000C-5
KM416C1000C-6
KM416C1000C-L5
KM416C1000C-L6
KM416C1200C-5
KM416C1200C-6
KM416C1200C-L5
KM416C1200C-L6
KM416C1004C-45
KM416C1004C-5
KM416C1004C-6
KM416C1004C-L45
KM416C1004C-L5
KM416C1004C-L6
KM416C1204C-45
KM416C1204C-5
KM416C1204C-6
KM416C1204C-L45
KM416C1204C-L5
KM416C1204C-L6
KM416V1000C-5
KM416V1000C-6
KM416V1000C-L5
KM416V1000C-L6
KM416V1200C-5
KM416V1200C-6
KM416V1200C-L5
KM416V1200C-L6
KM416V1004C-45
KM416V1004C-5
KM416V1004C-6
KM416V1004C-L45
KM416V1004C-L5
KM416V1004C-L6
KM416V1204C-45
KM416V1204C-5
KM416V1204C-6
KM416V1204C-L45
KM416V1204C-L5
KM416V1204C-L6
KM416U1004C-L6
KM416Q1004C-L6
KM416Q1004C-L7
512Kx32
KM432V515-6

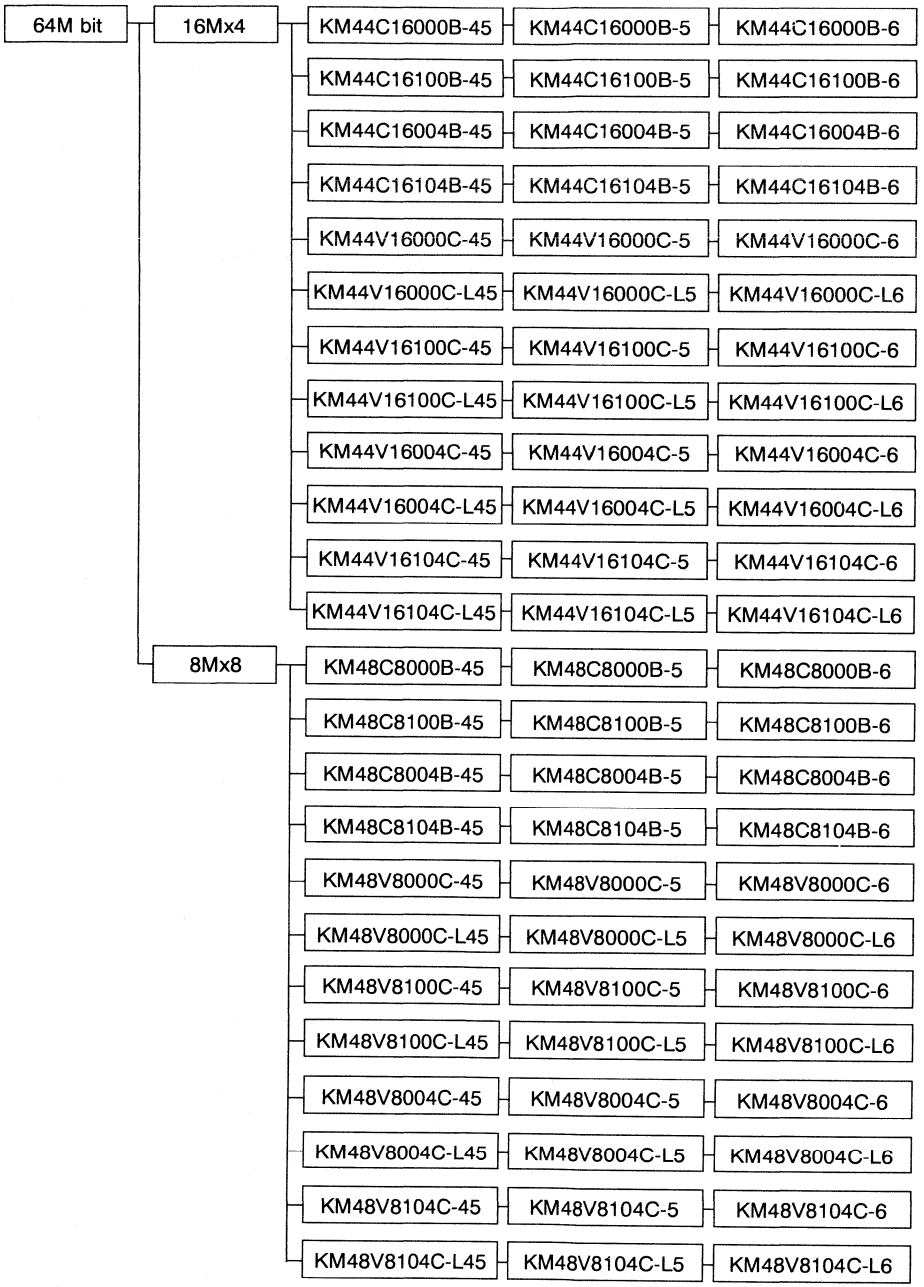


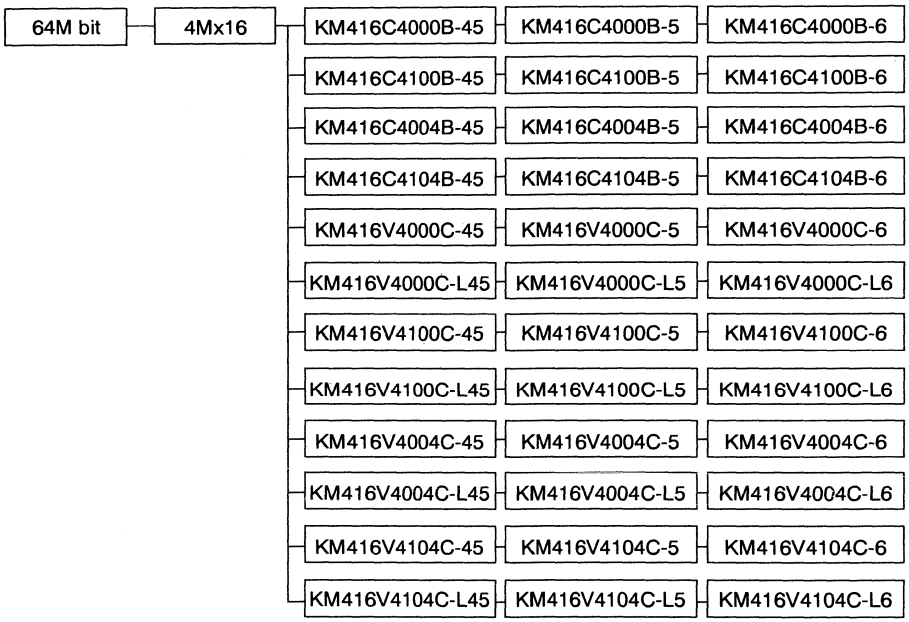
* Preliminary Specification





* Preliminary Specification


64M bit
16Mx4
KM44C16000B-45
KM44C16000B-5
KM44C16000B-6
KM44C16100B-45
KM44C16100B-5
KM44C16100B-6
KM44C16004B-45
KM44C16004B-5
KM44C16004B-6
KM44C16104B-45
KM44C16104B-5
KM44C16104B-6
KM44V16000C-45
KM44V16000C-5
KM44V16000C-6
KM44V16000C-L45
KM44V16000C-L5
KM44V16000C-L6
KM44V16100C-45
KM44V16100C-5
KM44V16100C-6
KM44V16100C-L45
KM44V16100C-L5
KM44V16100C-L6
KM44V16004C-45
KM44V16004C-5
KM44V16004C-6
KM44V16004C-L45
KM44V16004C-L5
KM44V16004C-L6
KM44V16104C-45
KM44V16104C-5
KM44V16104C-6
KM44V16104C-L45
KM44V16104C-L5
KM44V16104C-L6
8Mx8
KM48C8000B-45
KM48C8000B-5
KM48C8000B-6
KM48C8100B-45
KM48C8100B-5
KM48C8100B-6
KM48C8004B-45
KM48C8004B-5
KM48C8004B-6
KM48C8104B-45
KM48C8104B-5
KM48C8104B-6
KM48V8000C-45
KM48V8000C-5
KM48V8000C-6
KM48V8000C-L45
KM48V8000C-L5
KM48V8000C-L6
KM48V8100C-45
KM48V8100C-5
KM48V8100C-6
KM48V8100C-L45
KM48V8100C-L5
KM48V8100C-L6
KM48V8004C-45
KM48V8004C-5
KM48V8004C-6
KM48V8004C-L45
KM48V8004C-L5
KM48V8004C-L6
KM48V8104C-45
KM48V8104C-5
KM48V8104C-6
KM48V8104C-L45
KM48V8104C-L5
KM48V8104C-L6


64M bit
4Mx16
KM416C4000B-45
KM416C4000B-5
KM416C4000B-6
KM416C4100B-45
KM416C4100B-5
KM416C4100B-6
KM416C4004B-45
KM416C4004B-5
KM416C4004B-6
KM416C4104B-45
KM416C4104B-5
KM416C4104B-6
KM416V4000C-45
KM416V4000C-5
KM416V4000C-6
KM416V4000C-L45
KM416V4000C-L5
KM416V4000C-L6
KM416V4100C-45
KM416V4100C-5
KM416V4100C-6
KM416V4100C-L45
KM416V4100C-L5
KM416V4100C-L6
KM416V4004C-45
KM416V4004C-5
KM416V4004C-6
KM416V4004C-L45
KM416V4004C-L5
KM416V4004C-L6
KM416V4104C-45
KM416V4104C-5
KM416V4104C-6
KM416V4104C-L45
KM416V4104C-L5
KM416V4104C-L6

2. Product Guide

Org.	Part No.	Base	Vtg.	Mode*6	Ref.*7	Bank	PKG*8	Height	Tab*9	CS
4Byte Single In-Line Memory Module(SIMM)										
4Mx32	KMM5324000BSW/BSWG	4Mx16	5V	FP	4K	1	S	1.00"	G/S	Now
	KMM5324004BSW/BSWG	4Mx16	5V	EDO	4K	1	S	1.00"	G/S	Now
4Mx36*2	KMM5364003BSW/BSWG	4Mx16	5V	FP	4K	1	S	1.00"	G/S	Now
	KMM5364005BSW/BSWG	4Mx16	5V	EDO	4K	1	S	1.00"	G/S	Now
8Mx32	KMM5328000BSW/BSWG	4Mx16	5V	FP	4K	2	S	1.00"	G/S	Now
	KMM5328004BSW/BSWG	4Mx16	5V	EDO	4K	2	S	1.00"	G/S	Now
8Mx36*2	KMM5368003BSW/BSWG	4Mx16	5V	FP	4K	2	S	1.00"	G/S	Now
	KMM5368005BSW/BSWG	4Mx16	5V	EDO	4K	2	S	1.00"	G/S	Now
16Mx32	KMM53216000BK/BKG	16Mx4	5V	FP	4K	1	K	1.25"	G/S	Now
	KMM53216004BK/BKG	16Mx4	5V	EDO	4K	1	K	1.25"	G/S	Now
	KMM53216000BV/BVG	16Mx4	5V	FP	4K	1	K	1.00"	G/S	Now
	KMM53216004BV/BVG	16Mx4	5V	EDO	4K	1	K	1.00"	G/S	Now
16Mx36*2	KMM53616000BK/BKG	16Mx4	5V	FP	4K	1	K	1.25"	G/S	Now
	KMM53616004BK/BKG	16Mx4	5V	EDO	4K	1	K	1.25"	G/S	Now
32Mx32	KMM53232000BK/BKG	16Mx4	5V	FP	4K	2	K	1.42"	G/S	Now
	KMM53232004BK/BKG	16Mx4	5V	EDO	4K	2	K	1.42"	G/S	Now
	KMM53232000BV/BVG	16Mx4	5V	FP	4K	2	K	1.00"	G/S	Now
	KMM53232004BV/BVG	16Mx4	5V	EDO	4K	2	K	1.00"	G/S	Now
32Mx36*3	KMM53632000BK/BKG	16Mx4	5V	FP	4K	2	K	1.42"	G/S	Now
	KMM53632004BK/BKG	16Mx4	5V	EDO	4K	2	K	1.42"	G/S	Now
8Byte Small Out-Line Dual In-Line Memory Module(SODIMM)										
1Mx64	KMM466F124CT1-L	1Mx16	3.3V	EDO	1K	1	T	1.00"	G	Now
	KMM466F104CT1-L	1Mx16	3.3V	EDO	4K	1	T	1.00"	G	Now
2Mx64	KMM466F213CS2-L	2Mx8	3.3V	EDO	2K	1	S	1.00"	G	Now
	KMM466F203CS2-L	2Mx8	3.3V	EDO	4K	1	S	1.00"	G	Now
4Mx64	KMM466F404CS2-L	4Mx16	3.3V	EDO	4K	1	S	1.00"	G	Now
8Mx64	KMM466F803CS2-L	8Mx8	3.3V	EDO	4K	1	S	1.10"	G	Now
	KMM466F804CS1-L	4Mx16	3.3V	EDO	4K	2	S	1.00"	G	Now
8Byte Buffered Dual In-Line Memory Module(DIMM-3.3V)										
1Mx72*4	KMM372V124CT	1Mx16	3.3V	FP	1K	1	T	1.00"	G	Now
	KMM372F124CT	1Mx16	3.3V	EDO	1K	1	T	1.00"	G	Now
	KMM372F124CJ	1Mx16	3.3V	EDO	1K	1	J	1.00"	G	Now
2Mx72	KMM372V213CK/CS	2Mx8	3.3V	FP	2K	1	K/S	1.00"	G	Now
	KMM372F213CK/CS	2Mx8	3.3V	EDO	2K	1	K/S	1.00"	G	Now

Org.	Part No.	Base	Vtg.	Mode*6	Ref.*7	Bank	PKG*8	Height	Tab*9	CS
8Byte Buffered Dual In-Line Memory Module(DIMM-3.3V) Continued										
4Mx72*5	KMM372V404CS	4Mx16	3.3V	FP	4K	1	S	1.00"	G	Now
	KMM372F404CS	4Mx16	3.3V	EDO	4K	1	S	1.00"	G	Now
8Mx72	KMM372V803CK/CS	8Mx8	3.3V	FP	4K	1	S	1.25"	G	Now
	KMM372V883CK/CS	8Mx8	3.3V	FP	8K	1	S	1.25"	G	Now
	KMM372F803CK/CS	8Mx8	3.3V	EDO	4K	1	S	1.25"	G	Now
	KMM372F883CK/CS	8Mx8	3.3V	EDO	8K	1	S	1.25"	G	Now
8Mx72*5	KMM372V804CS	4Mx16	3.3V	FP	4K	2	S	1.00"	G	Now
	KMM372F804CS	4Mx16	3.3V	EDO	4K	2	S	1.00"	G	Now
16Mx72	KMM372V1600CK/CS	16Mx4	3.3V	FP	4K	1	K/S	1.25"	G	Now
	KMM372V1680CK/CS	16Mx4	3.3V	FP	8K	1	K/S	1.25"	G	Now
	KMM372F1600CK/CS	16Mx4	3.3V	EDO	4K	1	K/S	1.25"	G	Now
	KMM372F1680CK/CS	16Mx4	3.3V	EDO	8K	1	K/S	1.25"	G	Now
32Mx72	KMM372V3200CS1	16Mx4	3.3V	FP	4K	2	S	2.10"	G	Now
	KMM372V3280CS1	16Mx4	3.3V	FP	8K	2	S	2.10"	G	Now
	KMM372V3200CK4	16Mx4	3.3V	FP	4K	2	K	2.00"	G	Now
	KMM372V3280CK4	16Mx4	3.3V	FP	8K	2	K	2.00"	G	Now
	KMM372V3200CK3	16Mx4	3.3V	FP	4K	2	K	1.65"	G	Now
	KMM372V3280CK3	16Mx4	3.3V	FP	8K	2	K	1.65"	G	Now
	KMM372F3200CS1	16Mx4	3.3V	EDO	4K	2	S	2.10"	G	Now
	KMM372F3280CS1	16Mx4	3.3V	EDO	8K	2	S	2.10"	G	Now
	KMM372F3200CK4	16Mx4	3.3V	EDO	4K	2	K	2.00"	G	Now
	KMM372F3280CK4	16Mx4	3.3V	EDO	8K	2	K	2.00"	G	Now
	KMM372F3200CK3	16Mx4	3.3V	EDO	4K	2	K	1.65"	G	Now
	KMM372F3280CK3	16Mx4	3.3V	EDO	8K	2	K	1.65"	G	Now
8Byte Buffered Dual In-Line Memory Module(DIMM-5V)										
1Mx64	KMM364C124CJ	1Mx16	5V	FP	1K	1	J	1.00"	G	Now
	KMM364E124CJ	1Mx16	5V	EDO	1K	1	J	1.00"	G	Now
1Mx72*4	KMM372C124CT	1Mx16	5V	FP	1K	1	T	1.00"	G	Now
	KMM372E124CT	1Mx16	5V	EDO	1K	1	T	1.00"	G	Now
2Mx64	KMM364C224CJ	1Mx16	5V	FP	1K	2	J	1.00"	G	Now
	KMM364E224CJ	1Mx16	5V	EDO	1K	2	J	1.00"	G	Now
	KMM364C213CK/CS	2Mx8	5V	FP	2K	1	K/S	1.00"	G	Now
	KMM364E213CK/CS	2Mx8	5V	EDO	2K	1	K/S	1.00"	G	Now
2Mx72	KMM372C213CK/CS	2Mx8	5V	FP	2K	1	K/S	1.00"	G	Now
	KMM372E213CK/CS	2Mx8	5V	EDO	2K	1	K/S	1.00"	G	Now

Org.	Part No.	Base	Vtg.	Mode*6	Ref.*7	Bank	PKG*8	Height	Tab*9	CS
8Byte Buffered Dual In-Line Memory Module(DIMM-5V) Continued										
4Mx64	KMM364C404BS	4Mx16	5V	FP	4K	1	S	1.00"	G	Now
	KMM364C484BS	4Mx16	5V	FP	8K	1	S	1.00"	G	Now
	KMM364E404BS	4Mx16	5V	EDO	4K	1	S	1.00"	G	Now
	KMM364E484BS	4Mx16	5V	EDO	8K	1	S	1.00"	G	Now
4Mx72	KMM372C404BS	4Mx16	5V	FP	4K	1	S	1.00"	G	Now
	KMM372E404BS	4Mx16	5V	EDO	4K	1	S	1.00"	G	Now
8Mx64	KMM364C803BK/BS	8Mx8	5V	FP	4K	1	K/S	1.25"	G	Now
	KMM364C883BK/BS	8Mx8	5V	FP	8K	1	K/S	1.25"	G	Now
	KMM364E803BK/BS	8Mx8	5V	EDO	4K	1	K/S	1.25"	G	Now
	KMM364E883BK/BS	8Mx8	5V	EDO	8K	1	K/S	1.25"	G	Now
	KMM364C804BS	4Mx16	5V	FP	4K	2	S	1.00"	G	Now
	KMM364C884BS	4Mx16	5V	FP	8K	2	S	1.00"	G	Now
	KMM364E804BS	4Mx16	5V	EDO	4K	2	S	1.00"	G	Now
	KMM364E884BS	4Mx16	5V	EDO	8K	2	S	1.00"	G	Now
8MX72	KMM372C803BK/BS	8Mx8	5V	FP	4K	1	K/S	1.25"	G	Now
	KMM372C883BK/BS	8Mx8	5V	FP	8K	1	K/S	1.25"	G	Now
	KMM372E803BK/BS	8Mx8	5V	EDO	4K	1	K/S	1.25"	G	Now
	KMM372E883BK/BS	8Mx8	5V	EDO	8K	1	K/S	1.25"	G	Now
	KMM372C804BS	4Mx16	5V	FP	4K	2	S	1.00"	G	Now
	KMM372E804BS	4Mx16	5V	EDO	4K	2	S	1.00"	G	Now
16Mx64	KMM364C1600BK/BS	16Mx4	5V	FP	4K	1	K/S	1.25"	G	Now
	KMM364C1680BK/BS	16Mx4	5V	FP	8K	1	K/S	1.25"	G	Now
	KMM364E1600BK/BS	16Mx4	5V	EDO	4K	1	K/S	1.25"	G	Now
	KMM364E1680BK/BS	16Mx4	5V	EDO	8K	1	K/S	1.25"	G	Now
16Mx72	KMM372C1600BK/BS	16Mx4	5V	FP	4K	1	K/S	1.25"	G	Now
	KMM372C1680BK/BS	16Mx4	5V	FP	8K	1	K/S	1.25"	G	Now
	KMM372E1600BK/BS	16Mx4	5V	EDO	4K	1	K/S	1.25"	G	Now
	KMM372E1680BK/BS	16Mx4	5V	EDO	8K	1	K/S	1.25"	G	Now
32Mx72	KMM372C3200BK	16Mx4	5V	FP	4K	2	K	2.00"	G	Now
	KMM372C3280BK	16Mx4	5V	FP	8K	2	K	2.00"	G	Now
	KMM372E3200BK	16Mx4	5V	EDO	4K	2	K	2.00"	G	Now
	KMM372E3280BK	16Mx4	5V	EDO	8K	2	K	2.00"	G	Now
8Byte Unbuffered Dual In-Line Memory Module(DIMM-3.3V)										
1Mx64	KMM366F124CJ1	1Mx16	3.3V	EDO	1K	1	J	1.00"	G	Now
1Mx72*4	KMM374F124CJ1	1Mx16	3.3V	EDO	1K	1	J	1.00"	G	Now

Org.	Part No.	Base	Vtg.	Mode*6	Ref.*7	Bank	PKG*8	Height	Tab*9	CS
8Byte Unbuffered Dual In-Line Memory Module(DIMM-3.3V) Continued										
2Mx64	KMM366F224CJ1	1Mx16	3.3V	EDO	1K	2	T	1.00"	G	Now
	KMM366F213CK	2Mx8	3.3V	EDO	2K	1	K	1.00"	G	Now
	KMM366F203CK	2Mx8	3.3V	EDO	4K	1	K	1.00"	G	Now
2Mx72*4	KMM374F224CJ1	1Mx16	3.3V	EDO	1K	2	J	1.00"	G	Now
2Mx72	KMM374F213CK	2Mx8	3.3V	EDO	2K	1	K	1.00"	G	Now
	KMM374F203CK	2Mx8	3.3V	EDO	4K	1	K	1.00"	G	Now
4Mx64	KMM366F404CS1	4Mx16	3.3V	EDO	4K	1	S	1.00"	G	Now
	KMM366F484CS1	4Mx16	3.3V	EDO	8K	1	S	1.00"	G	Now
4MX72*5	KMM374F404CS1	4Mx16	3.3V	EDO	4K	1	S	1.00"	G	Now
8Mx64	KMM366F803CK2	8Mx8	3.3V	EDO	4K	1	K	1.00"	G	Now
	KMM366F883CK2	8Mx8	3.3V	EDO	8K	1	K	1.00"	G	Now
	KMM366F804CS1	4Mx16	3.3V	EDO	4K	2	S	1.00"	G	Now
	KMM366F884CS1	4Mx16	3.3V	EDO	8K	2	S	1.00"	G	Now
8MX72	KMM374F803CK1	8Mx8	3.3V	EDO	4K	1	K	1.00"	G	Now
	KMM374F883CK1	8Mx8	3.3V	EDO	8K	1	K	1.00"	G	Now
8MX72*5	KMM374F804CS1	4Mx16	3.3V	EDO	4K	2	S	1.00"	G	Now
16Mx64	KMM366F1600CK2	16Mx4	3.3V	EDO	4K	1	K	1.00"	G	Now
	KMM366F1680CK2	16Mx4	3.3V	EDO	8K	1	K	1.00"	G	Now
16MX72	KMM374F1600CK1	16Mx4	3.3V	EDO	4K	1	K	1.00"	G	Now
	KMM374F1680CK1	16Mx4	3.3V	EDO	8K	1	K	1.00"	G	Now
32Mx72	KMM374F3200CK1	16Mx4	3.3V	EDO	4K	2	K	1.625"	G	Now
	KMM374F3280CK1	16Mx4	3.3V	EDO	8K	2	K	1.625"	G	Now

Note

*1 ~*5 : Error checking DRAM data width is as follows ;

*1 : Quad $\overline{CAS}$ 1M X 4.
*2 : Quad $\overline{CAS}$ 4M X 4.
*3 : 16M X1.
*4 : 1M X4.
*5 : 4MX4.

*6 : FP - Fast Page Mode, EDO - Extended Data Out Mode.

*7 : 1K - 1024cycles/16ms,
2K - 2048cycles/32ms,
4K - 4096cycles/64ms,
8K - 4096cycles/64ms (CBR), 8192cycles/64ms (ROR).

*8 : Package
a. 16M base - J : 400mil SOJ, K : 300mil SOJ, T : 400mil TSOP II, S : 300mil TSOP II.
b. 64M base - K : 400mil SOJ, S : 400mil TSOP II.

*9 : G - Gold, S - Solder.

DRAM Component (for reference)

Density	Org.	Power Supply	Part Number	Speed (ns)	Features	Packages (#)
4M bit	4Mx1	+5V±10%	KM41C4000D#	50/60/70	FP	J:20pin SOJ T:20pin TSOP-II * Quad CAS J:24pin SOJ T:24pin TSOP-II
			KM41C4000D#-L		FP, LP	
		+3.3V±0.3V	KM41V4000D#	60/70	FP	
			KM41V4000D#-L		FP, LP	
	1Mx4	+5V±10%	KM44C1000D#	50/60/70	FP	
			KM44C1000D#-L		FP, LP	
			KM44C1003D#		Quad $\overline{CAS}$ FP	
			KM44C1004D#		EDO	
			KM44C1004D#-L		EDO, LP	
			KM44C1005D#		Quad $\overline{CAS}$ EDO	
		+3.3V±0.3V	KM44V1000D#	60/70	FP	
			KM44V1000D#-L		FP, LP	
			KM44V1004D#		EDO	
			KM44V1004D#-L		EDO, LP	
	512Kx8	+5V±10%	KM48C512D#	40/50/60/70	FP	J:28pin SOJ T:28pin TSOP-II
			KM48C512D#-L		FP, LP	
			KM48C514D#		EDO	
			KM48C514D#-L		EDO, LP	
		+3.3V±0.3V	KM48V512D#	60/70	FP	
			KM48V512D#-L		FP, LP	
			KM48V514D#		EDO	
			KM48V514D#-L		EDO, LP	
	256Kx16	+5V±10%	KM416C256D#	50/60/70	FP	J:40pin SOJ T:44(40)pin TSOP-II
			KM416C256D#-L		FP, LP	
			KM416C254D#	40/50/60/70	EDO	
			KM416C254D#-L		EDO, LP	
		+3.3V±0.3V	KM416V256D#	60/70	FP	
			KM416V256D#-L		FP, LP	
			KM416V254D#		EDO	
			KM416V254D#-L		EDO, LP	
16M bit	16Mx1	+5V±10%	KM41C16000C#	50/60	FP	K:26(24)pin SOJ (300mil) S:26(24)pin TSOP-II (300mil)
			KM41C16000C#-L		FP, LP	
		+3.3V±0.3V	KM41V16000C#		FP	
			KM41V16000C#-L		FP, LP	

Density	Org.	Power Supply	Part Number	Speed (ns)	Features	Packages (#)
16M bit	4Mx4	+5V±10%	KM44C4000C#	50/60	FP	K:26(24)pin SOJ (300mil) S:26(24)pin TSOP-II (300mil)
			KM44C4000C#-L		FP, LP	
			KM44C4100C#		FP	
			KM44C4100C#-L		FP, LP	
			KM44C4003C#		Quad $\overline{CAS}$ FP, 4K	
			KM44C4003C#-L		Quad $\overline{CAS}$ FP, 4K,LP	
			KM44C4103C#		Quad $\overline{CAS}$ FP, 2K	
			KM44C4103C#-L		Quad $\overline{CAS}$ FP, 2K,LP	
			KM44C4004C#		EDO	
			KM44C4004C#-L		EDO, LP	
			KM44C4104C#		EDO	
			KM44C4104C#-L		EDO, LP	
			KM44C4005C#		Quad $\overline{CAS}$ EDO, 4K	
			KM44C4005C#-L		Quad $\overline{CAS}$ EDO, 4K,LP	
			KM44C4105C#		Quad $\overline{CAS}$ EDO, 2K	
			KM44C4105C#-L		Quad $\overline{CAS}$ EDO, 2K,LP	
		+3.3V±0.3V	KM44V4000C#	50/60	FP	
			KM44V4000C#-L		FP, LP	
			KM44V4100C#		FP	
			KM44V4100C#-L		FP, LP	
			KM44V4004C#		EDO	
			KM44V4004C#-L		EDO, LP	
			KM44V4104C#		EDO	
			KM44V4104C#-L		EDO, LP	
	2Mx8	+5V±10%	KM48C2000C#	50/60	FP	K:28pin SOJ (300mil) S:28pin TSOP-II (300mil)
			KM48C2000C#-L		FP, LP	
			KM48C2100C#		FP	
			KM48C2100C#-L		FP, LP	
			KM48C2004C#		EDO	
			KM48C2004C#-L		EDO, LP	
			KM48C2104C#		EDO	
			KM48C2104C#-L		EDO, LP	
		+3.3V±0.3V	KM48V2000C#	50/60	FP	
			KM48V2000C#-L		FP, LP	
			KM48V2100C#		FP	
			KM48V2100C#-L		FP, LP	

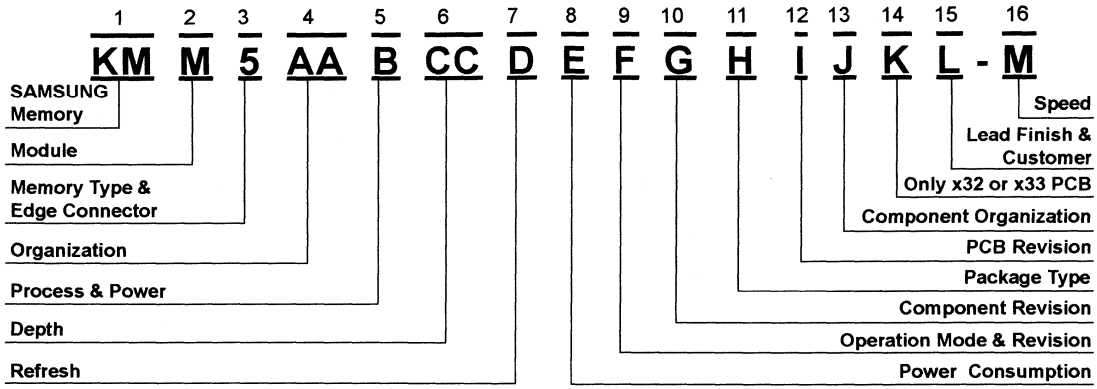
Density	Org.	Power Supply	Part Number	Speed (ns)	Features	Packages (#)
16M bit	2Mx8	+3.3V±0.3V	KM48V2004C#	50/60	EDO	(Continued)
			KM48V2004C#-L		EDO, LP	
			KM48V2104C#		EDO	
			KM48V2104C#-L		EDO, LP	
16M B/W	1Mx16	+5V±10%	KM416C1000C#	50/60	FP	J:42pin SOJ (400mil) T:50(44)pin TSOP-II (400mil)
			KM416C1000C#-L		FP, LP	
			KM416C1200C#		FP	
			KM416C1200C#-L		FP, LP	
			KM416C1004C#	45/50/60	EDO	
			KM416C1004C#-L		EDO, LP	
			KM416C1204C#		EDO	
			KM416C1204C#-L		EDO, LP	
		+3.3V±0.3V	KM416V1000C#	50/60	FP	
			KM416V1000C#-L		FP, LP	
			KM416V1200C#		FP	
			KM416V1200C#-L		FP, LP	
			KM416V1004C#	45/50/60	EDO	
			KM416V1004C#-L		EDO, LP	
			KM416V1204C#		EDO	
			KM416V1204C#-L		EDO, LP	
		3.0V+0.6/-0.3	KM416U1004C#-L	60	EDO, 4K, LP	T:50(44)pin TSOP-II (400mil)
		2.5V±0.2V	KM416Q1004C#-L	60/70	EDO, 4K, LP	
	512Kx32	+3.3V±0.3V	KM432V515#	60	Quad $\overline{CAS}$ EDO, 4K	J:70pin SOJ (400mil)
64M bit	16Mx4	+5V±10%	KM44C16000B#	45/50/60	FP, 8K	K:32pin SOJ (400mil) S:32pin TSOP-II (400mil)
			KM44C16100B#		FP, 4K	
			KM44C16004B#		EDO, 8K	
			KM44C16104B#		EDO, 4K	
		+3.3V±0.3V	KM44V16000C#	45/50/60	FP, 8K	
			KM44V16000C#-L		FP, 8K, LP	
			KM44V16100C#		FP, 4K	
			KM44V16100C#-L		FP, 4K, LP	
			KM44V16004C#		EDO, 8K	
			KM44V16004C#-L		EDO, 8K, LP	
			KM44V16104C#		EDO, 4K	
			KM44V16104C#-L		EDO, 4K, LP	

Density	Org.	Power Supply	Part Number	Speed (ns)	Features	Packages (#)
64M bit	8Mx8	+5V±10%	KM48C8000B#	45/50/60	FP, 8K	K:32pin SOJ (400mil) S:32pin TSOP-II (400mil)
			KM48C8100B#		FP, 4K	
			KM48C8004B#		EDO, 8K	
			KM48C8104B#		EDO, 4K	
		+3.3V±0.3V	KM48V8000C#	45/50/60	FP, 8K	
			KM48V8000C#-L		FP, 8K, LP	
			KM48V8100C#		FP, 4K	
			KM48V8100C#-L		FP, 4K, LP	
			KM48V8004C#		EDO, 8K	
			KM48V8004C#-L		EDO, 8K, LP	
			KM48V8104C#		EDO, 4K	
			KM48V8104C#-L		EDO, 4K, LP	
	4Mx16	+5V±10%	KM416C4000B#	45/50/60	FP, 8K	S:50pin TSOP-II (400mil)
			KM416C4100B#		FP, 4K	
			KM416C4004B#		EDO, 8K	
			KM416C4104B#		EDO, 4K	
		+3.3V±0.3V	KM416V4000C#	45/50/60	FP, 8K	
			KM416V4000C#-L		FP, 8K, LP	
			KM416V4100C#		FP, 4K	
			KM416V4100C#-L		FP, 4K, LP	
			KM416V4004C#		EDO, 8K	
			KM416V4004C#-L		EDO, 8K, LP	
			KM416V4104C#		EDO, 4K	
			KM416V4104C#-L		EDO, 4K, LP	

* Note

FP : Fast Page Mode
LP : Low Power Product
1K : 1024cycles/16ms
4K : 4096cycles/64ms
EDO : Extended Data Out Mode
512 : 512cycles/8ms
2K : 2048cycles/32ms
8K : 4096cycles/64ms (CBR) 8192cycles/64ms (ROR)

SIMM Module Ordering Information



1. SAMSUNG Memory

2. Module

3. Memory Type & Edge Connector

- 3 ---------- DRAM DIMM
- 4 ---------- DRAM 8Byte SODIMM
- **5 ---------- DRAM SIMM**

4. Organization

- 32/36 ---------- x32/x36 bit
- 64/72 ---------- x64/x72 bit

5. Process & Operating Voltage

- Blank ---------- CMOS 5V
- V ---------- CMOS 3.3V

6. Depth

- 32 ---------- 32M
- 16 ---------- 16M
- 8 ---------- 8M
- 4 ---------- 4M

7. Refresh

- 0 ---------- 4K Cycle
- 1 ---------- 2K Cycle
- 2 ---------- 1K Cycle
- 8 ---------- 8K Cycle

8. Power Consumption

- 0 ---------- Normal
- 2 ---------- Low Power & Self Refresh

9. Operation & Organization

- 0 ---------- F/P
- 3 ---------- Using Quad CAS
- 4 ---------- Using EDO
- 5 ---------- Using EDO & Quad CAS

10. Component Revision

- Blank ---------- None
- A ---------- First Rev.
- B ---------- Second Rev.
- C ---------- Third Rev.

11. Package Type

- Blank ---------- SOJ(1st)
- K ---------- SOJ(2nd)
- T ---------- TSOP(1st)
- S ---------- TSOP(2nd)

12. PCB Revision

- Blank ---------- None
- 1 ---------- First Rev.
- 2 ---------- Second Rev.
- 3 ---------- Third Rev.

13. Component Organization

- Blank ---------- x4
- U ---------- x8
- W ---------- x16

14. Only x32 or x33 PCB

- V ---------- x32 or x33 PCB

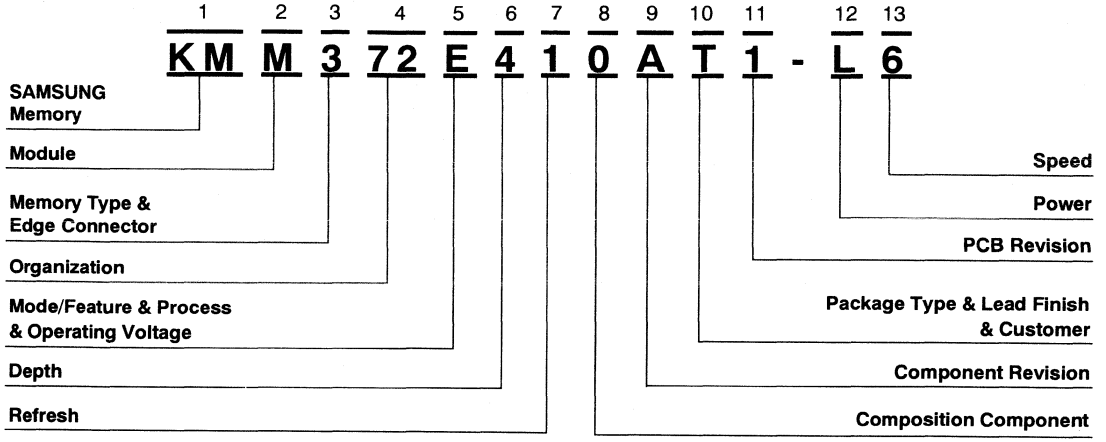
15. Lead Finish & Customer

- Blank ---------- Solder
- G ---------- Gold
- D --------- DEC
- H --------- HP
- M --------- IBM
- P --------- Nickel
- Q --------- Compaq
- X --------- Cambex

16. Speed

- 5 ---------- 50ns
- 6 ---------- 60ns

DIMM/SODIMM Module Ordering Information



1. SAMSUNG Memory

2. Module

3. Memory Type & Edge Connector

- **3 ---------- DRAM DIMM**
- **4 ---------- DRAM 8Byte SODIMM**
- 5 ---------- DRAM SIMM

4. Organization

- 32/36 ---------- x32/x36 bit
- 64/72 ---------- x64/x72 bit
- 66/74 ---------- x64/x72 Unbuffered DIMM
- 144 ---------- x144 bit

5. Mode/Feature & Process & Operating Voltage

- C ---------- F/P,5V
- V ---------- F/P,3.3V
- E ---------- EDO,5V
- F ---------- EDO,3.3V

6. Depth

- 4 ---------- 4M
- 8 ---------- 8M
- 16 ---------- 16M
- 32 ---------- 32M

7. Refresh

- 0 ---------- 4K Cycle
- 1 ---------- 2K Cycle
- 2 ---------- 1K Cycle
- 8 ---------- 8K Cycle

8. Composition Component

- 0 ---------- x4
- 1 ---------- x4 + x1
- 2 ---------- x4 + x4(Quad CAS)
- 3 ---------- x8
- 4 ---------- x16
- 5 ---------- x16 + x4(Quad CAS)

9. Component Revision

- Blank ---------- None
- A ---------- First Rev.
- B ---------- Second Rev.
- C ---------- Third Rev.

10. Package Type & Lead Finish & Customer

- J ---------- SOJ(1st) & Gold
- K ---------- SOJ(2nd) & Gold
- T ---------- TSOP(1st) & Gold
- S ---------- TSOP(2nd) & Gold

11. PCB Revision

- Blank ---------- None
- 1 ---------- First Rev.
- 2 ---------- Second Rev.
- 3 ---------- Third Rev.

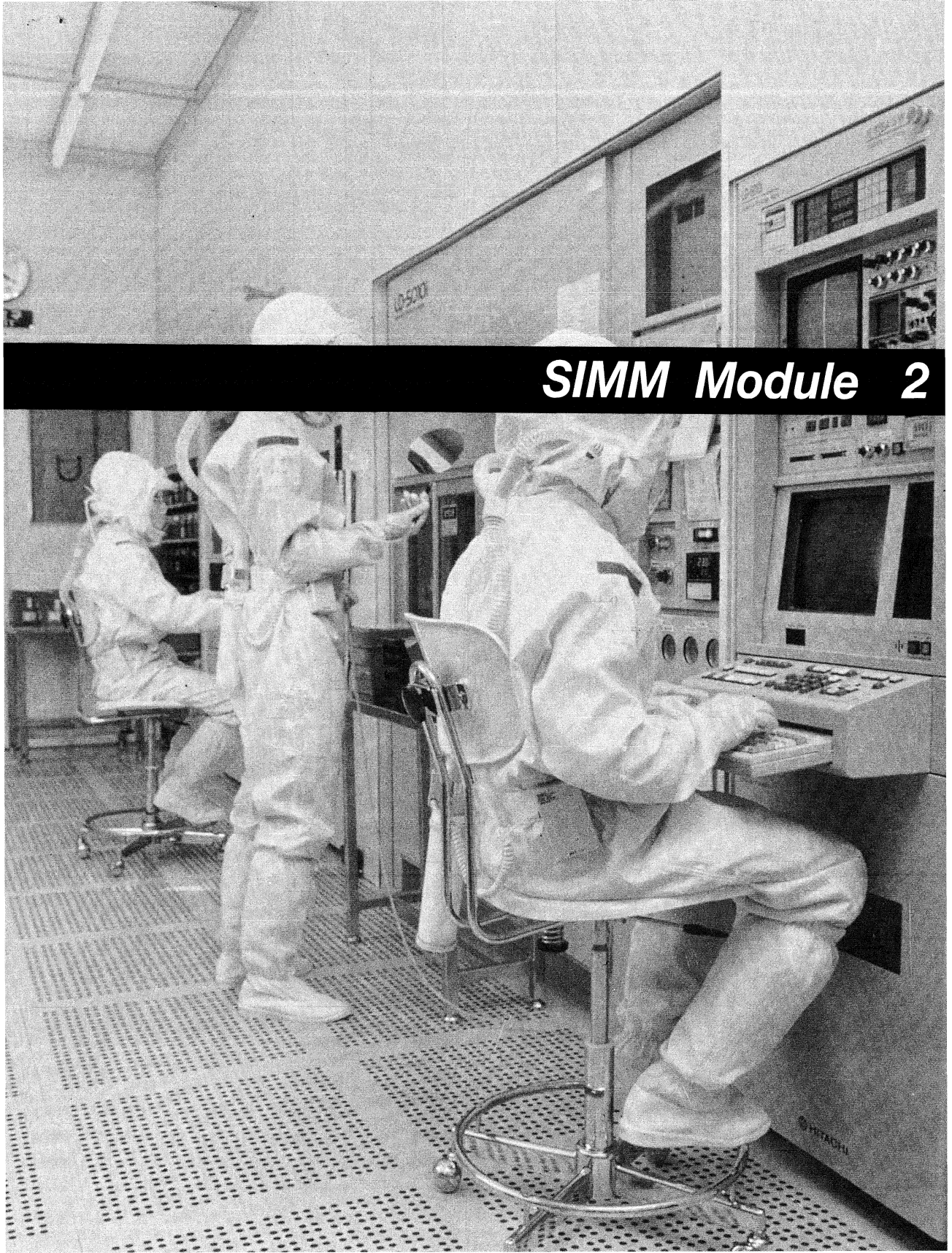
12. Power

- Blank ---------- Normal
- L ---------- Low Power & Self Refresh

13. Speed

- 5 ---------- 50ns
- 6 ---------- 60ns

NOTES


SIMM Module 2

KMM5324000BSW/BSWG Fast Page Mode

4M x 32 DRAM SIMM Using 4Mx16, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM5324000B is a 4Mx32bits Dynamic RAM high density memory module. The Samsung KMM5324000B consists of two CMOS 4Mx16bits DRAMs in TSOP packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM5324000B is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

FEATURES

- Part Identification
  - KMM5324000BSW(4K cycles/64ms Ref, TSOP, Solder)
  - KMM5324000BSWG(4K cycles/64ms Ref, TSOP, Gold)
- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ & Hidden Refresh capability
- $\overline{RAS}$-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1000mil), single sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	NC
2	DQ0	38	NC
3	DQ18	39	$\overline{Vss}$
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	NC
10	Vcc	46	$\overline{NC}$
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	$\overline{NC}$	69	PD3
34	$\overline{RAS2}$	70	PD4
35	NC	71	NC
36	NC	72	Vss

PIN NAMES

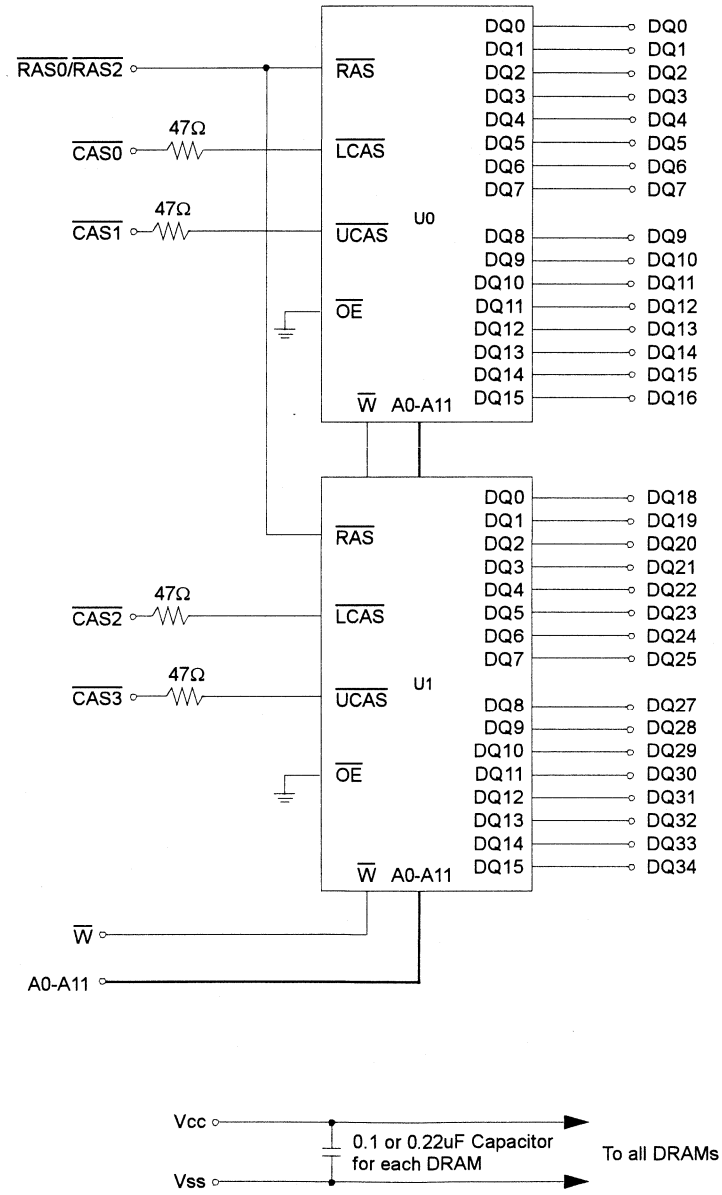
Pin Name	Function
A0 - A11	Address Inputs
DQ0-7, DQ9-16 DQ18-25, DQ27-34	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	Vss	Vss
PD2	NC	NC
PD3	Vss	NC
PD4	Vss	NC

SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	2	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width ≤ 20ns, which is measured at Vcc.

*2 : -2.0V at pulse width ≤ 20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM5324000BSW/BSWG		Unit
		Min	Max	
I_{CC1}	-5	-	240	mA
	-6	-	220	mA
I_{CC2}	Don't care	-	4	mA
I_{CC3}	-5	-	240	mA
	-6	-	220	mA
I_{CC4}	-5	-	140	mA
	-6	-	120	mA
I_{CC5}	Don't care	-	2	mA
I_{CC6}	-5	-	240	mA
	-6	-	220	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	24	pF
Input capacitance[$\overline{RAS0}$/$\overline{RAS2}$]	C_{IN3}	-	24	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	17	pF
Input/Output capacitance[DQ0-7, 9-16,18-25, 27-34]	C_{DQ}	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.6/0.8V, V_{oh}/V_{ol}=2.4/0.4V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns	6
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	10		10		ns	9
Refresh period	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35	ns	3

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.6/0.8V$, $V_{oh}/V_{ol}=2.4/0.4V$, output loading CL=100pF

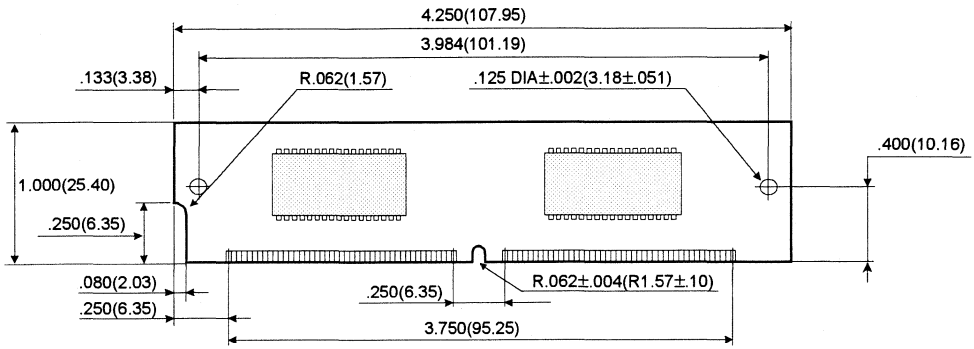
Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	35		40		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	

NOTES

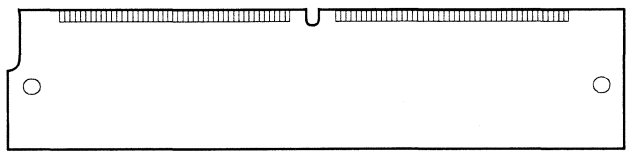
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

PACKAGE DIMENSIONS

Units : Inches (millimeters)

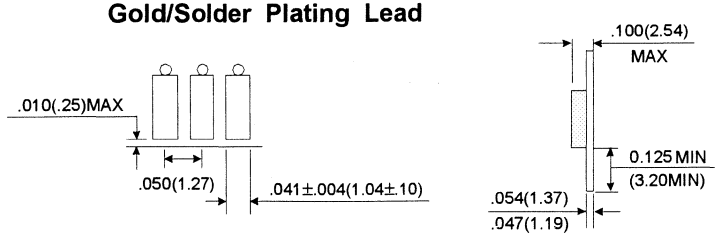


(Front view)



(Back view)

Gold/Solder Plating Lead



Tolerances :±.005(.13) unless otherwise specified

NOTE : The used device is 4Mx16 DRAM, TSOPII
DRAM Part No. : KMM5324000BSW/BSWG -- KM416C4100BS

KMM5324004BSW/BSWG EDO Mode

4M x 32 DRAM SIMM Using 4Mx16, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM5324004B is a 4Mx32bits Dynamic RAM high density memory module. The Samsung KMM5324004B consists of two CMOS 4Mx16bits DRAMs in TSOP packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM5324004B is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

FEATURES

- Part Identification
  - KMM5324004BSW(4K cycles/64ms Ref, TSOP, Solder)
  - KMM5324004BSWG(4K cycles/64ms Ref, TSOP, Gold)
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ & Hidden Refresh capability
- $\overline{RAS}$-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1000mil), single sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	NC
2	DQ0	38	NC
3	DQ18	39	$\overline{Vss}$
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	NC
10	Vcc	46	$\overline{NC}$
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	$\overline{NC}$	69	PD3
34	$\overline{RAS2}$	70	PD4
35	NC	71	NC
36	NC	72	Vss

PIN NAMES

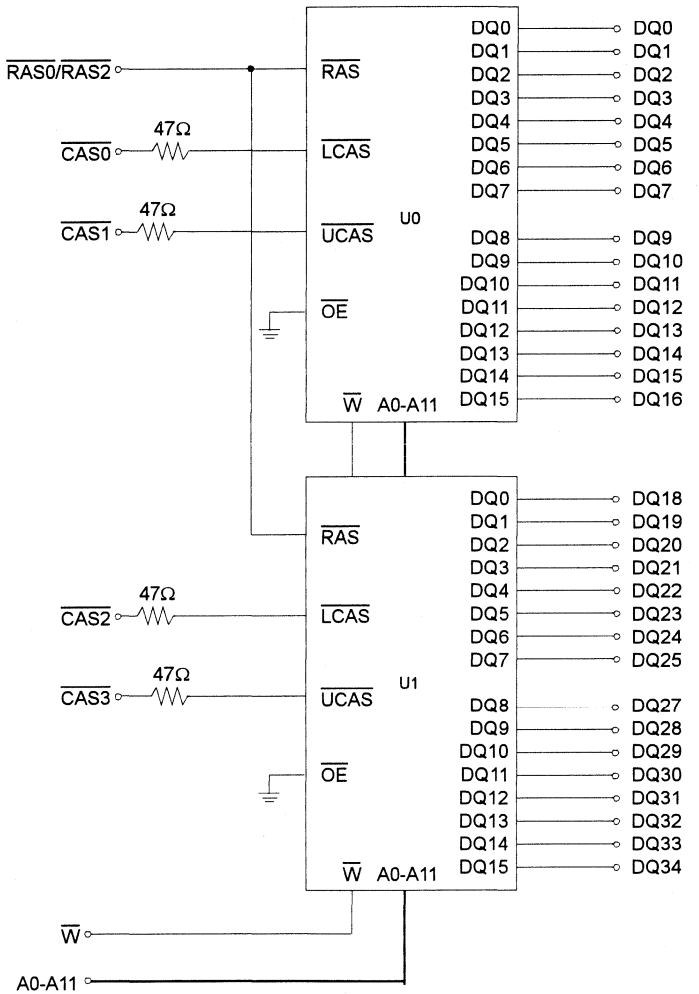
Pin Name	Function
A0 - A11	Address Inputs
DQ0-7, DQ9-16 DQ18-25, DQ27-34	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 - PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

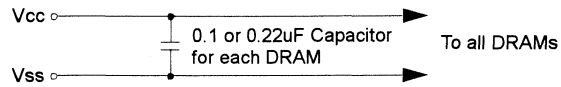
PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	Vss	Vss
PD2	NC	NC
PD3	Vss	NC
PD4	Vss	NC

SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

FUNCTIONAL BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	2	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM5324004BSW/BSWG		Unit
		Min	Max	
I_{CC1}	-5	-	240	mA
	-6	-	220	mA
I_{CC2}	Don't care	-	4	mA
I_{CC3}	-5	-	240	mA
	-6	-	220	mA
I_{CC4}	-5	-	220	mA
	-6	-	200	mA
I_{CC5}	Don't care	-	2	mA
I_{CC6}	-5	-	240	mA
	-6	-	220	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Hyper Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	24	pF
Input capacitance[$\overline{RAS0}$/$\overline{RAS2}$]	C_{IN3}	-	24	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	17	pF
Input/Output capacitance[DQ0-7, 9-16,18-25, 27-34]	C_{DQ}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.6/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	6,12
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		45		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	4
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	8		10		ns	9
Refresh period	t_{REF}		64		64	ms	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.6/0.8V$, $V_{oh}/V_{ol}=2.0/0.8V$, output loading CL=100pF

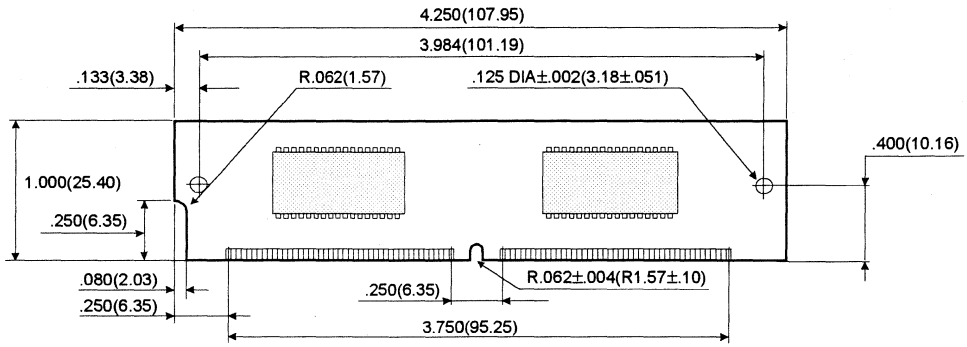
Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Hyper page mode cycle time	t_{HPC}	20		25		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	6,12
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	6
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{W}$ pulse width	t_{WPE}	5		5		ns	

NOTES

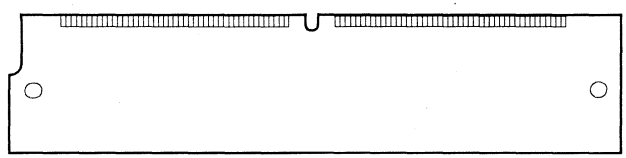
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit and is not referenced for V_{OH} or V_{OL}.
7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit access time is controlled by t_{AA}.
11. $t_{ASC} \geq 6ns$, Assume $t_T=2.0ns$.
12. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

PACKAGE DIMENSIONS

Units : Inches (millimeters)

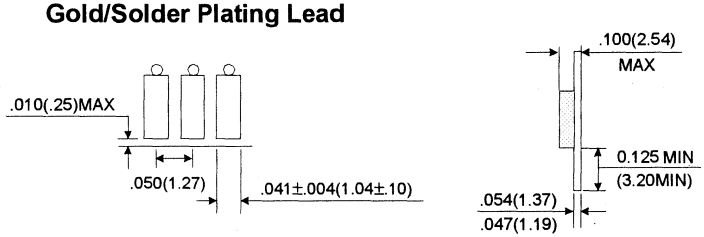


(Front view)



(Back view)

Gold/Solder Plating Lead



Tolerances :±.005(.13) unless otherwise specified

NOTE : The used device is 4Mx16 DRAM, TSOPII
DRAM Part No. : KMM5324004BSW/BSWG -- KM416C4104BS (400 mil)

KMM5364003BSW/BSWG Fast Page Mode

4M x 36 DRAM SIMM Using 4Mx16 & Quad $\overline{CAS}$ 4Mx4, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM5364003B is a 4Mx36bits Dynamic RAM high density memory module. The Samsung KMM5364003B consists of two CMOS 4Mx16bits and one CMOS Quad $\overline{CAS}$ 4Mx4bits DRAMs in TSOP packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM5364003B is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns

FEATURES

- Part Identification
  - KMM5364003BSW(4K cycles/64ms Ref, TSOP, Solder)
  - KMM5364003BSWG(4K cycles/64ms Ref, TSOP, Gold)
- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ & Hidden Refresh capability
- $\overline{RAS}$-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1000mil), single sided component

2

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	$\overline{Vss}$
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	RAS0
9	DQ21	45	NC
10	Vcc	46	$\overline{NC}$
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	$\overline{NC}$	69	PD3
34	$\overline{RAS2}$	70	PD4
35	DQ26	71	NC
36	DQ8	72	Vss

PIN NAMES

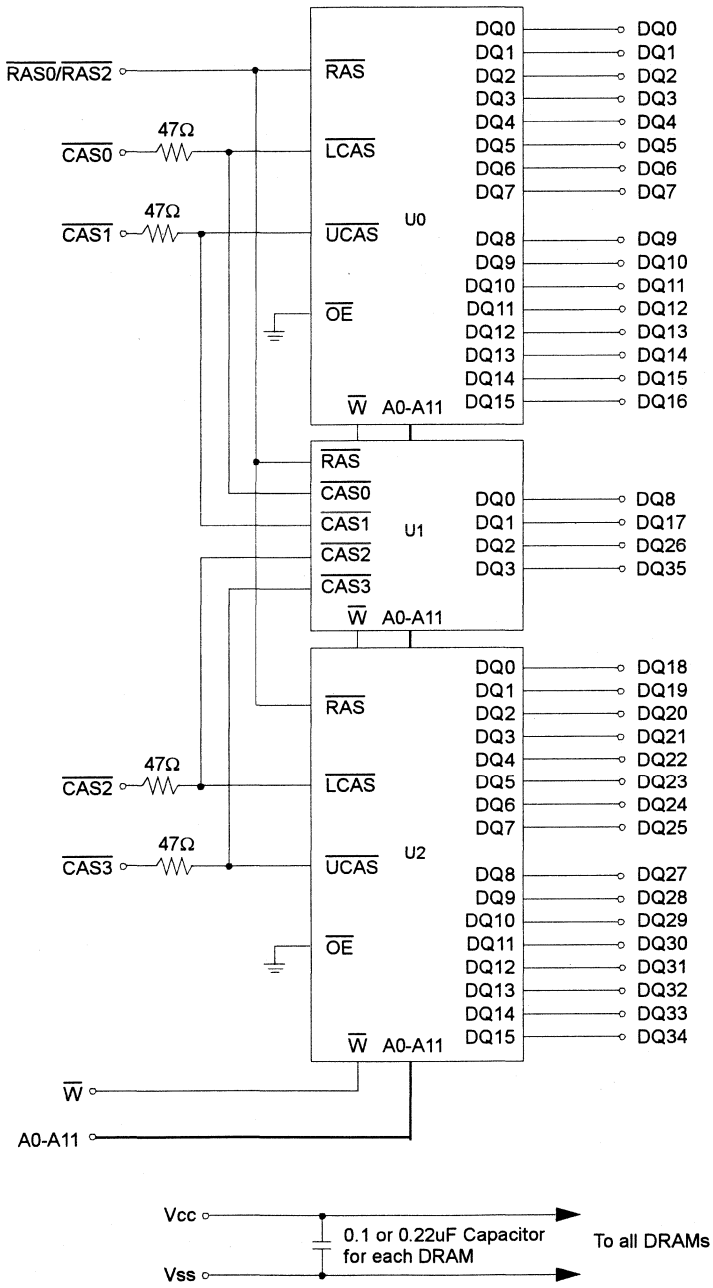
Pin Name	Function
A0 - A11	Address Inputs
DQ0 - 35	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	Vss	Vss
PD2	NC	NC
PD3	Vss	NC
PD4	Vss	NC

SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	3	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : V_{CC}+2.0V at pulse width≤20ns, which is measured at V_{CC}.

*2 : -2.0V at pulse width≤20ns, which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM5364003BSW/BSWG		Unit
		Min	Max	
I_{CC1}	-5	-	330	mA
	-6	-	300	mA
I_{CC2}	Don't care	-	6	mA
I_{CC3}	-5	-	330	mA
	-6	-	300	mA
I_{CC4}	-5	-	220	mA
	-6	-	190	mA
I_{CC5}	Don't care	-	3	mA
I_{CC6}	-5	-	330	mA
	-6	-	300	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	25	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	31	pF
Input capacitance[$\overline{RAS0}$/$\overline{RAS2}$]	C_{IN3}	-	31	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	24	pF
Input/Output capacitance[DQ0 - 35]	C_{DQ}	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.6/0.8V, V_{oh}/V_{ol}=2.4/0.4V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns	6
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	10		10		ns	9
Refresh period	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35	ns	3

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.6/0.8V$, $V_{oh}/V_{ol}=2.4/0.4V$, output loading CL=100pF

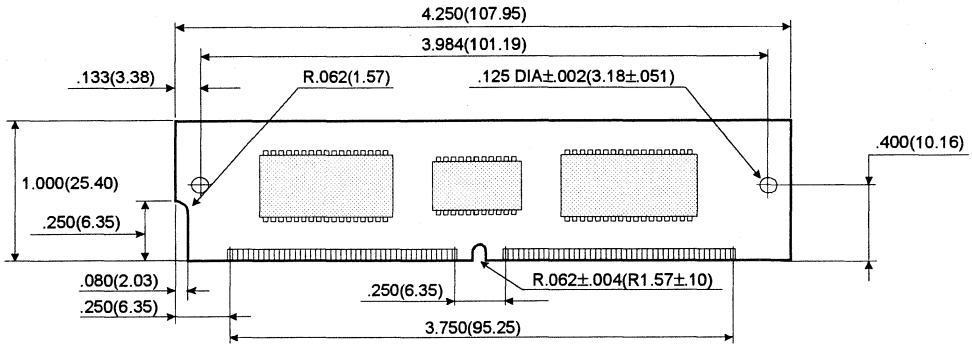
Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	35		40		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	

NOTES

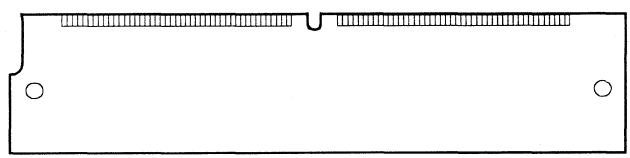
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

PACKAGE DIMENSIONS

Units : Inches (millimeters)

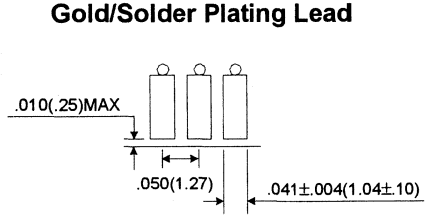


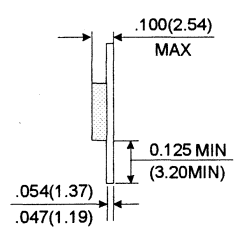
(Front view)



(Back view)

Gold/Solder Plating Lead





Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 4Mx16 & Quad $\overline{CAS}$ 4Mx4 DRAM, TSOPII

DRAM Part No. : KMM5364003BSW/BSWG -- KM416C4100BS & KM44C4003CS(300 mil)

KMM5364005BSW/BSWG EDO Mode

4M x 36 DRAM SIMM Using 4Mx16 & Quad $\overline{CAS}$ 4Mx4, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM5364005B is a 4Mx36bits Dynamic RAM high density memory module. The Samsung KMM5364005B consists of two CMOS 4Mx16bits and one CMOS Quad $\overline{CAS}$ 4Mx4bits DRAMs in TSOP packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM5364005B is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

FEATURES

- Part Identification
  - KMM5364005BSW(4K cycles/64ms Ref, TSOP, Solder)
  - KMM5364005BSWG(4K cycles/64ms Ref, TSOP, Gold)
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ & Hidden Refresh capability
- $\overline{RAS}$-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1000mil), single sided component

2

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	$\overline{Vss}$
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	RAS0
9	DQ21	45	NC
10	Vcc	46	$\overline{NC}$
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	$\overline{NC}$	69	PD3
34	$\overline{RAS2}$	70	PD4
35	DQ26	71	NC
36	DQ8	72	Vss

PIN NAMES

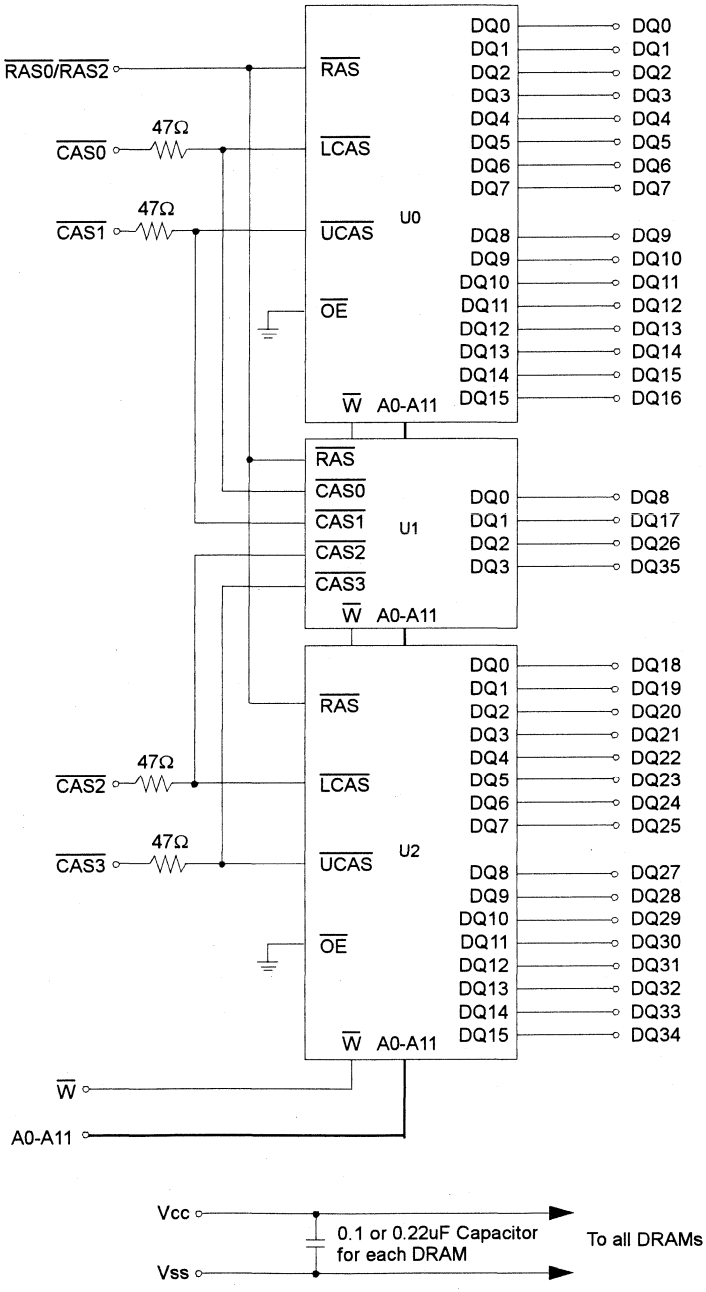
Pin Name	Function
A0 - A11	Address Inputs
DQ0 - 35	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	Vss	Vss
PD2	NC	NC
PD3	Vss	NC
PD4	Vss	NC

SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	3	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤ 20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM5364005BSW/BSWG		Unit
		Min	Max	
I_{CC1}	-5	-	330	mA
	-6	-	300	mA
I_{CC2}	Don't care	-	6	mA
I_{CC3}	-5	-	330	mA
	-6	-	300	mA
I_{CC4}	-5	-	260	mA
	-6	-	230	mA
I_{CC5}	Don't care	-	3	mA
I_{CC6}	-5	-	330	mA
	-6	-	300	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Hyper Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	25	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	31	pF
Input capacitance[$\overline{RAS0}$/$\overline{RAS2}$]	C_{IN3}	-	31	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	24	pF
Input/Output capacitance[DQ0 - 35]	C_{DQ}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, Vcc=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.6/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	6,12
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		45		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	4
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	8		10		ns	9
Refresh period	t_{REF}		64		64	ms	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, V_{CC} = 5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.6/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Hyper page mode cycle time	t_{HPC}	20		25		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	6,12
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	6
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{W}$ pulse width	t_{WPE}	5		5		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit and is not referenced for V_{OH} or V_{OL}

7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

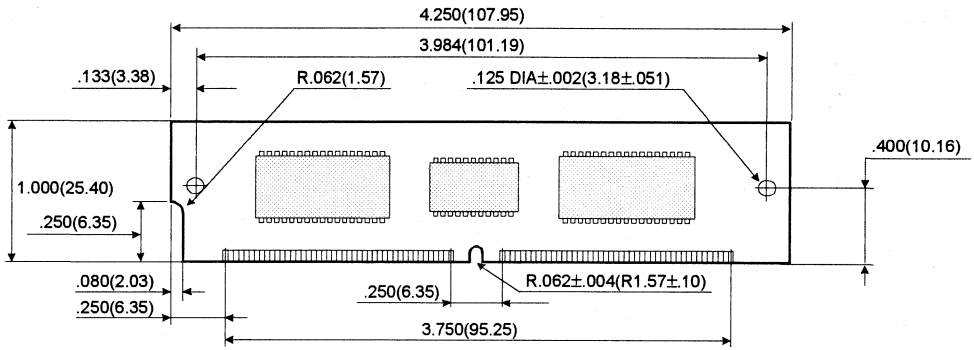
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit access time is controlled by t_{AA}.

11. $t_{ASC} \geq 6$ns, Assume tT=2.0ns.

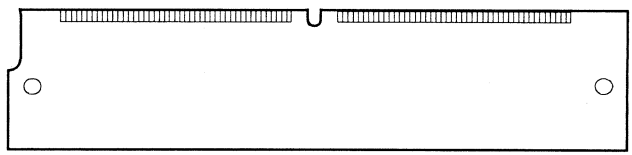
12. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

PACKAGE DIMENSIONS

Units : Inches (millimeters)

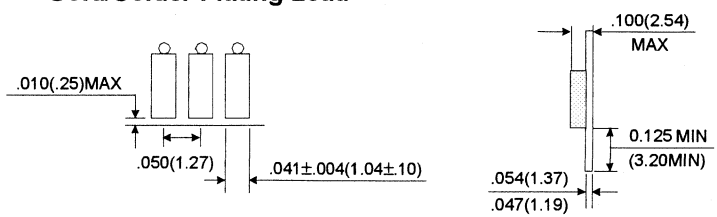


(Front view)



(Back view)

Gold/Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 4Mx16 & Quad $\overline{CAS}$ 4Mx4 DRAM, TSOPII
DRAM Part No. : KMM5364005BSW/BSWG -- KM416C4104BS & KM44C4005CS(300 mil)

KMM5328000BSW/BSWG Fast Page Mode
8M x 32 DRAM SIMM Using 4Mx16, 4K Refresh, 5V

GENERAL DESCRIPTION
The Samsung KMM5328000B is a 8Mx32bits Dynamic RAM high density memory module. The Samsung KMM5328000B consists of four CMOS 4Mx16bits DRAMs in TSOP packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM5328000B is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns

FEATURES
- Part Identification
  - KMM5328000BSW(4K cycles/64ms Ref, TSOP, Solder)
  - KMM5328000BSWG(4K cycles/64ms Ref, TSOP, Gold)
- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ & Hidden Refresh capability
- $\overline{RAS}$-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1000mil), double sided component

2

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	NC
2	DQ0	38	NC
3	DQ18	39	$\overline{Vss}$
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	$\overline{RAS1}$
10	Vcc	46	$\overline{NC}$
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	$\overline{A9}$	68	PD2
33	$\overline{RAS3}$	69	PD3
34	$\overline{RAS2}$	70	PD4
35	NC	71	NC
36	NC	72	Vss

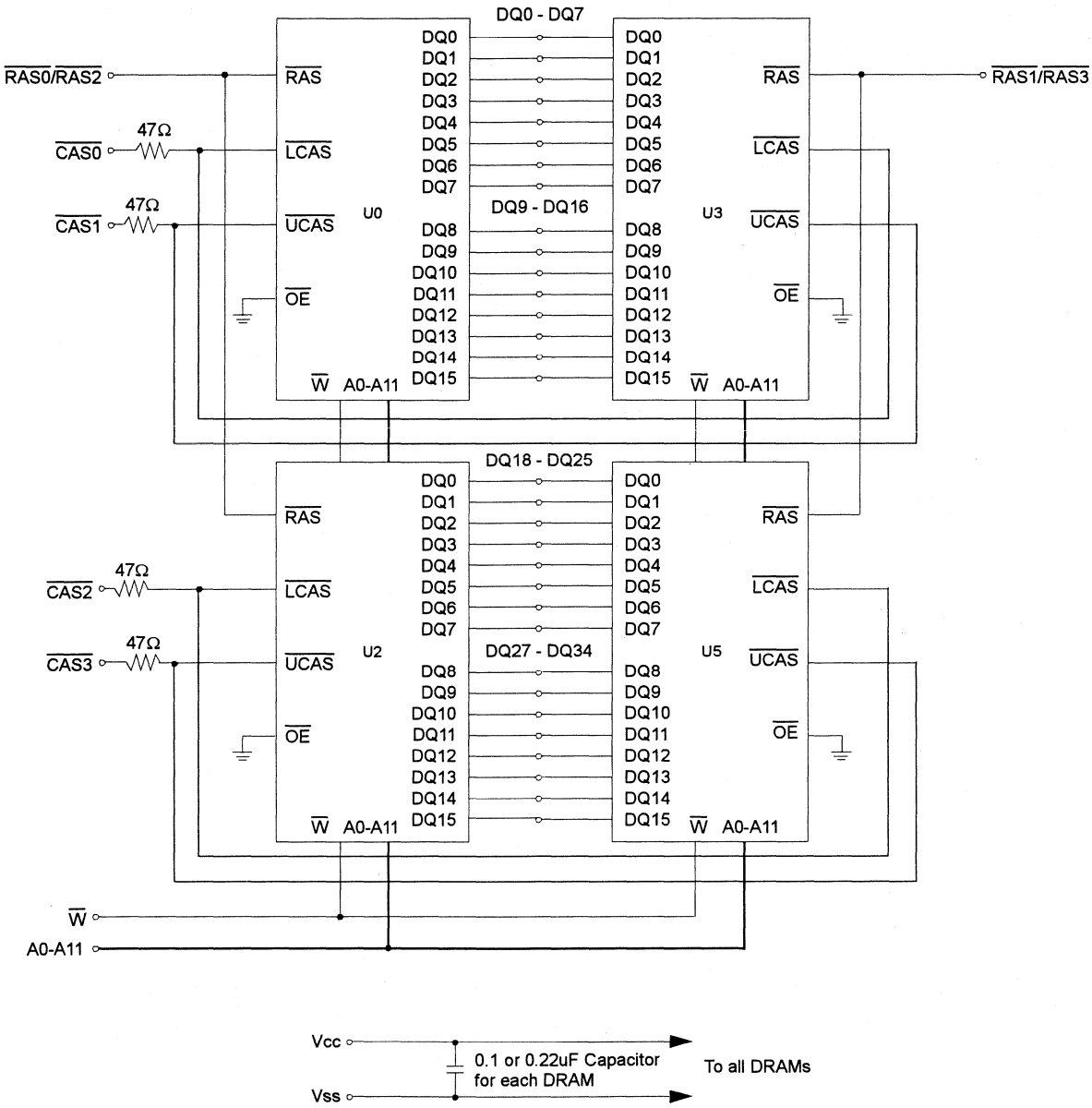
PIN NAMES

Pin Name	Function
A0 - A11	Address Inputs
DQ0-7, DQ9-16 DQ18-25, DQ27-34	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	NC	NC
PD2	Vss	Vss
PD3	Vss	NC
PD4	Vss	NC

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	4	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width ≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM5328000BSW/BSWG		Unit
		Min	Max	
I_{CC1}	-5	-	244	mA
	-6	-	224	mA
I_{CC2}	Don't care	-	8	mA
I_{CC3}	-5	-	244	mA
	-6	-	224	mA
I_{CC4}	-5	-	144	mA
	-6	-	124	mA
I_{CC5}	Don't care	-	4	mA
I_{CC6}	-5	-	244	mA
	-6	-	224	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-10	10	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	30	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	38	pF
Input capacitance[$\overline{RAS0}$/$\overline{RAS2}$, $\overline{RAS1}$/$\overline{RAS3}$]	C_{IN3}	-	24	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	24	pF
Input/Output capacitance[DQ0-7, 9-16,18-25, 27-34]	C_{DQ}	-	24	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.6/0.8V, V_{oh}/V_{ol}=2.4/0.4V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns	6
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	10		10		ns	9
Refresh period	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35	ns	3

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.6/0.8V$, $V_{oh}/V_{ol}=2.4/0.4V$, output loading CL=100pF

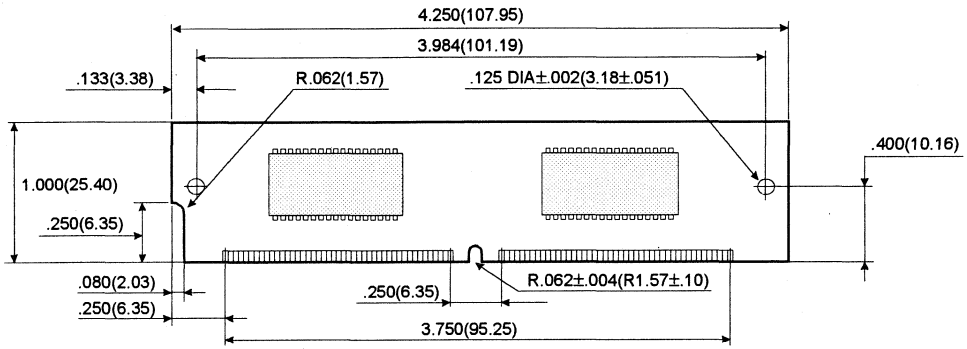
Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	35		40		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	

NOTES

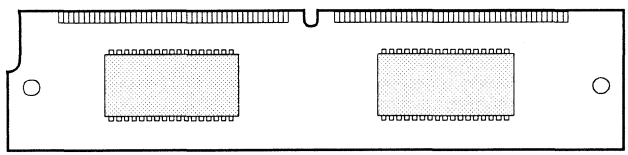
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

PACKAGE DIMENSIONS

Units : Inches (millimeters)

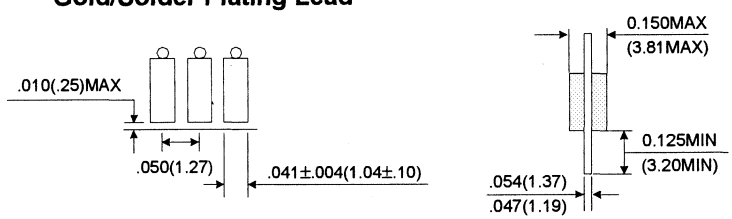


(Front view)



(Back view)

Gold/Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 4Mx16 DRAM, TSOPII
DRAM Part No. : KMM5328000BSW/BSWG -- KM416C4100BS

KMM5328004BSW/BSWG EDO Mode

8M x 32 DRAM SIMM Using 4Mx16, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM5328004B is a 8Mx32bits Dynamic RAM high density memory module. The Samsung KMM5328004B consists of four CMOS 4Mx16bits DRAMs in TSOP packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM5328004B is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

FEATURES

- Part Identification
  - KMM5328004BSW(4K cycles/64ms Ref, TSOP, Solder)
  - KMM5328004BSWG(4K cycles/64ms Ref, TSOP, Gold)
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ & Hidden Refresh capability
- $\overline{RAS}$-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1000mil), double sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	NC
2	DQ0	38	NC
3	DQ18	39	$\overline{Vss}$
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	$\overline{RAS1}$
10	Vcc	46	$\overline{NC}$
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	$\overline{A9}$	68	PD2
33	$\overline{RAS3}$	69	PD3
34	$\overline{RAS2}$	70	PD4
35	NC	71	NC
36	NC	72	Vss

PIN NAMES

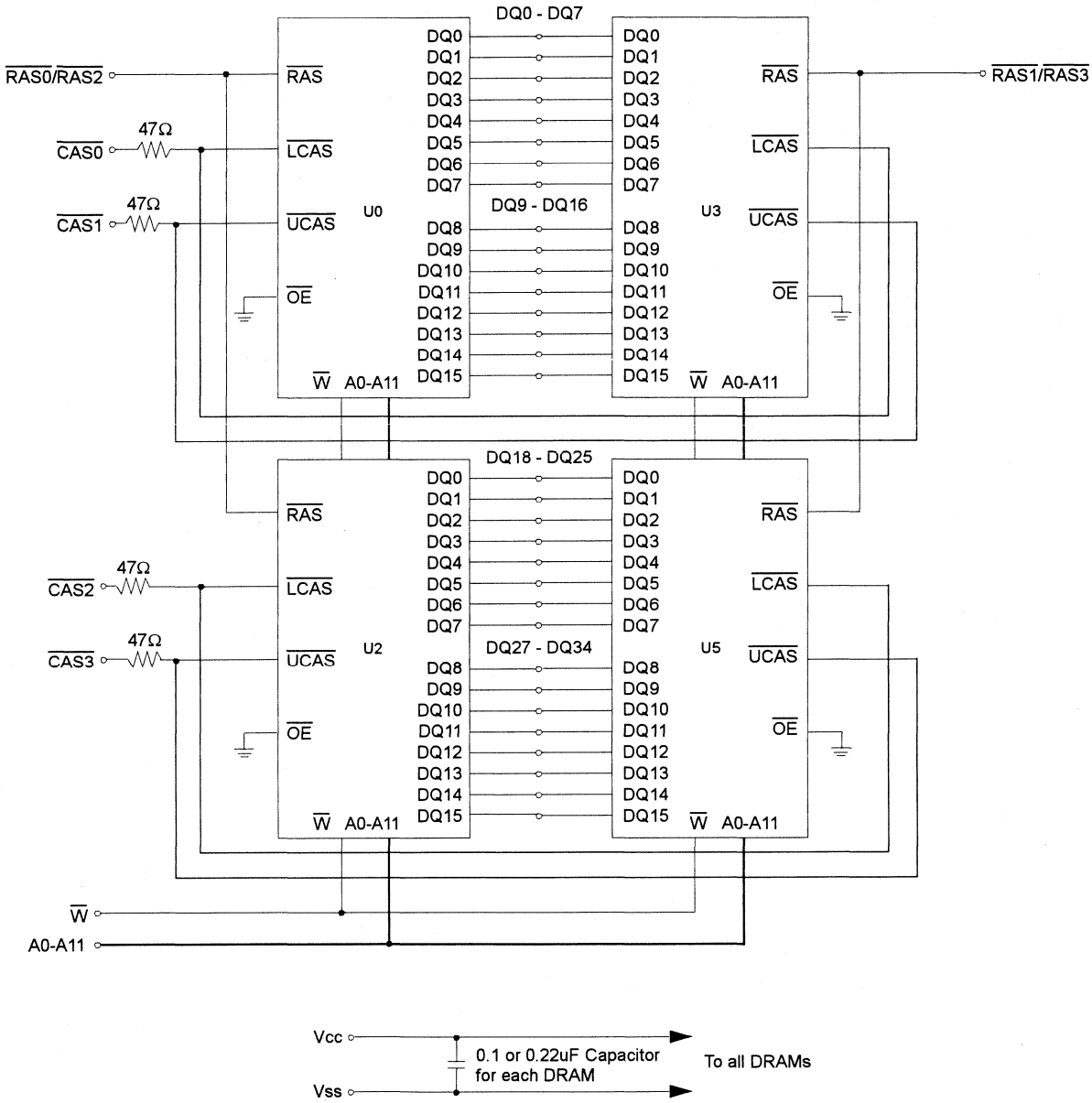
Pin Name	Function
A0 - A11	Address Inputs
DQ0-7, DQ9-16 DQ18-25, DQ27-34	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	NC	NC
PD2	Vss	Vss
PD3	Vss	NC
PD4	Vss	NC

SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	4	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM5328004BSW/BSWG		Unit
		Min	Max	
I_{CC1}	-5	-	244	mA
	-6	-	224	mA
I_{CC2}	Don't care	-	8	mA
I_{CC3}	-5	-	244	mA
	-6	-	224	mA
I_{CC4}	-5	-	224	mA
	-6	-	204	mA
I_{CC5}	Don't care	-	4	mA
I_{CC6}	-5	-	244	mA
	-6	-	224	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-10	10	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} :Hyper Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	30	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	38	pF
Input capacitance[$\overline{RAS0}$/$\overline{RAS2}$, $\overline{RAS1}$/$\overline{RAS3}$]	C_{IN3}	-	24	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	24	pF
Input/Output capacitance[DQ0-7, 9-16,18-25, 27-34]	C_{DQ}	-	24	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.6/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	6,12
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		45		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	4
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	8		10		ns	9
Refresh period	t_{REF}		64		64	ms	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3

AC CHARACTERISTICS (0°C≤TA≤70°C, Vcc=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.6/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Hyper page mode cycle time	t_{HPC}	20		25		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	6,12
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	6
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{W}$ pulse width	t_{WPE}	5		5		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit and is not referenced for V_{OH} or V_{OL}.

7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

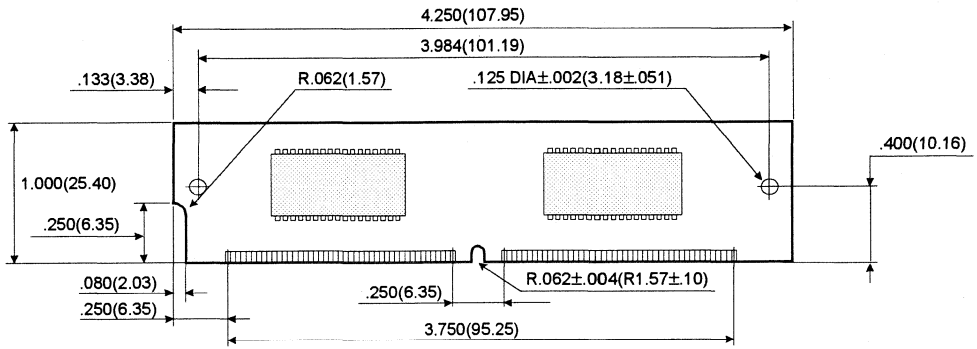
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit access time is controlled by t_{AA}.

11. $t_{ASC} \geq 6$ns, Assume t_T=2.0ns.

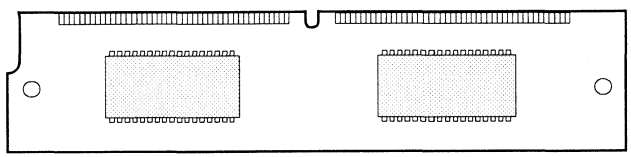
12. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

PACKAGE DIMENSIONS

Units : Inches (millimeters)

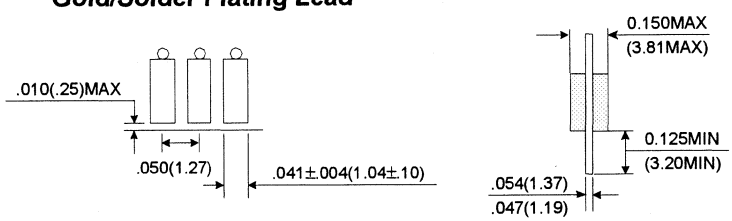


(Front view)



(Back view)

Gold/Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 4Mx16 DRAM, TSOPII
DRAM Part No. : KMM5328004BSW/BSWG -- KM416C4104BS (400 mil)

KMM5368003BSW/BSWG Fast Page Mode

8M x 36 DRAM SIMM Using 4Mx16 & Quad CAS 4Mx4, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM5368003B is a 8Mx36bits Dynamic RAM high density memory module. The Samsung KMM5368003B consists of four CMOS 4Mx16bits and two CMOS Quad CAS 4Mx4bits DRAMs in TSOP packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM5368003B is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PERFORMANCE RANGE

Speed	tRAC	tCAC	tRC	tPC
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns

FEATURES

- Part Identification
  - KMM5368003BSW(4K cycles/64ms Ref, TSOP, Solder)
  - KMM5368003BSWG(4K cycles/64ms Ref, TSOP, Gold)
- Fast Page Mode Operation
- CAS-before-RAS & Hidden Refresh capability
- RAS-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1000mil), double sided component

2

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	Vss
4	DQ1	40	CAS0
5	DQ19	41	CAS2
6	DQ2	42	CAS3
7	DQ20	43	CAS1
8	DQ3	44	RAS0
9	DQ21	45	RAS1
10	Vcc	46	NC
11	NC	47	W
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	RAS3	69	PD3
34	RAS2	70	PD4
35	DQ26	71	NC
36	DQ8	72	Vss

PIN NAMES

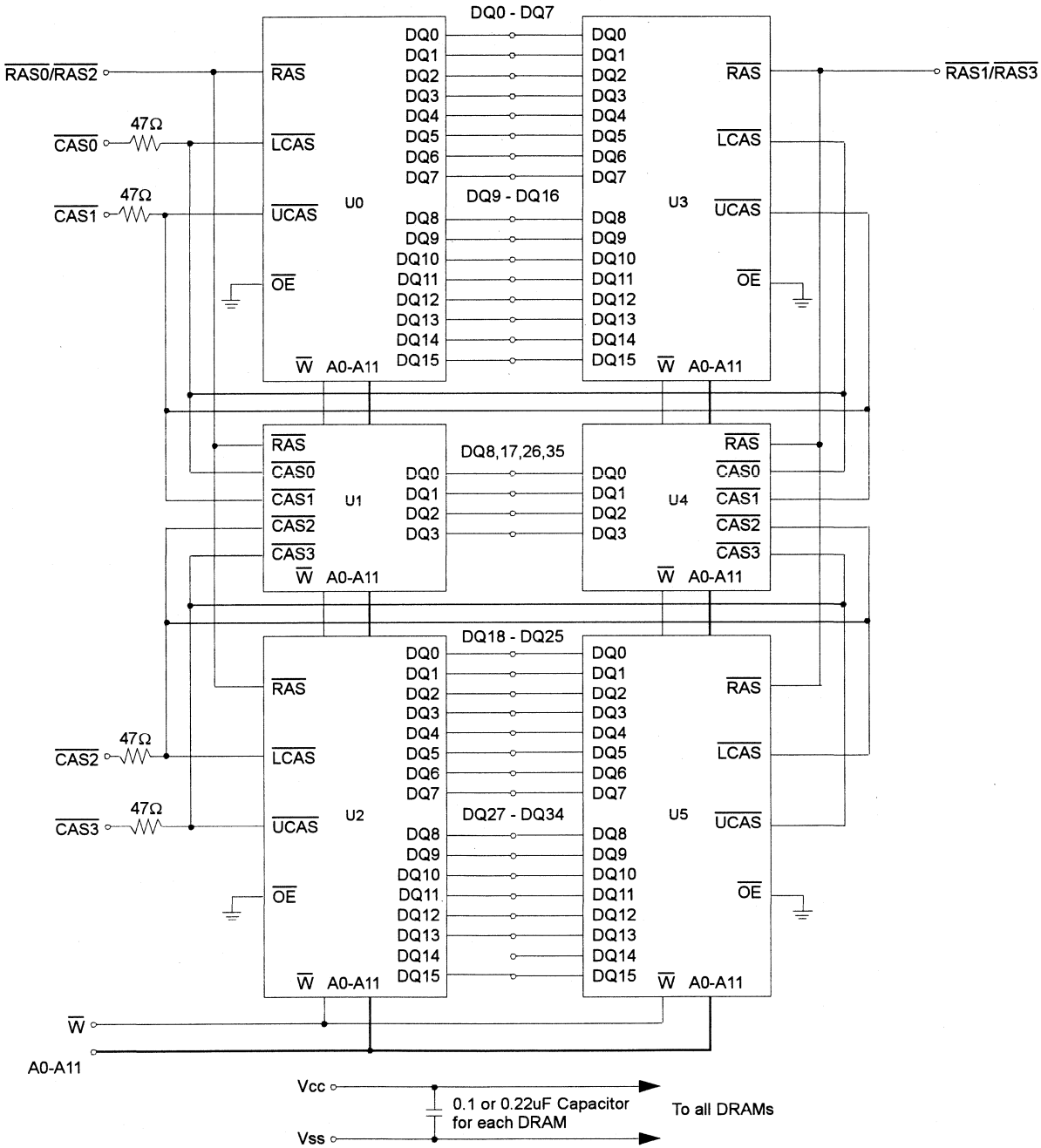
Pin Name	Function
A0 - A11	Address Inputs
DQ0 - 35	Data In/Out
W	Read/Write Enable
RAS0 - RAS3	Row Address Strobe
CAS0 - CAS3	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	NC	NC
PD2	Vss	Vss
PD3	Vss	NC
PD4	Vss	NC

SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	6	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM5368003BSW/BSWG		Unit
		Min	Max	
I_{CC1}	-5 -6	- -	336 306	mA mA
I_{CC2}	Don't care	-	12	mA
I_{CC3}	-5 -6	- -	336 306	mA mA
I_{CC4}	-5 -6	- -	226 196	mA mA
I_{CC5}	Don't care	-	6	mA
I_{CC6}	-5 -6	- -	336 306	mA mA
$I_{I(L)}$ $I_{O(L)}$	Don't care	-10 -10	10 10	uA uA
V_{OH} V_{OL}	Don't care	2.4 -	- 0.4	V V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	40	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	52	pF
Input capacitance[$\overline{RAS0}$/$\overline{RAS2}$, $\overline{RAS1}$/$\overline{RAS3}$]	C_{IN3}	-	31	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	24	pF
Input/Output capacitance[DQ0 - 35]	C_{DQ}	-	24	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.6/0.8V, V_{oh}/V_{ol}=2.4/0.4V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns	6
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	10		10		ns	9
Refresh period	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35	ns	3

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.6/0.8V$, $V_{oh}/V_{ol}=2.4/0.4V$, output loading CL=100pF

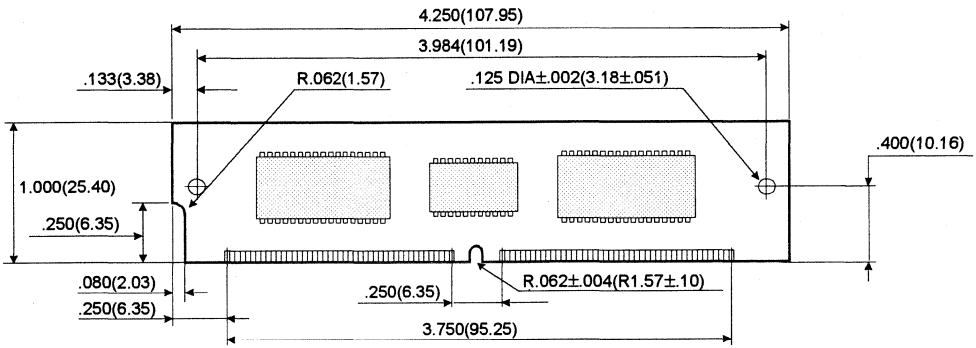
Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	35		40		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	

NOTES

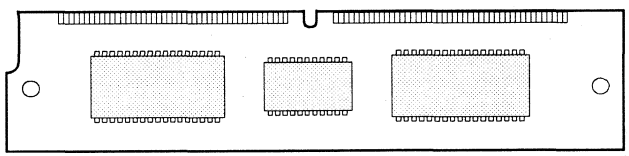
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

PACKAGE DIMENSIONS

Units : Inches (millimeters)

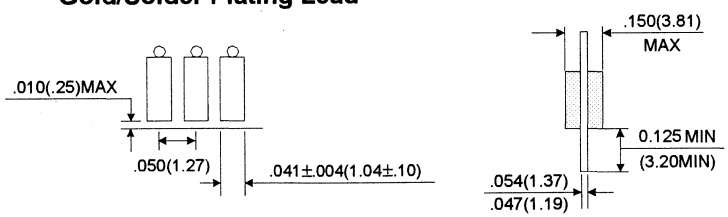


(Front view)



(Back view)

Gold/Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 4Mx16 & Quad $\overline{CAS}$ 4Mx4 DRAM, TSOPII
DRAM Part No. : KMM5368003BSW/BSWG -- KM416C4100BS & KM44C4003CS(300 mil)

KMM5368005BSW/BSWG EDO Mode

8M x 36 DRAM SIMM Using 4Mx16 & Quad $\overline{CAS}$ 4Mx4, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM5368005B is a 8Mx36bits Dynamic RAM high density memory module. The Samsung KMM5368005B consists of four CMOS 4Mx16bits and two CMOS Quad $\overline{CAS}$ 4Mx4bits DRAMs in TSOP packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM5368005B is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

FEATURES

- Part Identification
  - KMM5368005BSW(4K cycles/64ms Ref, TSOP, Solder)
  - KMM5368005BSWG(4K cycles/64ms Ref, TSOP, Gold)
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ & Hidden Refresh capability
- $\overline{RAS}$-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1000mil), double sided component

2

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	$\overline{Vss}$
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	$\overline{RAS1}$
10	Vcc	46	$\overline{NC}$
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	$\overline{A9}$	68	PD2
33	$\overline{RAS3}$	69	PD3
34	$\overline{RAS2}$	70	PD4
35	DQ26	71	NC
36	DQ8	72	Vss

PIN NAMES

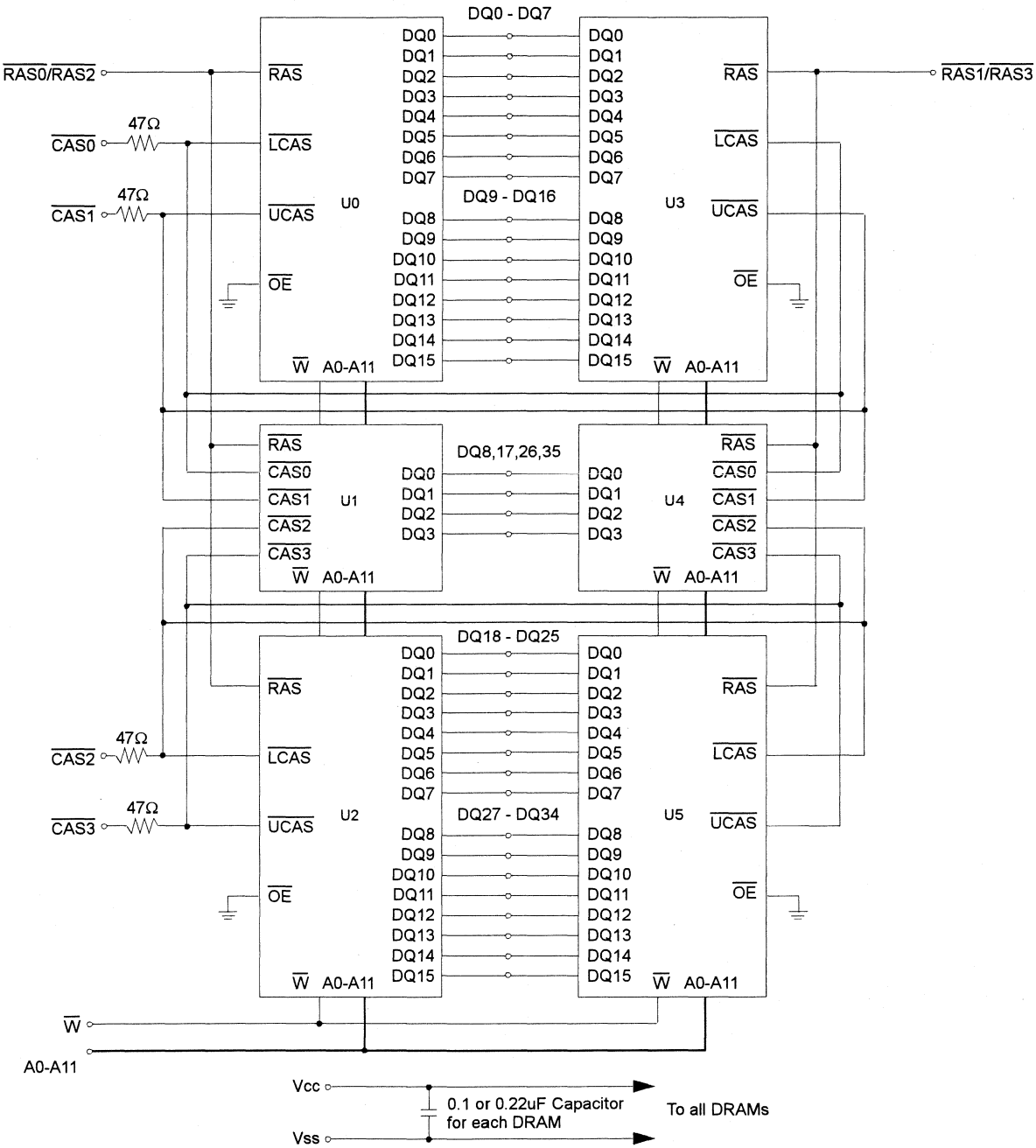
Pin Name	Function
A0 - A11	Address Inputs
DQ0 - 35	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	NC	NC
PD2	Vss	Vss
PD3	Vss	Vss
PD4	Vss	NC

SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	6	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM5368005BSW/BSWG		Unit
		Min	Max	
I_{CC1}	-5	-	336	mA
	-6	-	306	mA
I_{CC2}	Don't care	-	12	mA
I_{CC3}	-5	-	336	mA
	-6	-	306	mA
I_{CC4}	-5	-	306	mA
	-6	-	276	mA
I_{CC5}	Don't care	-	6	mA
I_{CC6}	-5	-	336	mA
	-6	-	306	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-10	10	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Hyper Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	40	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	52	pF
Input capacitance[$\overline{RAS0}$/$\overline{RAS2}$, $\overline{RAS1}$/$\overline{RAS3}$]	C_{IN3}	-	31	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	24	pF
Input/Output capacitance[DQ0 - 35]	C_{DQ}	-	24	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, Vcc=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.6/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	6,12
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		45		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	4
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	8		10		ns	9
Refresh period	t_{REF}		64		64	ms	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.6/0.8V$, $V_{oh}/V_{ol}=2.0/0.8V$, output loading CL=100pF

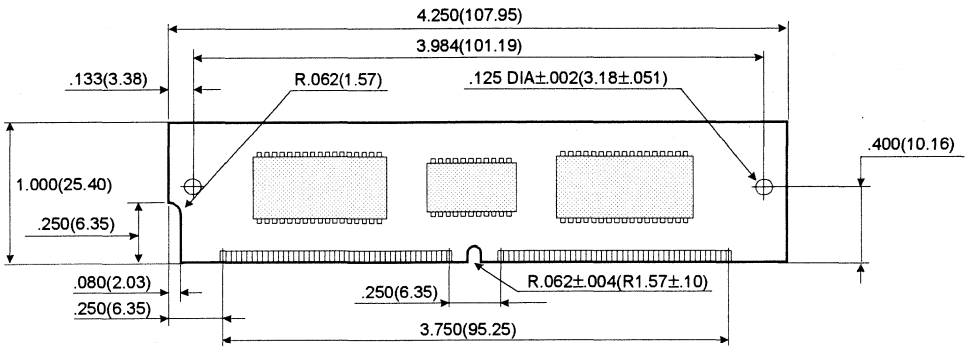
Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Hyper page mode cycle time	t_{HPC}	20		25		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	6,12
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	6
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{W}$ pulse width	t_{WPE}	5		5		ns	

NOTES

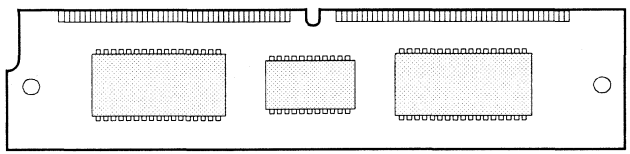
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit and is not referenced for V_{OH} or V_{OL}.
7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit access time is controlled by t_{AA}.
11. $t_{ASC} \geq 6ns$, Assume tT=2.0ns.
12. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

PACKAGE DIMENSIONS

Units : Inches (millimeters)

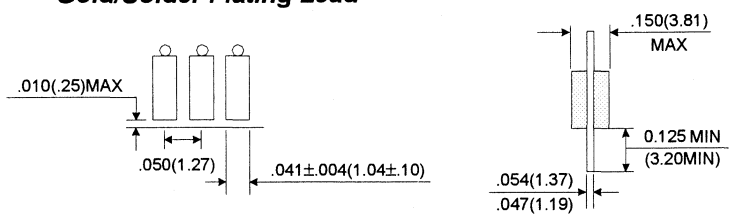


(Front view)



(Back view)

Gold/Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 4Mx16 & Quad $\overline{CAS}$ 4Mx4 DRAM, TSOPII
DRAM Part No. : KMM5368005BSW/BSWG -- KM416C4104BS & KM44C4005CS(300 mil)

KMM53216000BK/BKG Fast Page Mode
16M x 32 DRAM SIMM Using 16Mx4, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM53216000B is a 16Mx32bits Dynamic RAM high density memory module. The Samsung KMM53216000B consists of eight CMOS 16Mx4bits DRAMs in SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM53216000B is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

FEATURES

- Part Identification
  - KMM53216000BK(4K cycles/64ms Ref, SOJ, Solder)
  - KMM53216000BKG(4K cycles/64ms Ref, SOJ, Gold)
- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ & Hidden Refresh capability
- $\overline{RAS}$-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1250mil), double sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	NC
2	DQ0	38	NC
3	DQ18	39	$\overline{Vss}$
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	NC
10	Vcc	46	$\overline{NC}$
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	$\overline{NC}$	69	PD3
34	$\overline{RAS2}$	70	PD4
35	NC	71	NC
36	NC	72	Vss

PIN NAMES

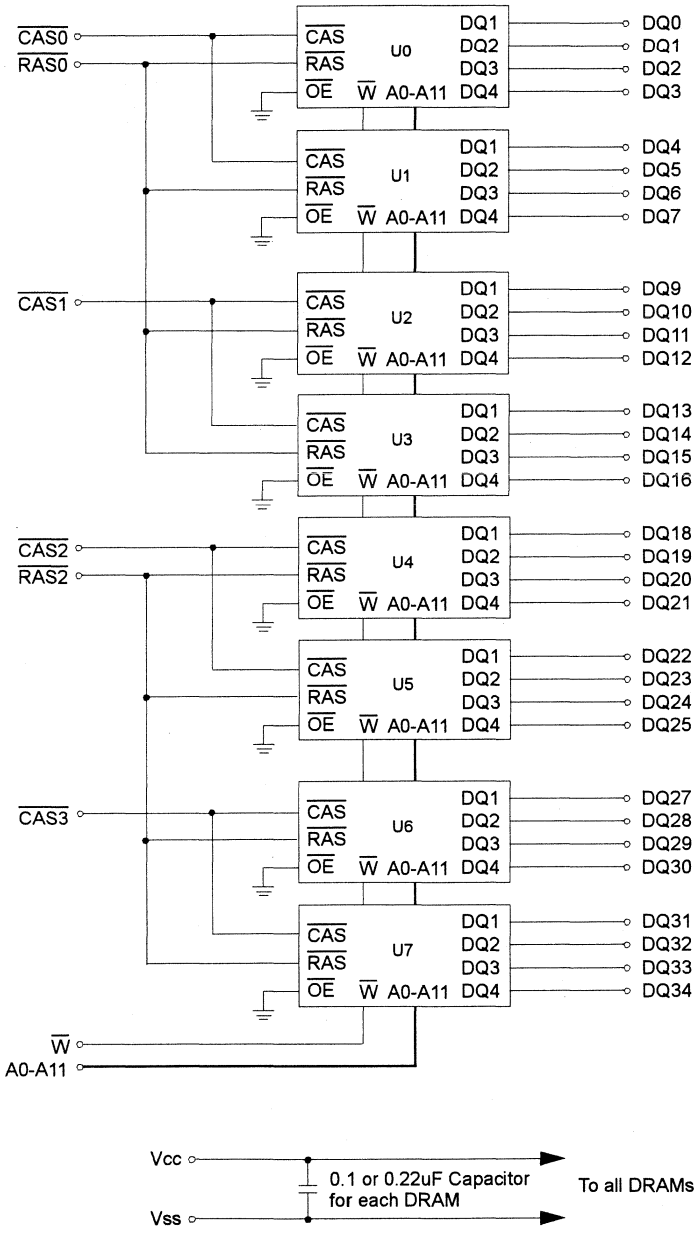
Pin Name	Function
A0 - A11	Address Inputs
DQ0-7, DQ9-16 DQ18-25, DQ27-34	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	Vss	Vss
PD2	NC	NC
PD3	Vss	NC
PD4	Vss	NC

SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width ≤ 20ns, which is measured at Vcc.

*2 : -2.0V at pulse width ≤ 20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM53216000BK/BKG		Unit
		Min	Max	
I_{CC1}	-5	-	960	mA
	-6	-	880	mA
I_{CC2}	Don't care	-	16	mA
I_{CC3}	-5	-	960	mA
	-6	-	880	mA
I_{CC4}	-5	-	560	mA
	-6	-	480	mA
I_{CC5}	Don't care	-	8	mA
I_{CC6}	-5	-	960	mA
	-6	-	880	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	50	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	66	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	38	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	24	pF
Input/Output capacitance[DQ0-7, 9-16,18-25, 27-34]	C_{DQ}	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns	6
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	10		10		ns	9
Refresh period	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35	ns	3

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.4/0.8V$, $V_{oh}/V_{ol}=2.4/0.4V$, output loading CL=100pF

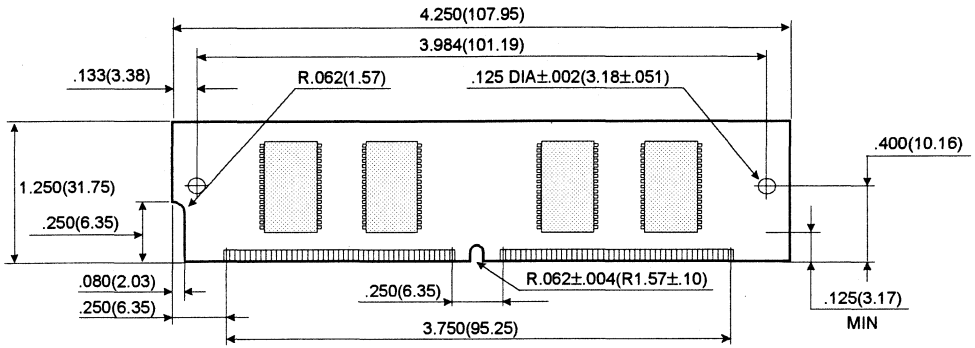
Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	35		40		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	

NOTES

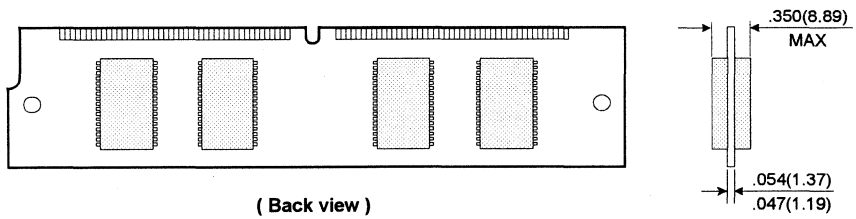
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

PACKAGE DIMENSIONS

Units : Inches (millimeters)

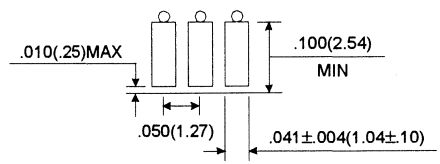


(Front view)



(Back view)

Gold/Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 16Mx4 DRAM, SOJ
DRAM Part No. : KMM53216000BK/BKG -- KM44C16100BK

KMM53216004BK/BKG EDO Mode

16M x 32 DRAM SIMM Using 16Mx4, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM53216004B is a 16Mx32bits Dynamic RAM high density memory module. The Samsung KMM53216004B consists of eight CMOS 16Mx4bits DRAMs in SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM53216004B is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

FEATURES

- Part Identification
  - KMM53216004BK(4K cycles/64ms Ref, SOJ, Solder)
  - KMM53216004BKG(4K cycles/64ms Ref, SOJ, Gold)
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ & Hidden Refresh capability
- $\overline{RAS}$-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1250mil), double sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	NC
2	DQ0	38	NC
3	DQ18	39	$\overline{Vss}$
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	NC
10	Vcc	46	$\overline{NC}$
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	$\overline{NC}$	69	PD3
34	$\overline{RAS2}$	70	PD4
35	NC	71	NC
36	NC	72	Vss

PIN NAMES

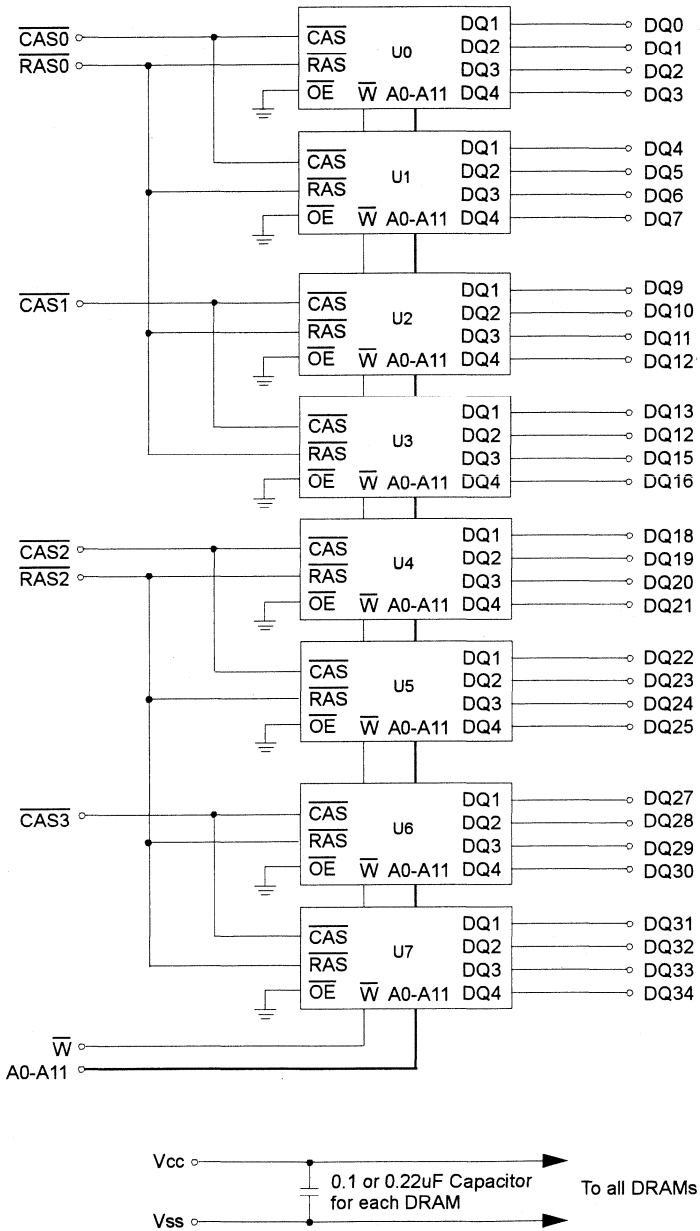
Pin Name	Function
A0 - A11	Address Inputs
DQ0-7, DQ9-16 DQ18-25, DQ27-34	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	Vss	Vss
PD2	NC	NC
PD3	Vss	NC
PD4	Vss	NC

SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM53216004BK/BKG		Unit
		Min	Max	
I_{CC1}	-5	-	960	mA
	-6	-	880	mA
I_{CC2}	Don't care	-	16	mA
I_{CC3}	-5	-	960	mA
	-6	-	880	mA
I_{CC4}	-5	-	880	mA
	-6	-	800	mA
I_{CC5}	Don't care	-	8	mA
I_{CC6}	-5	-	960	mA
	-6	-	880	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Hyper Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	50	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	66	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	38	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	24	pF
Input/Output capacitance[DQ0-7, 9-16,18-25, 27-34]	C_{DQ}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	6,12
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		45		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	4
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	8		10		ns	9
Refresh period	t_{REF}		64		64	ms	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.4/0.8V$, $V_{oh}/V_{ol}=2.0/0.8V$, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Hyper page mode cycle time	t_{HPC}	20		25		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	6,12
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	6
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{W}$ pulse width	t_{WPE}	5		5		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit and is not referenced for V_{OH} or V_{OL}.

7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

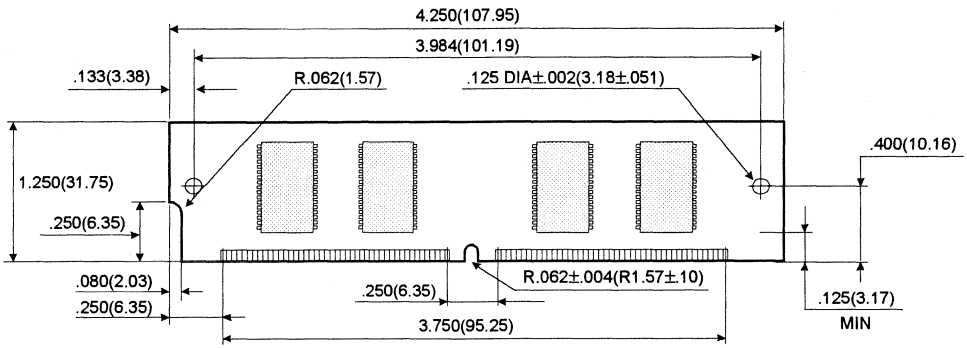
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit access time is controlled by t_{AA}.

11. $t_{ASC} \geq 6ns$, Assume $t_T=2.0ns$.

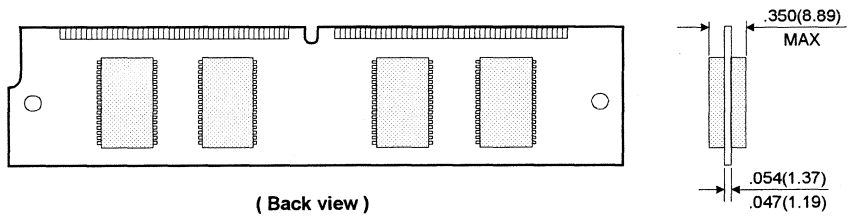
12. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

PACKAGE DIMENSIONS

Units : Inches (millimeters)

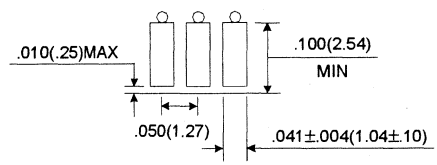


(Front view)



(Back view)

Gold/Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 16Mx4 DRAM, SOJ
DRAM Part No. : KMM53216004BK/BKG -- KM44C16104BK

KMM53216000BV/BVG Fast Page Mode
16M x 32 DRAM SIMM Using 16Mx4, 4K Refresh, 5V

GENERAL DESCRIPTION
The Samsung KMM53216000B is a 16Mx32bits Dynamic RAM high density memory module. The Samsung KMM53216000B consists of eight CMOS 16Mx4bits DRAMs in SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM53216000B is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

FEATURES
- Part Identification
  - KMM53216000BV(4K cycles/64ms Ref, SOJ, Solder)
  - KMM53216000BVG(4K cycles/64ms Ref, SOJ, Gold)
- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ & Hidden Refresh capability
- $\overline{RAS}$-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1000mil), single sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	NC
2	DQ0	38	NC
3	DQ18	39	$\overline{Vss}$
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	NC
10	Vcc	46	$\overline{NC}$
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	$\overline{NC}$	69	PD3
34	$\overline{RAS2}$	70	PD4
35	NC	71	NC
36	NC	72	Vss

PIN NAMES

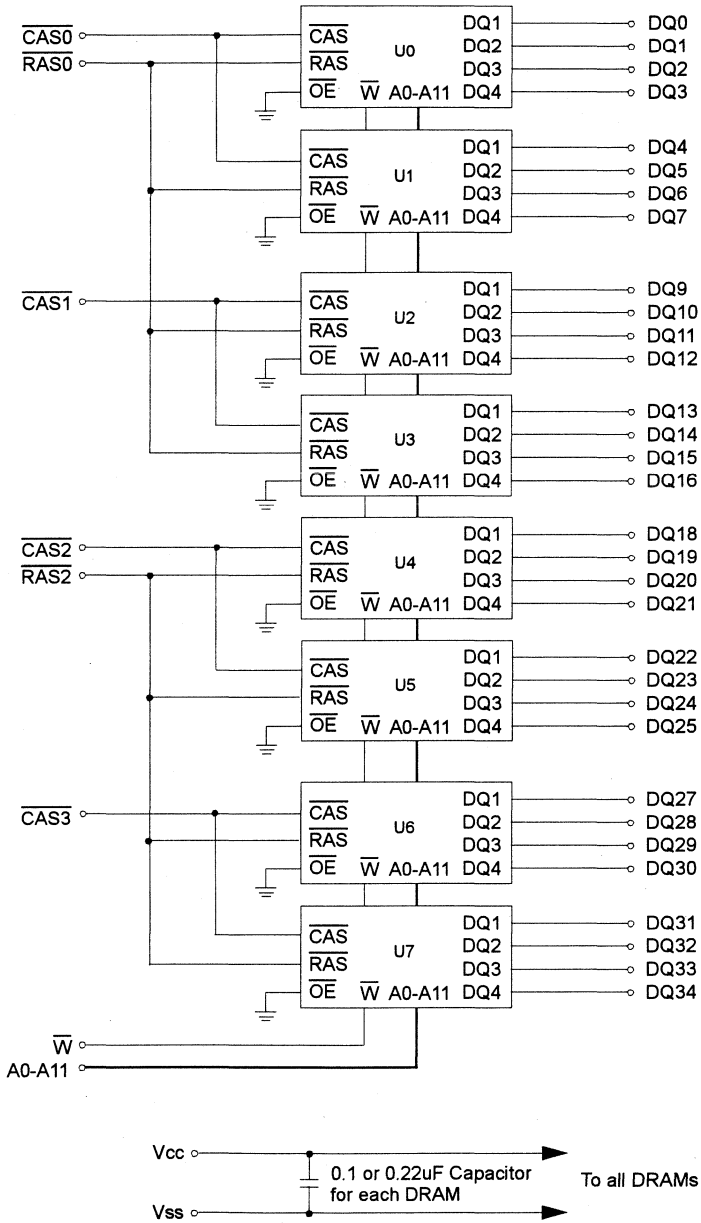
Pin Name	Function
A0 - A11	Address Inputs
DQ0-7, DQ9-16 DQ18-25, DQ27-34	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	Vss	Vss
PD2	NC	NC
PD3	Vss	NC
PD4	Vss	NC

SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width ≤ 20ns, which is measured at Vcc.

*2 : -2.0V at pulse width ≤ 20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM53216000BV/BVG		Unit
		Min	Max	
I_{CC1}	-5	-	960	mA
	-6	-	880	mA
I_{CC2}	Don't care	-	16	mA
I_{CC3}	-5	-	960	mA
	-6	-	880	mA
I_{CC4}	-5	-	560	mA
	-6	-	480	mA
I_{CC5}	Don't care	-	8	mA
I_{CC6}	-5	-	960	mA
	-6	-	880	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	50	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	66	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	38	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	24	pF
Input/Output capacitance[DQ0-7, 9-16,18-25, 27-34]	C_{DQ}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns	6
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	10		10		ns	9
Refresh period	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35	ns	3

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.4/0.8V$, $V_{oh}/V_{ol}=2.4/0.4V$, output loading CL=100pF

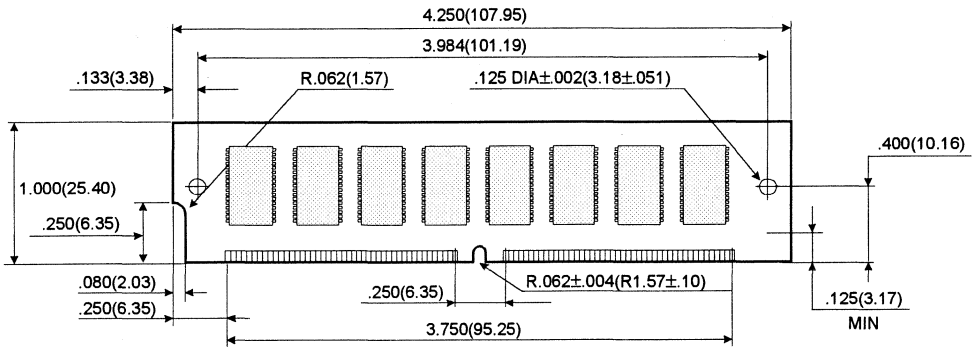
Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	35		40		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	

NOTES

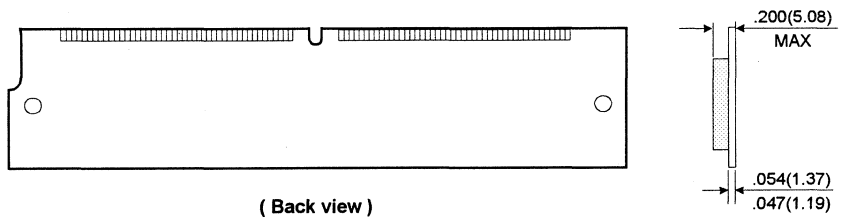
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

PACKAGE DIMENSIONS

Units : Inches (millimeters)

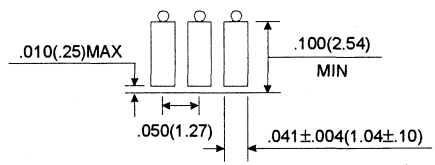


(Front view)



(Back view)

Gold/Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 16Mx4 DRAM, SOJ
DRAM Part No. : KMM53216000BV/BVG -- KM44C16100BK

KMM53216004BV/BVG EDO Mode

16M x 32 DRAM SIMM Using 16Mx4, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM53216004B is a 16Mx32bits Dynamic RAM high density memory module. The Samsung KMM53216004B consists of eight CMOS 16Mx4bits DRAMs in SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM53216004B is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

FEATURES

- Part Identification
  - KMM53216004BV(4K cycles/64ms Ref, SOJ, Solder)
  - KMM53216004BVG(4K cycles/64ms Ref, SOJ, Gold)
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ & Hidden Refresh capability
- $\overline{RAS}$-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1000mil), single sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	NC
2	DQ0	38	NC
3	DQ18	39	$\overline{Vss}$
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	NC
10	Vcc	46	$\overline{NC}$
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	$\overline{NC}$	69	PD3
34	$\overline{RAS2}$	70	PD4
35	NC	71	NC
36	NC	72	Vss

PIN NAMES

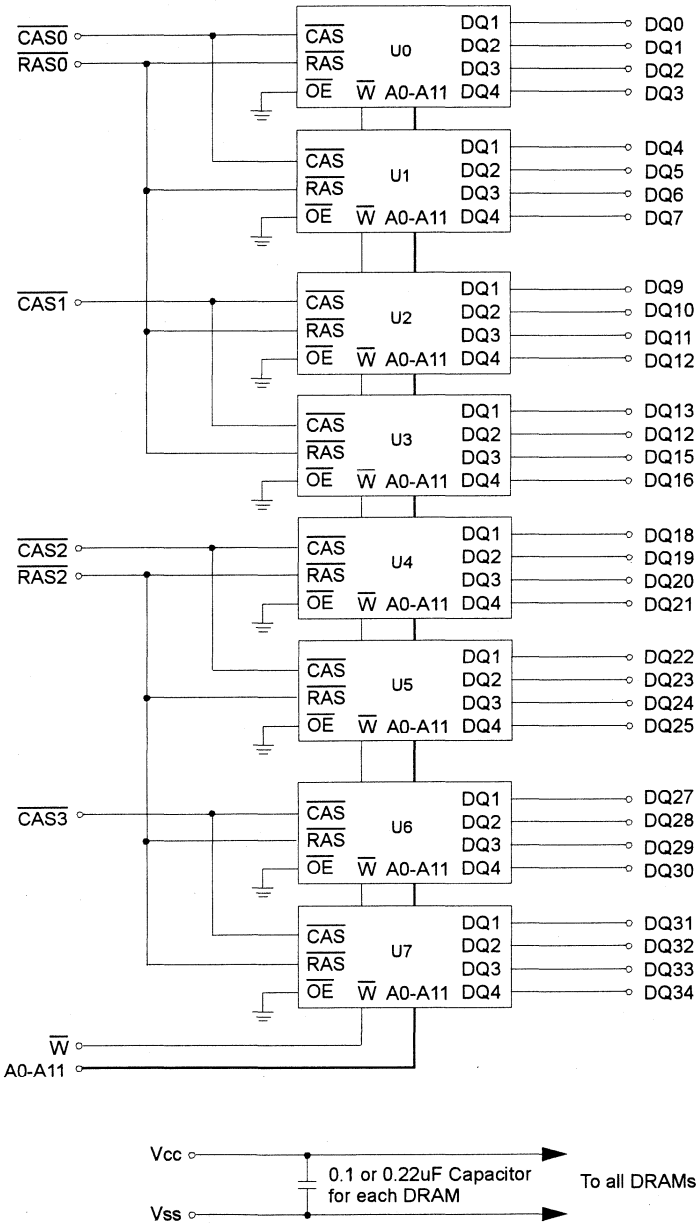
Pin Name	Function
A0 - A11	Address Inputs
DQ0-7, DQ9-16 DQ18-25, DQ27-34	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	Vss	Vss
PD2	NC	NC
PD3	Vss	NC
PD4	Vss	NC

SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM53216004BV/BVG		Unit
		Min	Max	
I_{CC1}	-5	-	960	mA
	-6	-	880	mA
I_{CC2}	Don't care	-	16	mA
I_{CC3}	-5	-	960	mA
	-6	-	880	mA
I_{CC4}	-5	-	880	mA
	-6	-	800	mA
I_{CC5}	Don't care	-	8	mA
I_{CC6}	-5		960	mA
	-6	-	880	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Hyper Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	50	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	66	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	38	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	24	pF
Input/Output capacitance[DQ0-7, 9-16,18-25, 27-34]	C_{DQ}	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	6,12
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		45		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	4
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	8		10		ns	9
Refresh period	t_{REF}		64		64	ms	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.4/0.8V$, $V_{oh}/V_{ol}=2.0/0.8V$, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3
Hyper page mode cycle time	t_{HPC}	20		25		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	6,12
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	6
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{W}$ pulse width	t_{WPE}	5		5		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit and is not referenced for V_{OH} or V_{OL}.

7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

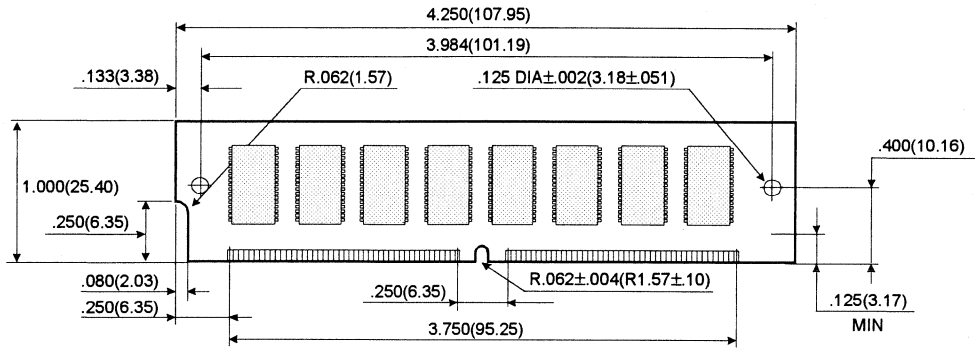
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit access time is controlled by t_{AA}.

11. $t_{ASC} \geq 6ns$, Assume $t_T=2.0ns$.

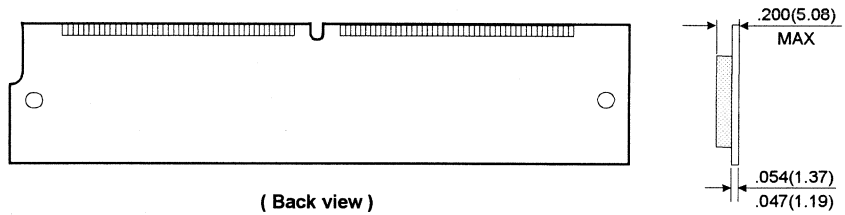
12. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

PACKAGE DIMENSIONS

Units : Inches (millimeters)

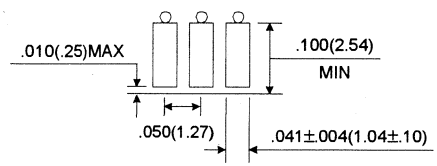


(Front view)



(Back view)

Gold/Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 16Mx4 DRAM, SOJ
DRAM Part No. : KMM53216004BV/BVG-- KM44C16104BK

KMM53616000BK/BKG Fast Page Mode

16M x 36 DRAM SIMM Using 16Mx4 & 16Mx1, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM53616000B is a 16Mx36bits Dynamic RAM high density memory module. The Samsung KMM53616000B consists of eight CMOS 16Mx4bits DRAMs and four CMOS 16Mx1bit DRAMs in SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM53616000B is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

FEATURES

- Part Identification
  - KMM53616000BK(4K cycles/64ms Ref, SOJ, Solder)
  - KMM53616000BKG(4K cycles/64ms Ref, SOJ, Gold)
- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ & Hidden Refresh capability
- $\overline{RAS}$-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1250mil), double sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	$\overline{Vss}$
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	NC
10	Vcc	46	$\overline{NC}$
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	$\overline{NC}$	69	PD3
34	$\overline{RAS2}$	70	PD4
35	DQ26	71	NC
36	DQ8	72	Vss

PIN NAMES

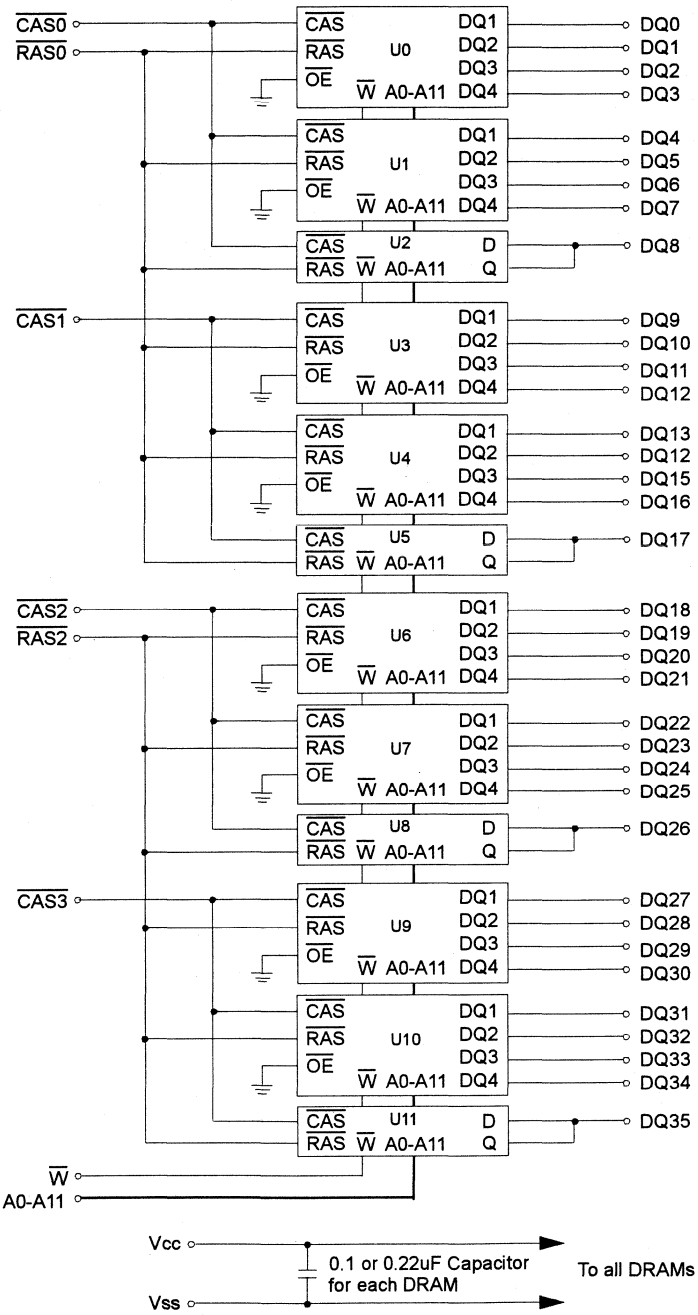
Pin Name	Function
A0 - A11	Address Inputs
DQ0 - DQ35	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	Vss	Vss
PD2	NC	NC
PD3	Vss	NC
PD4	Vss	NC

SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	12	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤ 20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤ 20ns, whcih is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM53616000BK/BKG		Unit
		Min	Max	
I_{CC1}	-5	-	1320	mA
	-6	-	1200	mA
I_{CC2}	Don't care	-	24	mA
I_{CC3}	-5	-	1320	mA
	-6	-	1200	mA
I_{CC4}	-5	-	880	mA
	-6	-	760	mA
I_{CC5}	Don't care	-	12	mA
I_{CC6}	-5	-	1320	mA
	-6	-	1200	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time,t_{PC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	70	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	94	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	52	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	31	pF
Input/Output capacitance[DQ0-35]	C_{DQ}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns	6
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	10		10		ns	9
Refresh period	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35	ns	3

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.4/0.8V$, $V_{oh}/V_{ol}=2.4/0.4V$, output loading CL=100pF

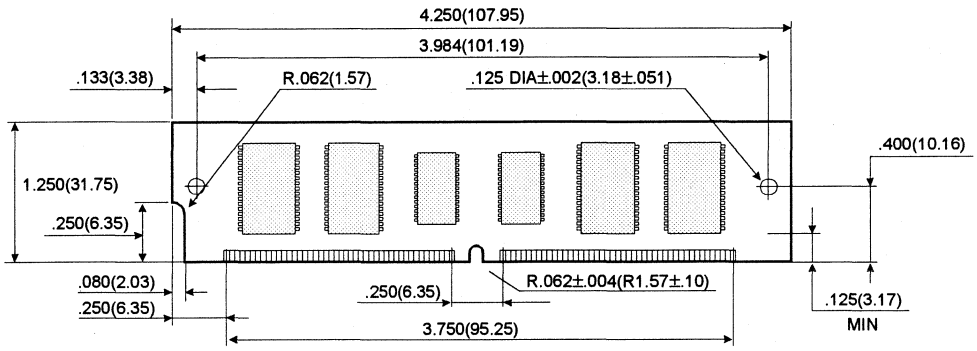
Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	35		40		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	

NOTES

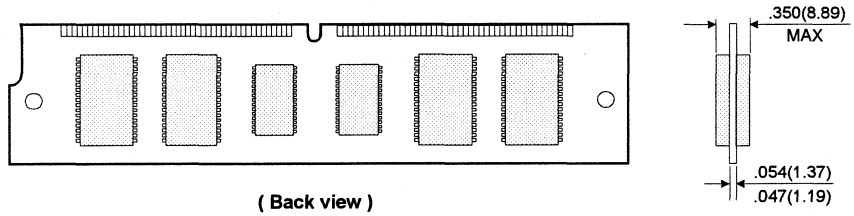
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

PACKAGE DIMENSIONS

Units : Inches (millimeters)

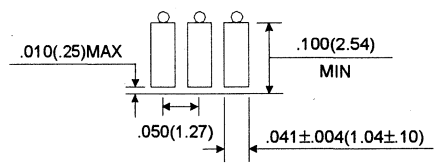


(Front view)



(Back view)

Gold/Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 16Mx4 DRAM & 16Mx1 DRAM, SOJ
DRAM Part No. : KMM53616000BK/BKG -- KM44C16100BK
KM41C16000CK

KMM53616004BK/BKG EDO Mode

16M x 36 DRAM SIMM Using 16Mx4 & 16Mx1, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM53616004B is a 16Mx36bits Dynamic RAM high density memory module. The Samsung KMM53616004B consists of eight CMOS 16Mx4bits DRAMs and four CMOS 16Mx1bit DRAMs in SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM53616004B is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

FEATURES

- Part Identification
  - KMM53616004BK(4K cycles/64ms Ref, SOJ, Solder)
  - KMM53616004BKG(4K cycles/64ms Ref, SOJ, Gold)
- Hyper Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ & Hidden Refresh capability
- $\overline{RAS}$-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1250mil), double sided component

2

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	$\overline{Vss}$
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	NC
10	Vcc	46	$\overline{NC}$
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	$\overline{NC}$	69	PD3
34	$\overline{RAS2}$	70	PD4
35	DQ26	71	NC
36	DQ8	72	Vss

PIN NAMES

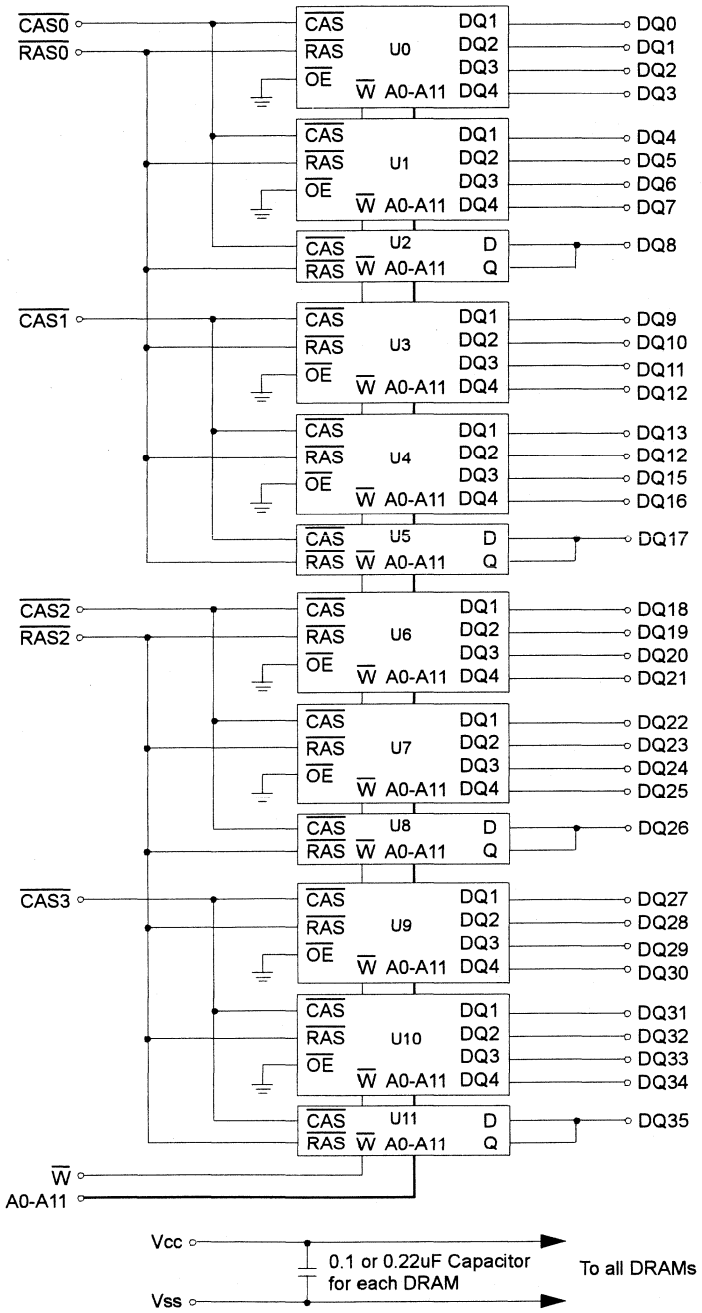
Pin Name	Function
A0 - A11	Address Inputs
DQ0 - DQ35	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	Vss	Vss
PD2	NC	NC
PD3	Vss	NC
PD4	Vss	NC

SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	12	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, whcih is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM53616004BK/BKG		Unit
		Min	Max	
I_{CC1}	-5	-	1320	mA
	-6	-	1200	mA
I_{CC2}	Don't care	-	24	mA
I_{CC3}	-5	-	1320	mA
	-6	-	1200	mA
I_{CC4}	-5	-	1200	mA
	-6	-	1080	mA
I_{CC5}	Don't care	-	12	mA
I_{CC6}	-5	-	1320	mA
	-6	-	1200	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Hyper Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	70	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	94	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	52	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	31	pF
Input/Output capacitance[DQ0-35]	C_{DQ}	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.4V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	6,12
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		45		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	4
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	8		10		ns	9
Refresh period	t_{REF}		64		64	ms	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3

AC CHARACTERISTICS (0°C≤TA≤70°C, Vcc=5.0V±10%. See notes 1,2.)

Test condition : Vih/Vil=2.4/0.8V, Voh/Vol=2.0/0.8V, output loading CL=100pF

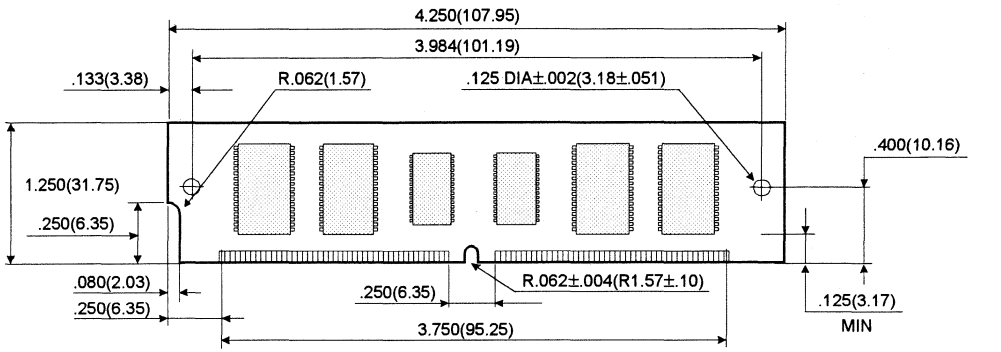
Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Hyper page mode cycle time	t_{HPC}	20		25		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	6,12
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	6
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{W}$ pulse width	t_{WPE}	5		5		ns	

NOTES

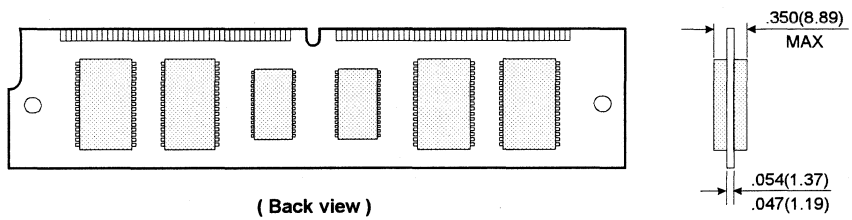
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are Vih/Vil. VIH(min) and VIL(max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥tRCD(max).
6. This parameter defines the time at which theoutput achieves the open circuit and is not referenced for VOH or VOL
7. tWCS is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If tWCS≥tWCS(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as reference point only. If tRAD is greater than the specified tRAD(max) limit access time is controlled by tAA.
11. tASC≥6ns, Assume tT=2.0ns.
12. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

PACKAGE DIMENSIONS

Units : Inches (millimeters)

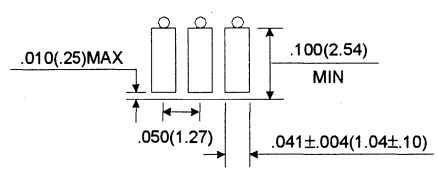


(Front view)



(Back view)

Gold/Solder Plating Lead



Tolerances :±.005(.13) unless otherwise specified

NOTE : The used device is 16Mx4 DRAM & 16Mx1 DRAM, SOJ
DRAM Part No. : KMM53616004BK/BKG -- KM44C16104BK
KM41C16004CK

KMM53232000BK/BKG Fast Page Mode
32M x 32 DRAM SIMM Using 16Mx4, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM53232000B is a 32Mx32bits Dynamic RAM high density memory module. The Samsung KMM53232000B consists of sixteen CMOS 16Mx4bits DRAMs in SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM53232000B is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns

FEATURES

- Part Identification
  - KMM53232000BK(4K cycles/64ms Ref, SOJ, Solder)
  - KMM53232000BKG(4K cycles/64ms Ref, SOJ, Gold)
- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ & Hidden Refresh capability
- $\overline{RAS}$-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1420mil), double sided component

2

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	NC
2	DQ0	38	NC
3	DQ18	39	$\overline{Vss}$
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	$\overline{RAS1}$
10	Vcc	46	$\overline{NC}$
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	$\overline{A9}$	68	PD2
33	$\overline{RAS3}$	69	PD3
34	$\overline{RAS2}$	70	PD4
35	NC	71	NC
36	NC	72	Vss

PIN NAMES

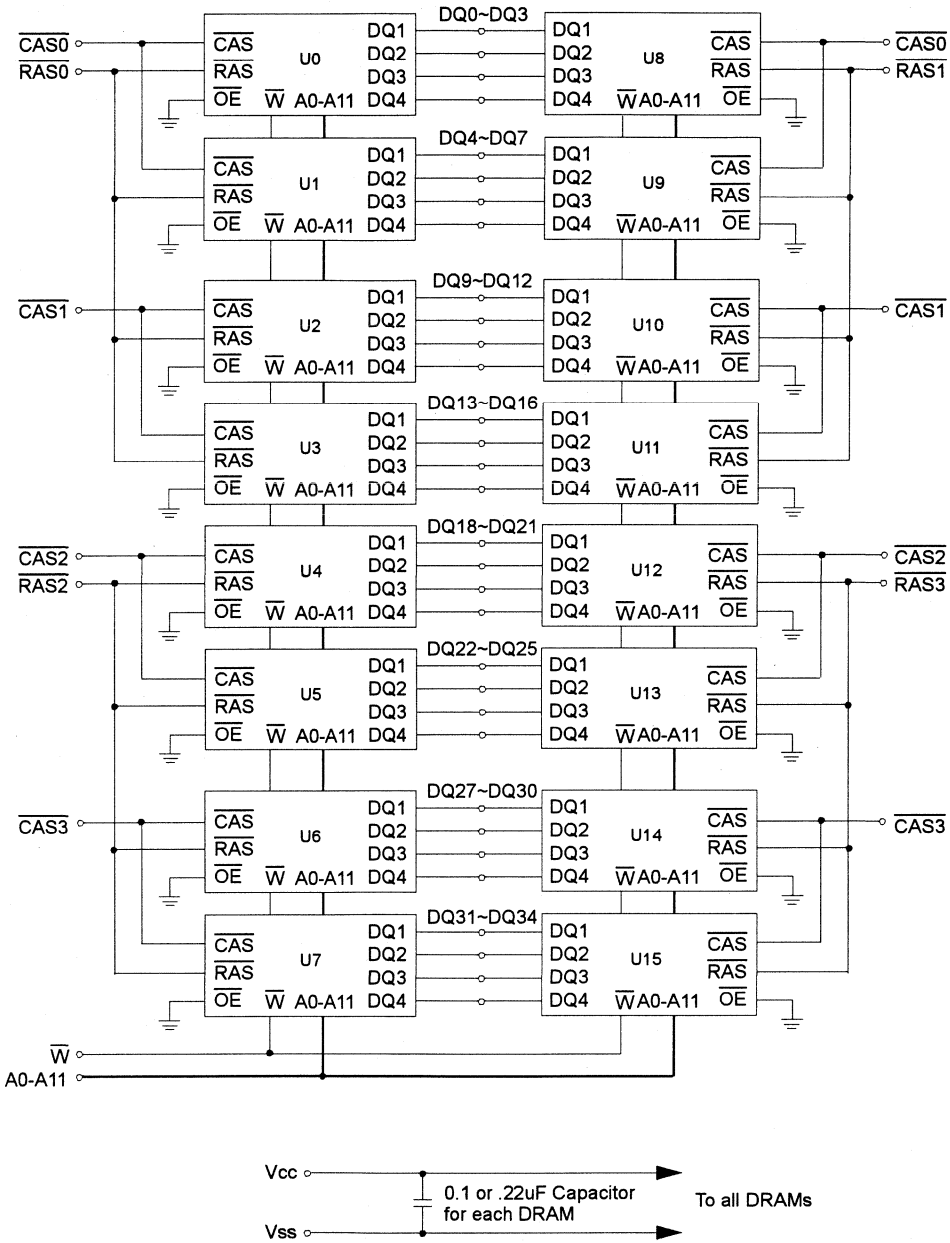
Pin Name	Function
A0 - A11	Address Inputs
DQ0-7, DQ9-16 DQ18-25, DQ27-34	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	NC	NC
PD2	Vss	Vss
PD3	Vss	NC
PD4	Vss	NC

SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	16	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width ≤ 20ns, which is measured at Vcc.

*2 : -2.0V at pulse width ≤ 20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM53232000BK/BKG		Unit
		Min	Max	
I_{CC1}	-5	-	976	mA
	-6	-	896	mA
I_{CC2}	Don't care	-	32	mA
I_{CC3}	-5	-	976	mA
	-6	-	896	mA
I_{CC4}	-5	-	576	mA
	-6	-	496	mA
I_{CC5}	Don't care	-	16	mA
I_{CC6}	-5	-	976	mA
	-6	-	896	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-10	10	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	90	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	122	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	38	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	38	pF
Input/Output capacitance[DQ0-7, 9-16,18-25, 27-34]	C_{DQ}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns	6
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	10		10		ns	9
Refresh period	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35	ns	3

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.4/0.8V$, $V_{oh}/V_{ol}=2.4/0.4V$, output loading CL=100pF

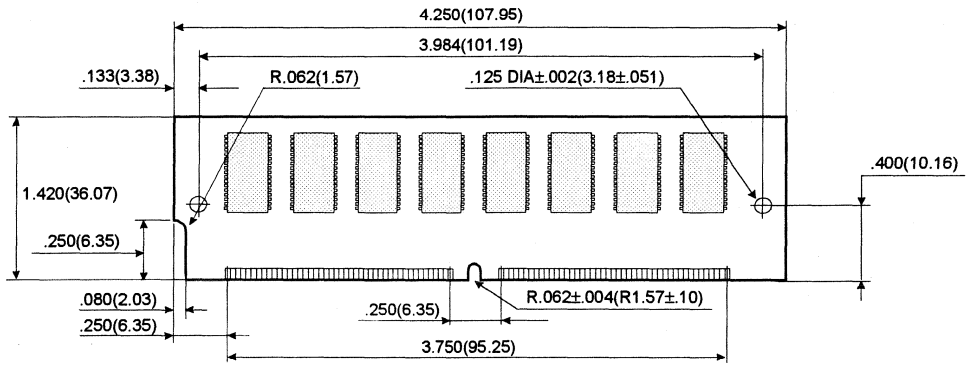
Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	35		40		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	

NOTES

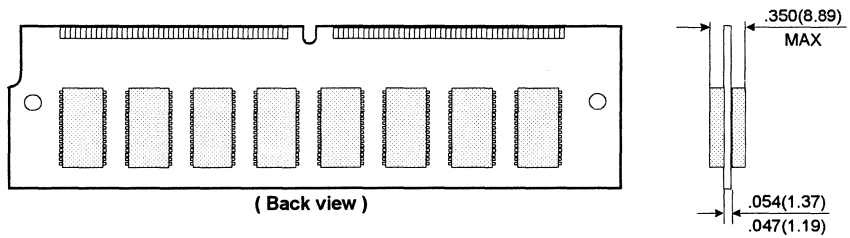
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

PACKAGE DIMENSIONS

Units : Inches (millimeters)

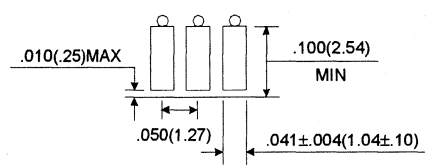


(Front view)



(Back view)

Gold/Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 16Mx4 DRAM, SOJ
DRAM Part No. : KMM53232000BK/BKG -- KM44C16100BK

KMM53232004BV/BVG EDO Mode

32M x 32 DRAM SIMM Using 16Mx4, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM53232004B is a 32Mx32bits Dynamic RAM high density memory module. The Samsung KMM53232004B consists of sixteen CMOS 16Mx4bits DRAMs in SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM53232004B is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

FEATURES

- Part Identification
  - KMM53232004BV(4K cycles/64ms Ref, SOJ, Solder)
  - KMM53232004BVG(4K cycles/64ms Ref, SOJ, Gold)
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ & Hidden Refresh capability
- $\overline{RAS}$-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1000mil), double sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	NC
2	DQ0	38	NC
3	DQ18	39	$\overline{Vss}$
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	RAS1
10	Vcc	46	$\overline{NC}$
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	$\overline{A9}$	68	PD2
33	$\overline{RAS3}$	69	PD3
34	RAS2	70	PD4
35	NC	71	NC
36	NC	72	Vss

PIN NAMES

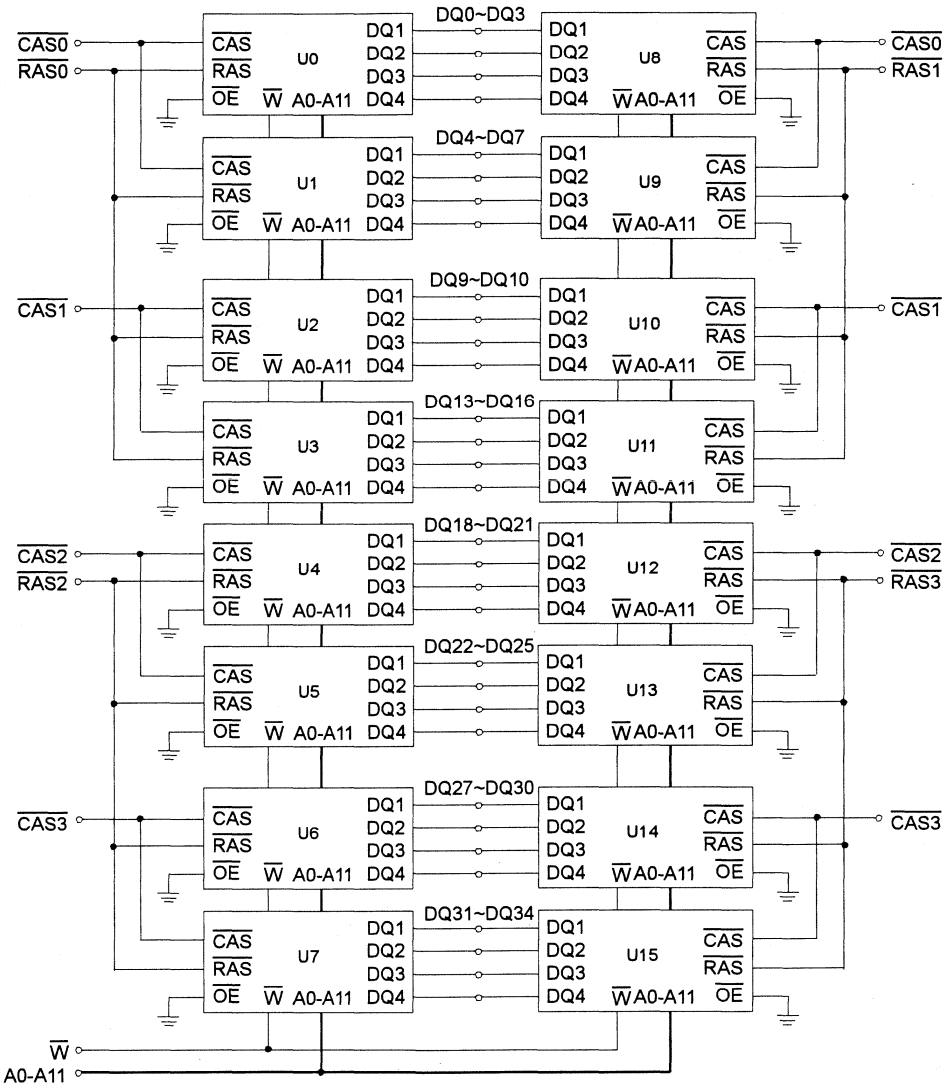
Pin Name	Function
A0 - A11	Address Inputs
DQ0-7, DQ9-16 DQ18-25, DQ27-34	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	NC	NC
PD2	Vss	Vss
PD3	Vss	NC
PD4	Vss	NC

SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	16	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, whcih is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM53232004BV/BVG		Unit
		Min	Max	
I_{CC1}	-5	-	976	mA
	-6	-	896	mA
I_{CC2}	Don't care	-	32	mA
I_{CC3}	-5	-	976	mA
	-6	-	896	mA
I_{CC4}	-5	-	896	mA
	-6	-	816	mA
I_{CC5}	Don't care	-	16	mA
I_{CC6}	-5	-	976	mA
	-6	-	896	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Hyper Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	90	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	122	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	38	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	38	pF
Input/Output capacitance[DQ0-7, 9-16,18-25, 27-34]	C_{DQ}	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	6,12
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		45		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	4
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	8		10		ns	9
Refresh period	t_{REF}		64		64	ms	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.4/0.8V$, $V_{oh}/V_{ol}=2.0/0.8V$, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3
Hyper page mode cycle time	t_{HPC}	20		25		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	6,12
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	6
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{W}$ pulse width	t_{WPE}	5		5		ns	

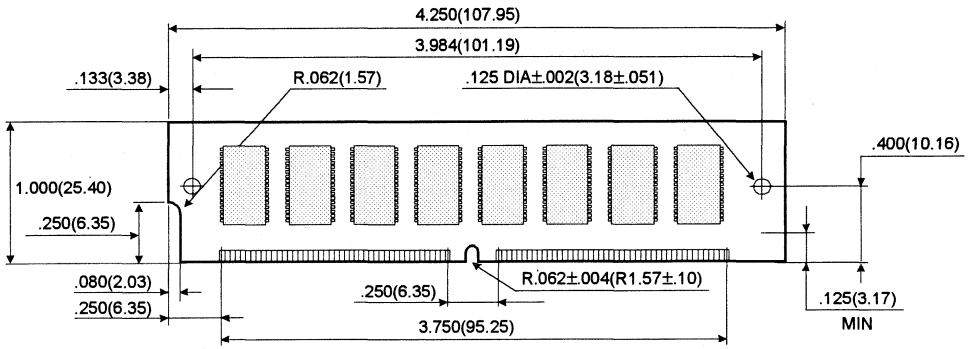
2

NOTES

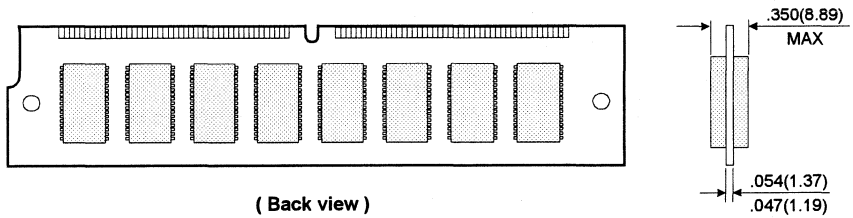
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit and is not referenced for V_{OH} or V_{OL}
7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit access time is controlled by t_{AA}.
11. $t_{ASC} \geq 6ns$, Assume $t_T=2.0ns$.
12. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

PACKAGE DIMENSIONS

Units : Inches (millimeters)

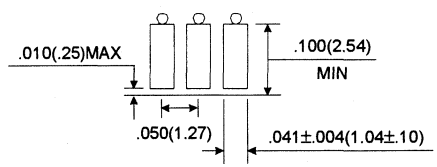


(Front view)



(Back view)

Gold/Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 16Mx4 DRAM, SOJ
DRAM Part No. : KMM53232004BV/BVG-- KM44C16104BK

KMM53232000BV/BVG Fast Page Mode
32M x 32 DRAM SIMM Using 16Mx4, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM53232000B is a 32Mx32bits Dynamic RAM high density memory module. The Samsung KMM53232000B consists of sixteen CMOS 16Mx4bits DRAMs in SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM53232000B is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns

FEATURES

- Part Identification
  - KMM53232000BV(4K cycles/64ms Ref, SOJ, Solder)
  - KMM53232000BVG(4K cycles/64ms Ref, SOJ, Gold)
- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ & Hidden Refresh capability
- $\overline{RAS}$-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1000mil), double sided component

2

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	NC
2	DQ0	38	NC
3	DQ18	39	$\overline{Vss}$
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	$\overline{RAS1}$
10	Vcc	46	$\overline{NC}$
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	$\overline{A9}$	68	PD2
33	$\overline{RAS3}$	69	PD3
34	$\overline{RAS2}$	70	PD4
35	NC	71	NC
36	NC	72	Vss

PIN NAMES

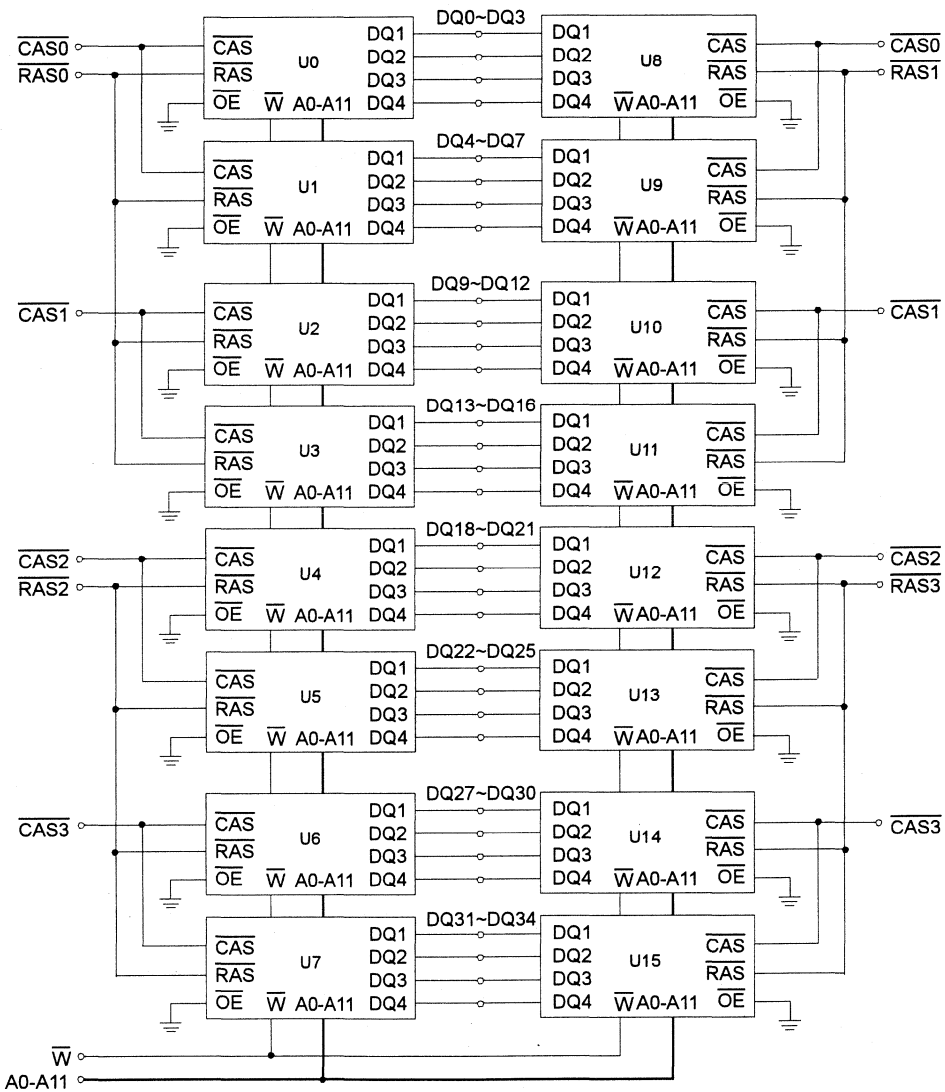
Pin Name	Function
A0 - A11	Address Inputs
DQ0-7, DQ9-16 DQ18-25, DQ27-34	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	NC	NC
PD2	Vss	Vss
PD3	Vss	NC
PD4	Vss	NC

SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	16	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM53232000BV/BVG		Unit
		Min	Max	
I_{CC1}	-5	-	976	mA
	-6	-	896	mA
I_{CC2}	Don't care	-	32	mA
I_{CC3}	-5	-	976	mA
	-6	-	896	mA
I_{CC4}	-5	-	576	mA
	-6	-	496	mA
I_{CC5}	Don't care	-	16	mA
I_{CC6}	-5	-	976	mA
	-6	-	896	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-10	10	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	90	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	122	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	38	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	38	pF
Input/Output capacitance[DQ0-7, 9-16,18-25, 27-34]	C_{DQ}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns	6
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	10		10		ns	9
Refresh period	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35	ns	3

AC CHARACTERISTICS ($0°C \leq T_A \leq 70 \leq °C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V, output loading CL=100pF

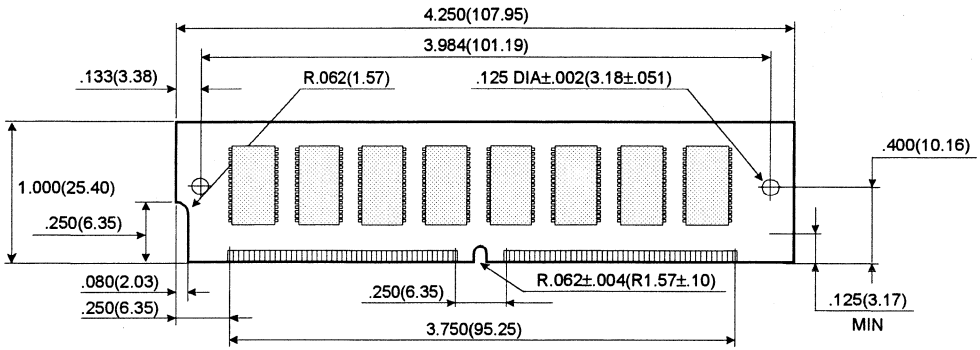
Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	35		40		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	

NOTES

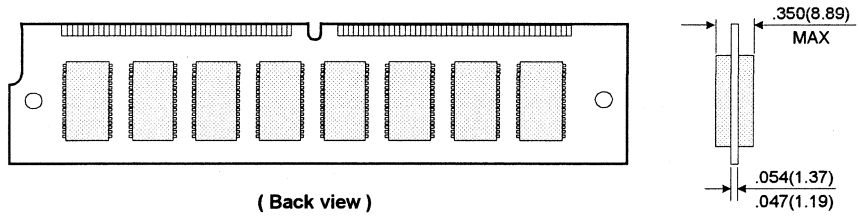
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

PACKAGE DIMENSIONS

Units : Inches (millimeters)

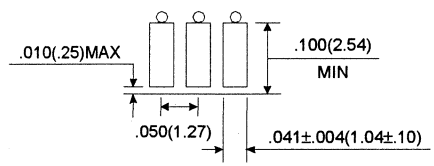


(Front view)



(Back view)

Gold/Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 16Mx4 DRAM, SOJ
DRAM Part No. : KMM53232000BV/BVG -- KM44C16100BK

KMM53232004BK/BKG EDO Mode

32M x 32 DRAM SIMM Using 16Mx4, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM53232004B is a 32Mx32bits Dynamic RAM high density memory module. The Samsung KMM53232004B consists of sixteen CMOS 16Mx4bits DRAMs in SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM53232004B is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

FEATURES

- Part Identification
  - KMM53232004BK(4K cycles/64ms Ref, SOJ, Solder)
  - KMM53232004BKG(4K cycles/64ms Ref, SOJ, Gold)
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ & Hidden Refresh capability
- $\overline{RAS}$-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1420mil), double sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	NC
2	DQ0	38	NC
3	DQ18	39	$\overline{Vss}$
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	$\overline{RAS1}$
10	Vcc	46	$\overline{NC}$
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	$\overline{A9}$	68	PD2
33	$\overline{RAS3}$	69	PD3
34	$\overline{RAS2}$	70	PD4
35	NC	71	NC
36	NC	72	Vss

PIN NAMES

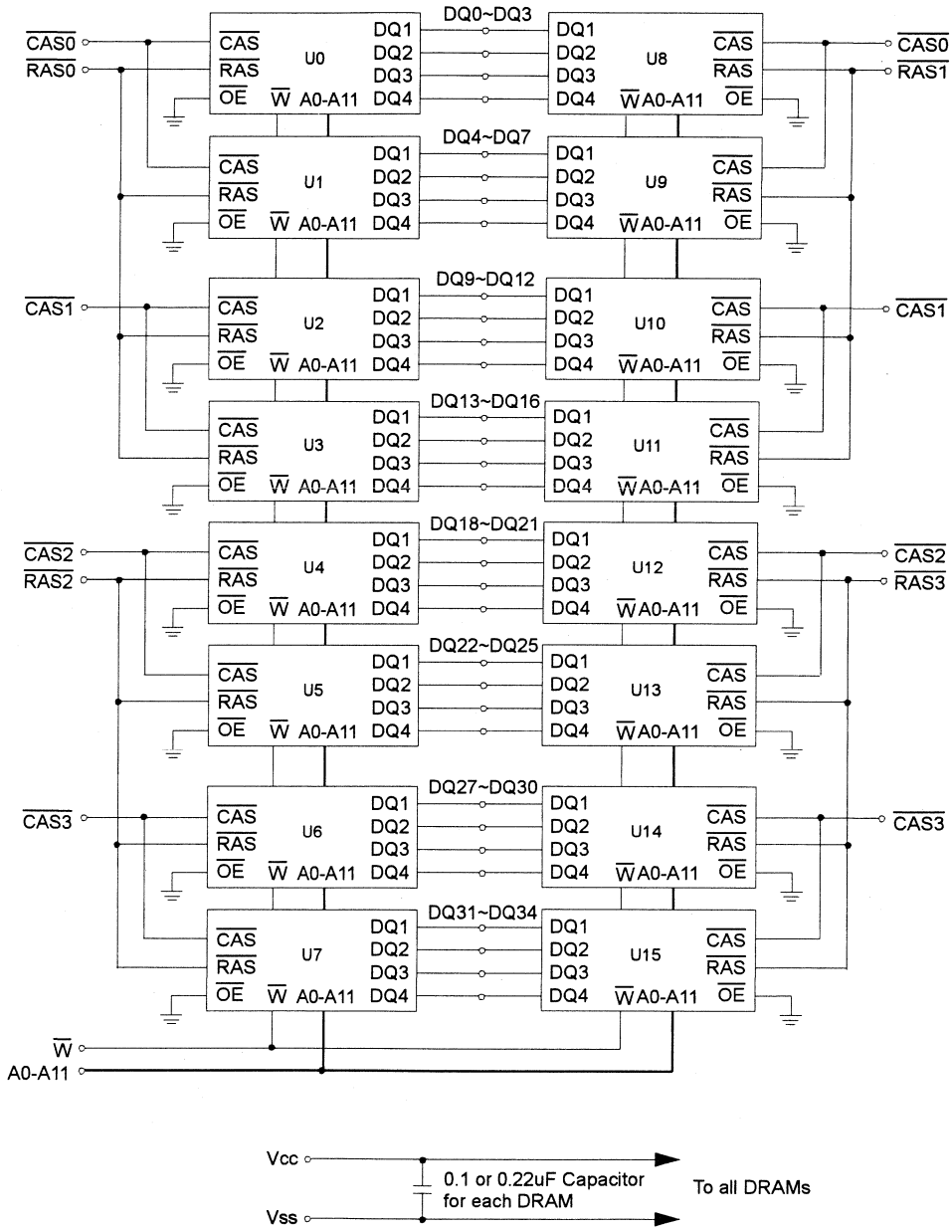
Pin Name	Function
A0 - A11	Address Inputs
DQ0-7, DQ9-16 DQ18-25, DQ27-34	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	NC	NC
PD2	Vss	Vss
PD3	Vss	NC
PD4	Vss	NC

SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	16	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, whcih is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM53232004BK/BKG		Unit
		Min	Max	
I_{CC1}	-5 -6	- -	976 896	mA mA
I_{CC2}	Don't care	-	32	mA
I_{CC3}	-5 -6	- -	976 896	mA mA
I_{CC4}	-5 -6	- -	896 816	mA mA
I_{CC5}	Don't care	-	16	mA
I_{CC6}	-5 -6	- -	976 896	mA mA
$I_{I(L)}$ $I_{O(L)}$	Don't care	-10 -10	10 10	uA uA
V_{OH} V_{OL}	Don't care	2.4 -	- 0.4	V V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Hyper Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	90	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	122	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	38	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	38	pF
Input/Output capacitance[DQ0-7, 9-16,18-25, 27-34]	C_{DQ}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	6,12
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		45		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	4
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	8		10		ns	9
Refresh period	t_{REF}		64		64	ms	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.4/0.8V$, $V_{oh}/V_{ol}=2.0/0.8V$, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Hyper page mode cycle time	t_{HPC}	20		25		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	6,12
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	6
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{W}$ pulse width	t_{WPE}	5		5		ns	

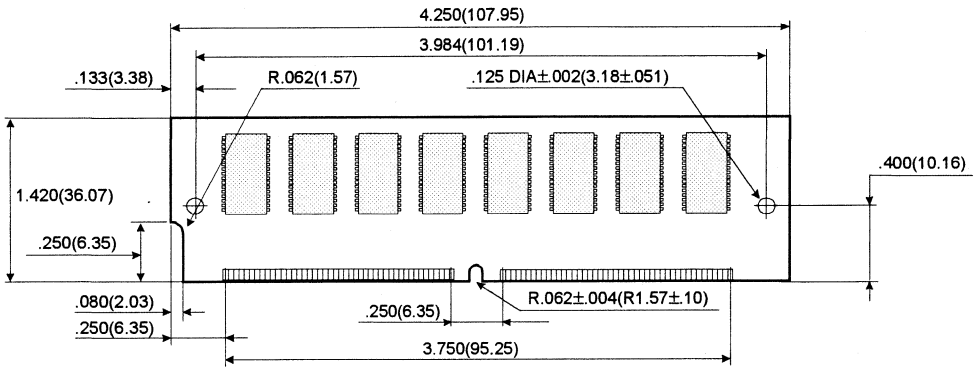
2

NOTES

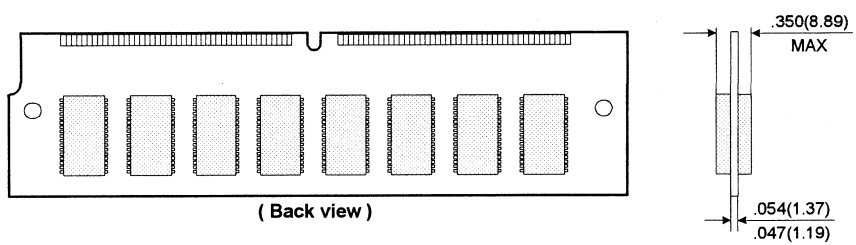
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit and is not referenced for V_{OH} or V_{OL}.
7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit access time is controlled by t_{AA}.
11. $t_{ASC} \geq 6ns$, Assume $t_T=2.0ns$.
12. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

PACKAGE DIMENSIONS

Units : Inches (millimeters)

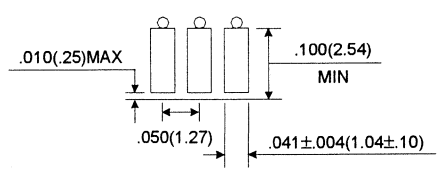


(Front view)



(Back view)

Gold/Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 16Mx4 DRAM, SOJ
DRAM Part No. : KMM53232004BK/BKG -- KM44C16104BK

SAMSUNG ELECTRONICS

KMM53632000BK/BKG Fast Page Mode

32M x 36 DRAM SIMM Using 16Mx4 & 16Mx1, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM53632000B is a 32Mx36bits Dynamic RAM high density memory module. The Samsung KMM53632000B consists of sixteen CMOS 16Mx4bits and eight CMOS 16Mx1bit DRAMs in SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM53632000B is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

FEATURES

- Part Identification
  - KMM53632000BK(4K cycles/64ms Ref, SOJ, Solder)
  - KMM53632000BKG(4K cycles/64ms Ref, SOJ, Gold)
- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ & Hidden Refresh capability
- $\overline{RAS}$-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1420mil), double sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	$\overline{Vss}$
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	$\overline{RAS1}$
10	Vcc	46	$\overline{NC}$
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	$\overline{A9}$	68	PD2
33	$\overline{RAS3}$	69	PD3
34	$\overline{RAS2}$	70	PD4
35	DQ26	71	NC
36	DQ8	72	Vss

PIN NAMES

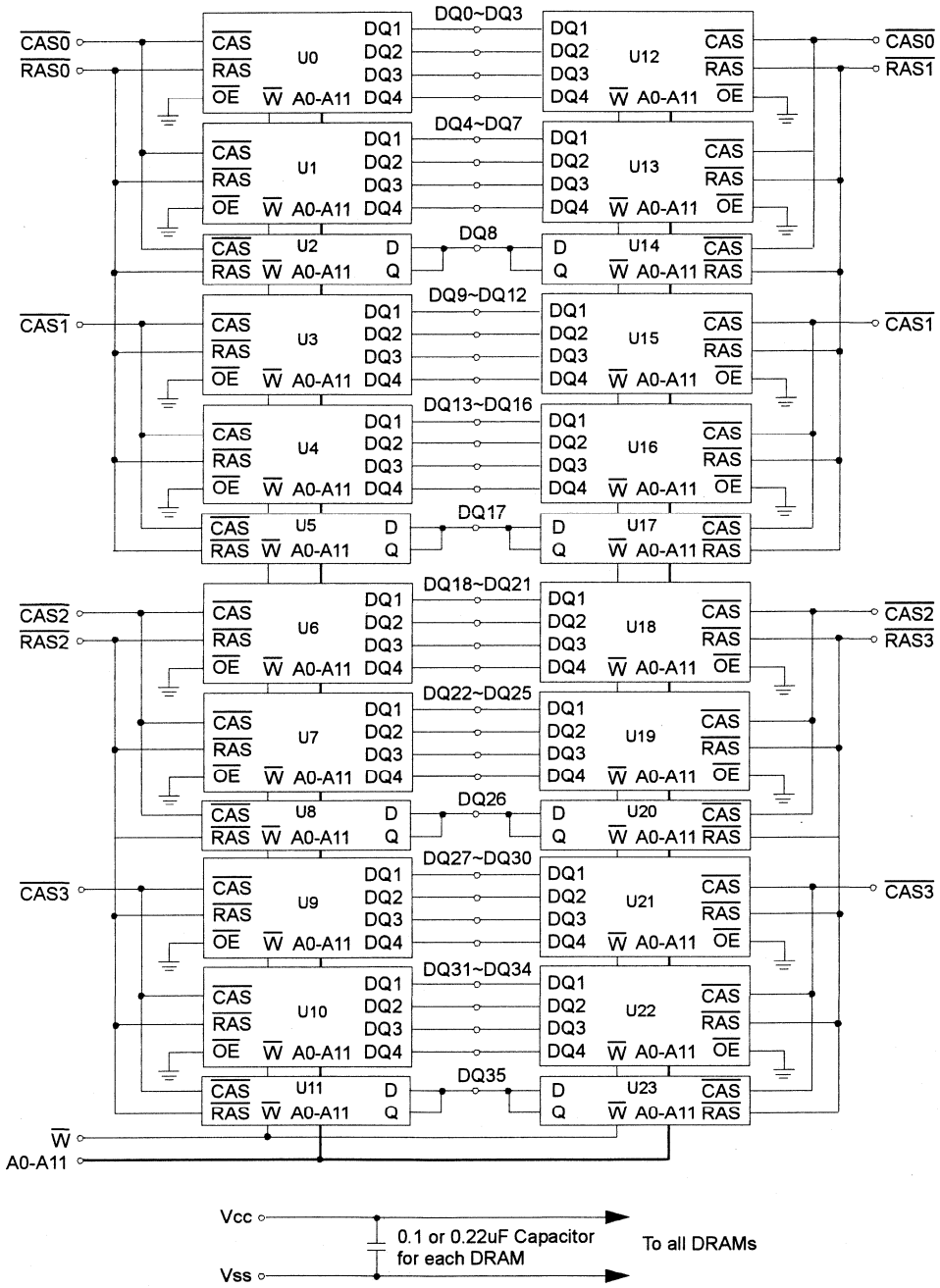
Pin Name	Function
A0 - A11	Address Inputs
DQ0 - 35	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	NC	NC
PD2	Vss	Vss
PD3	Vss	NC
PD4	Vss	NC

SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	24	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM53632000BK/BKG		Unit
		Min	Max	
I_{CC1}	-5 -6	- -	1344 1224	mA mA
I_{CC2}	Don't care	-	48	mA
I_{CC3}	-5 -6	- -	1344 1224	mA mA
I_{CC4}	-5 -6	- -	904 784	mA mA
I_{CC5}	Don't care	-	24	mA
I_{CC6}	-5 -6	- -	1344 1224	mA mA
$I_{I(L)}$ $I_{O(L)}$	Don't care	-10 -10	10 10	uA uA
V_{OH} V_{OL}	Don't care	2.4 -	- 0.4	V V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	130	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	178	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	52	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	52	pF
Input/Output capacitance[DQ0-35]	C_{DQ}	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns	6
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	10		10		ns	9
Refresh period	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35	ns	3

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.4/0.8V$, $V_{oh}/V_{ol}=2.4/0.4V$, output loading $C_L=100pF$

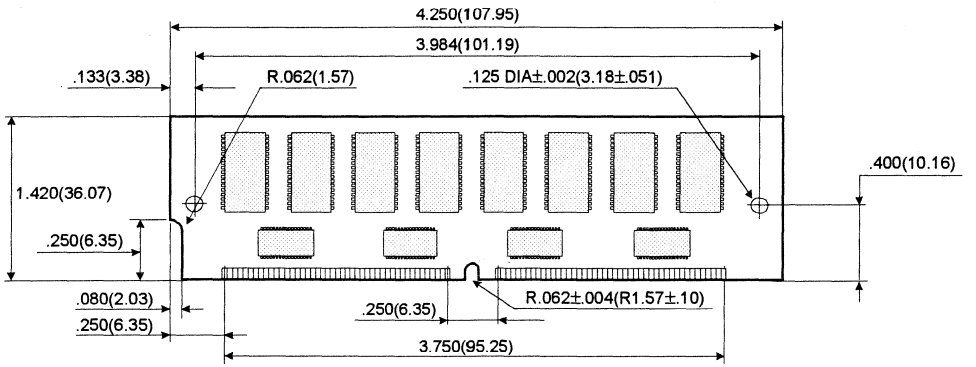
Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	35		40		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	

NOTES

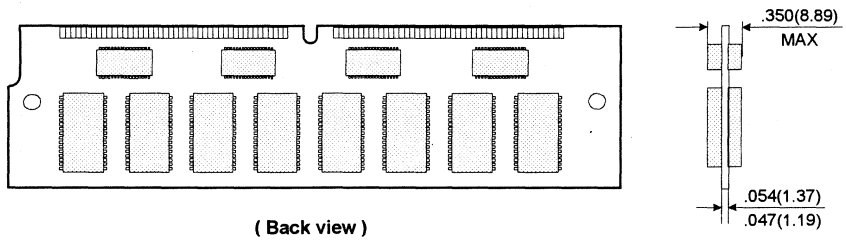
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

PACKAGE DIMENSIONS

Units : Inches (millimeters)

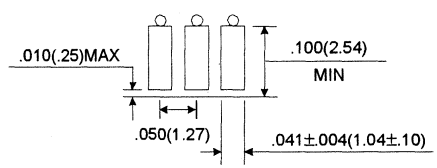


(Front view)



(Back view)

Gold/Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 16Mx4 DRAM & 16Mx1 DRAM, SOJ
DRAM Part No. : KMM53632000BK/BKG -- KM44C16100BK
KM41C16000CK

KMM53632004BK/BKG EDO Mode

32M x 36 DRAM SIMM Using 16Mx4 & 16Mx1 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM53632004B is a 32Mx36bits Dynamic RAM high density memory module. The Samsung KMM53632004B consists of sixteen CMOS 16Mx4bits and eight CMOS 16Mx1bit DRAMs in SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM53632004B is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

FEATURES

- Part Identification
  - KMM53632004BK(4K cycles/64ms Ref, SOJ, Solder)
  - KMM53632004BKG(4K cycles/64ms Ref, SOJ, Gold)
- Extended Out Data Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ & Hidden Refresh capability
- $\overline{RAS}$-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1420mil), double sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	$\overline{Vss}$
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	$\overline{RAS1}$
10	Vcc	46	$\overline{NC}$
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	$\overline{A9}$	68	PD2
33	$\overline{RAS3}$	69	PD3
34	$\overline{RAS2}$	70	PD4
35	DQ26	71	NC
36	DQ8	72	Vss

PIN NAMES

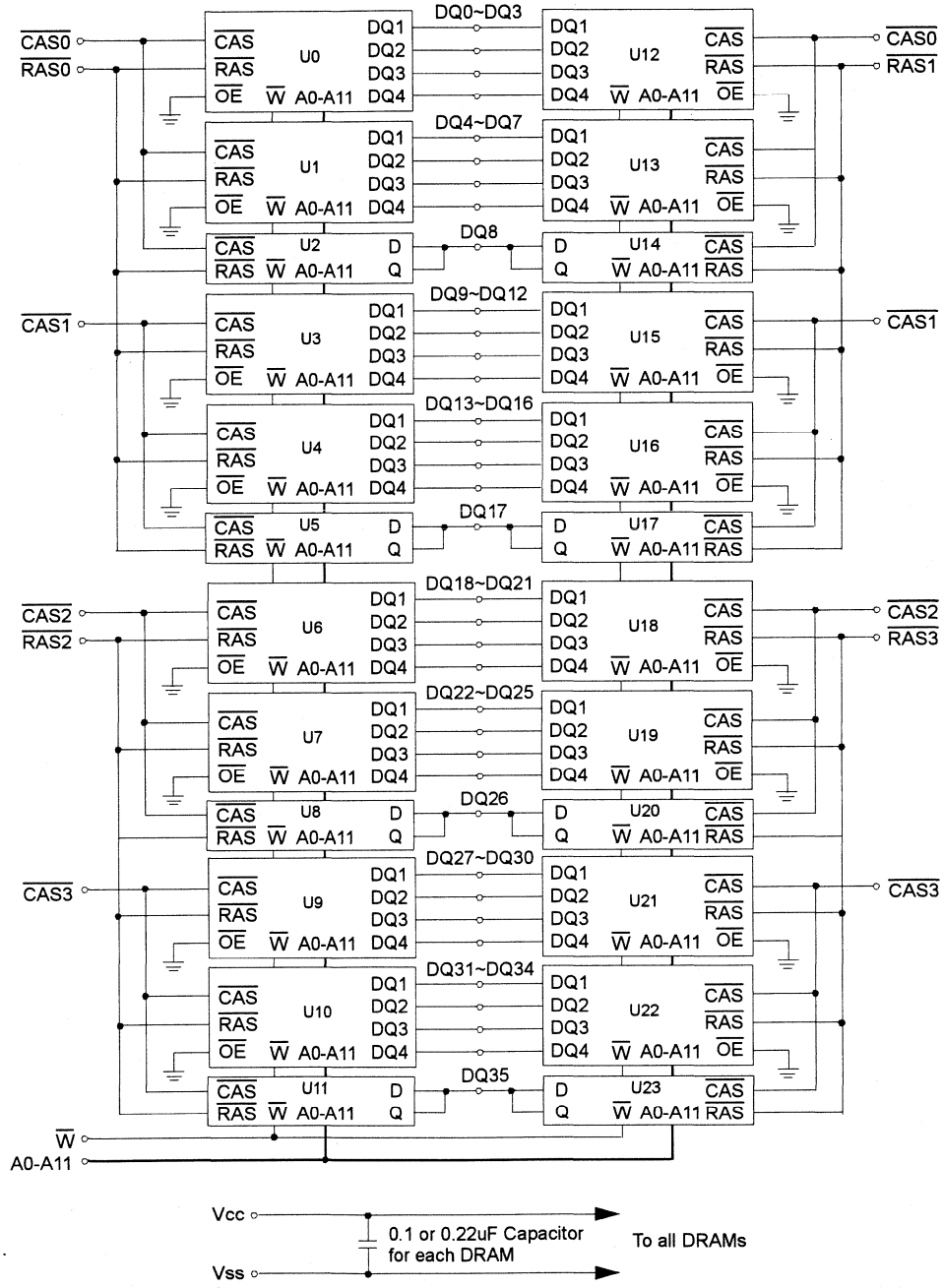
Pin Name	Function
A0 - A11	Address Inputs
DQ0 - 35	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	NC	NC
PD2	Vss	Vss
PD3	Vss	NC
PD4	Vss	NC

SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	24	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, whcih is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM53632004BK/BKG		Unit
		Min	Max	
I_{CC1}	-5	-	1344	mA
	-6	-	1224	mA
I_{CC2}	Don't care	-	48	mA
I_{CC3}	-5	-	1344	mA
	-6	-	1224	mA
I_{CC4}	-5	-	1224	mA
	-6	-	1104	mA
I_{CC5}	Don't care	-	24	mA
I_{CC6}	-5	-	1344	mA
	-6	-	1224	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-10	10	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Hyper Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	130	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	178	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	52	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	52	pF
Input/Output capacitance[DQ0 - 35]	C_{DQ}	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	6,12
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		45		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	4
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	8		10		ns	9
Refresh period	t_{REF}		64		64	ms	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.4/0.8V$, $V_{oh}/V_{ol}=2.0/0.8V$, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Hyper page mode cycle time	t_{HPC}	20		25		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	6,12
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	6
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{W}$ pulse width	t_{WPE}	5		5		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit and is not referenced for V_{OH} or V_{OL}.

7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

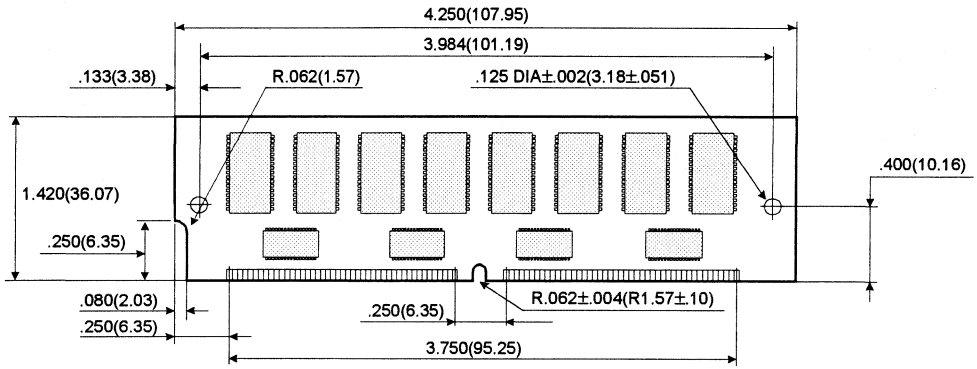
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit access time is controlled by t_{AA}.

11. $t_{ASC} \geq 6ns$, Assume tT=2.0ns.

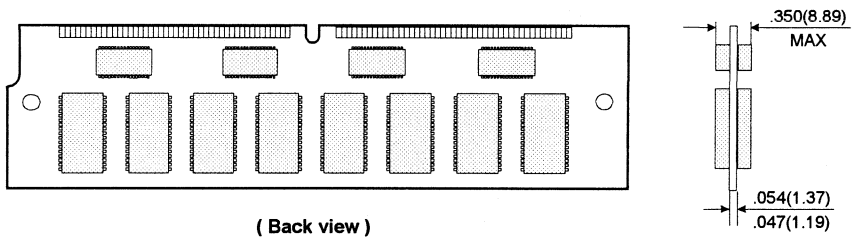
12. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

PACKAGE DIMENSIONS

Units : Inches (millimeters)

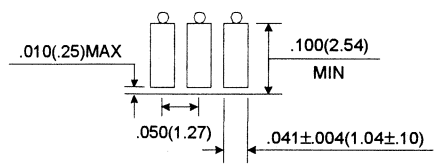


(Front view)



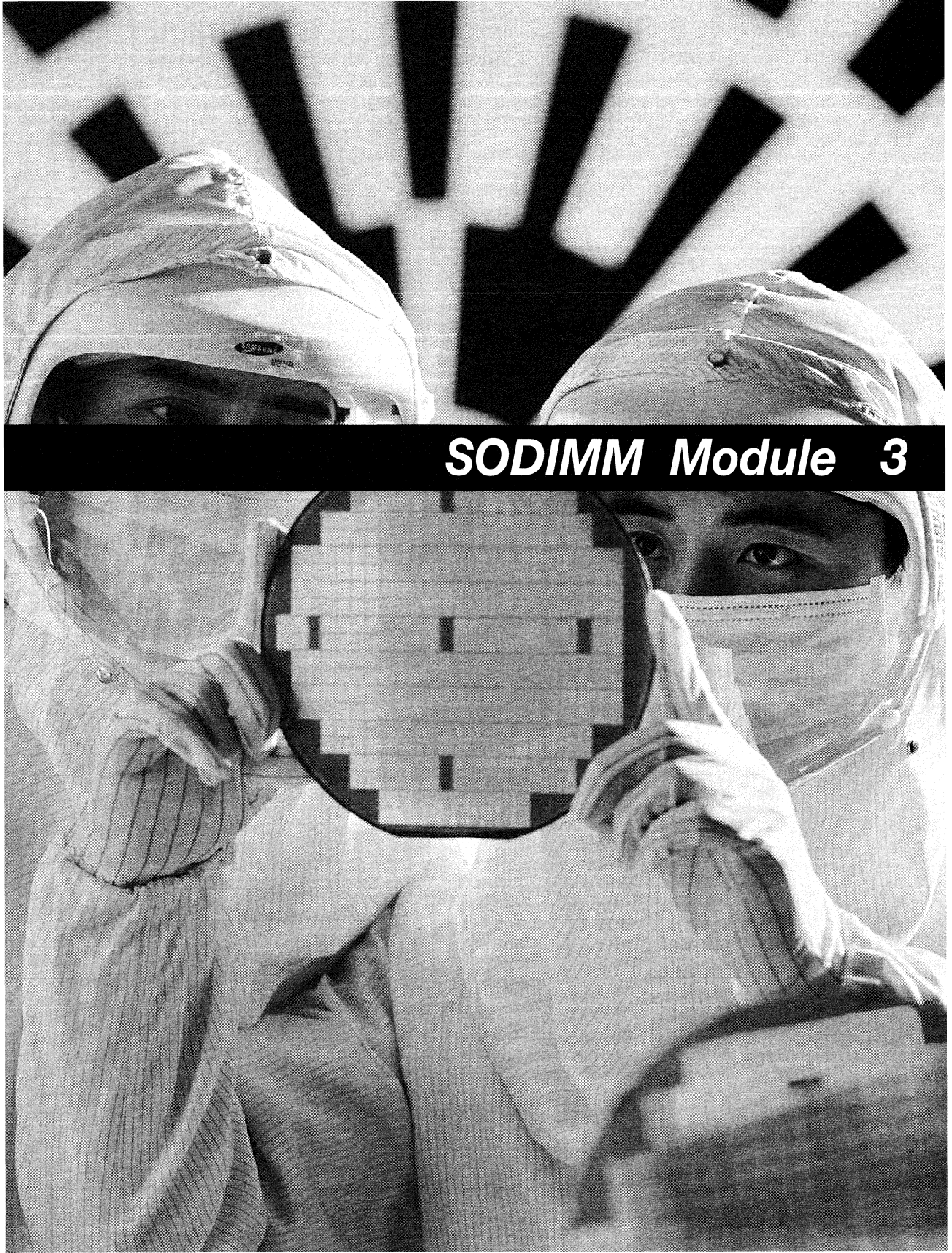
(Back view)

Gold/Solder Plating Lead



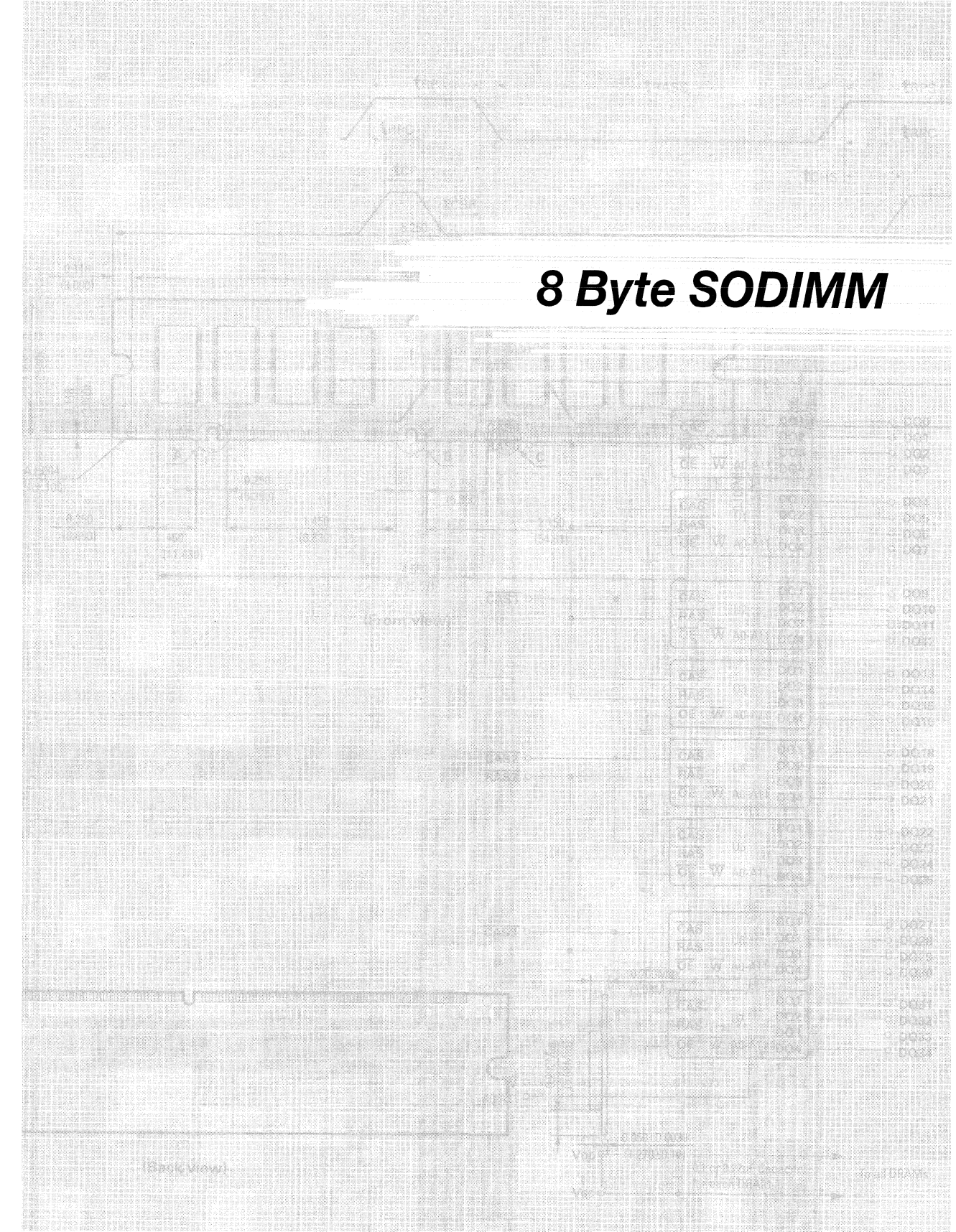
Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 16Mx4 DRAM & 16Mx1 DRAM, SOJ
DRAM Part No. : KMM53632004BK/BKG -- KM44C16104BK
KM41C16004CK



SODIMM Module 3

8 Byte SODIMM



KMM466F104CT1-L & KMM466F124CT1-L EDO Mode

1M x 64 DRAM SODIMM using 1Mx16, 1K/4K Refresh 3.3V, Low power/Self-Refresh

GENERAL DESCRIPTION

The Samsung KMM466F10(2)4CT1-L is a 1Mx64bits Dynamic RAM high density memory module. The Samsung KMM466F10(2)4CT1-L consists of four CMOS 1Mx16bits DRAMs in TSOP 400mil packages and 1K or 2K EEPROM in 8-pin TSSOP package mounted on a 144-pin glass-epoxy substrate. A 0.1uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM466F10(2)4CT1-L is a Small Out-line Dual in-line Memory Module and is intended for mounting into 144 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-L5	50ns	15ns	84ns	20ns
-L6	60ns	17ns	104ns	25ns

FEATURES

- Part Identification
  - KMM466F104CT1-L(4096 cycles/128ms, TSOP, L-ver)
  - KMM466F124CT1-L(1024 cycles/128ms, TSOP, L-ver)
- Extended Data Out Mode Operation
- New JEDEC standard proposal with EEPROM
- Serial Presense Detect with EEPROM
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Self -refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), double sided component

3

PIN CONFIGURATIONS

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	49	DQ13	50	DQ45	97	DQ22	98	DQ54
3	DQ0	4	DQ32	51	DQ14	52	DQ46	99	DQ23	100	DQ55
5	DQ1	6	DQ33	53	DQ15	54	DQ47	101	Vcc	102	Vcc
7	DQ2	8	DQ34	55	Vss	56	Vss	103	A6	104	A7
9	DQ3	10	DQ35	57	RSVD	58	RSVD	105	A8	106	A11
11	Vcc	12	Vcc	59	RSVD	60	RSVD	107	Vss	108	Vss
13	DQ4	14	DQ36	61	RFU	62	RFU	109	A9	110	NC
15	DQ5	16	DQ37	63	Vcc	64	Vcc	111	A10	112	NC
17	DQ6	18	DQ38	65	RFU	66	RFU	113	Vcc	114	Vcc
19	DQ7	20	DQ39	67	$\overline{W}$	68	RFU	115	$\overline{CAS2}$	116	$\overline{CAS6}$
21	Vss	22	Vss	69	$\overline{RAS0}$	70	RFU	117	$\overline{CAS3}$	118	$\overline{CAS7}$
23	$\overline{CAS0}$	24	$\overline{CAS4}$	71	NC	72	RFU	119	Vss	120	Vss
25	$\overline{CAS1}$	26	$\overline{CAS5}$	73	$\overline{OE}$	74	RFU	121	DQ24	122	DQ56
27	Vcc	28	Vcc	75	Vss	76	Vss	123	DQ25	124	DQ57
29	A0	30	A3	77	RSVD	78	RSVD	125	DQ26	126	DQ58
31	A1	32	A4	79	RSVD	80	RSVD	127	DQ27	128	DQ59
33	A2	34	A5	81	Vcc	82	Vcc	129	Vcc	130	Vcc
35	Vss	36	Vss	83	DQ16	84	DQ48	131	DQ28	132	DQ60
37	DQ8	38	DQ40	85	DQ17	86	DQ49	133	DQ29	134	DQ61
39	DQ9	40	DQ41	87	DQ18	88	DQ50	135	DQ30	136	DQ62
41	DQ10	42	DQ42	89	DQ19	90	DQ51	137	DQ31	138	DQ63
43	DQ11	44	DQ43	91	Vss	92	Vss	139	Vss	140	Vss
45	Vcc	46	Vcc	93	DQ20	94	DQ52	141	**SDA	142	**SCL
47	DQ12	48	DQ44	95	DQ21	96	DQ53	143	Vcc	144	Vcc

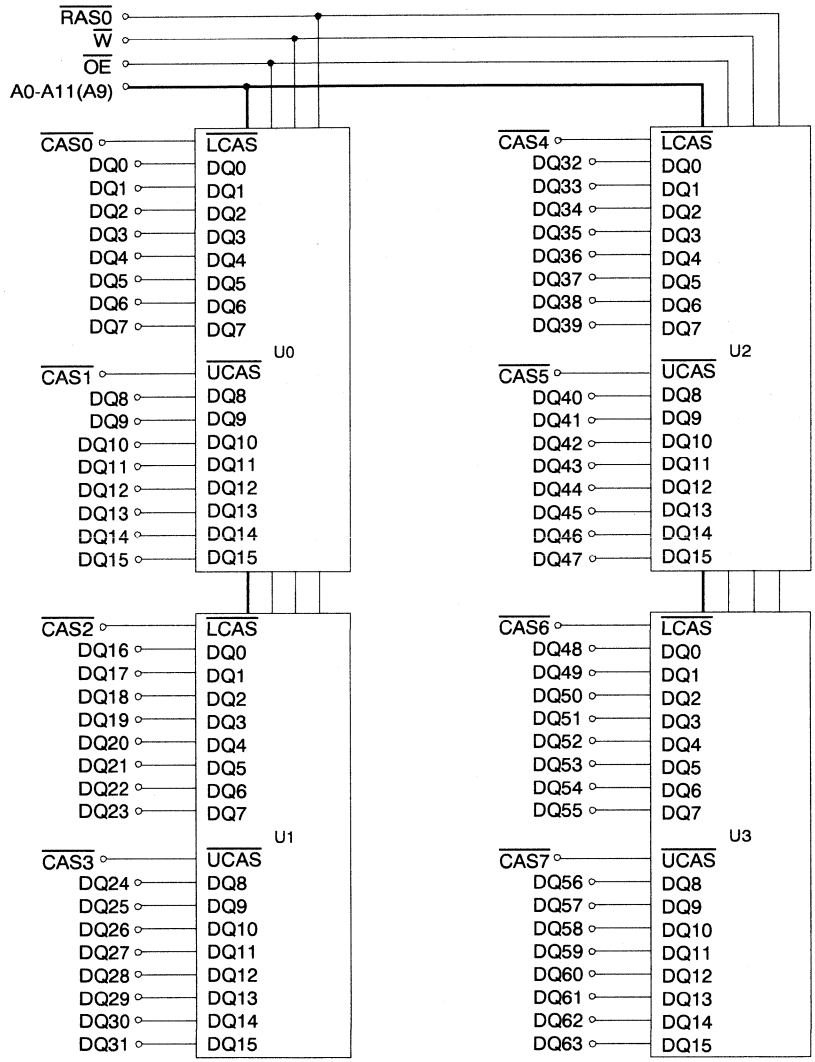
Note : A11 & A10 are used for only KMM466F104CT1-L (4K ref.)

PIN NAMES

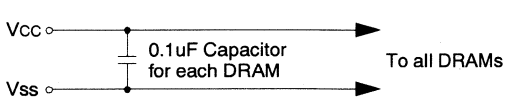
Pin Name	Function
A0 to 11	Address Inputs (4K ref.)
A0 to A9	Address Inputs (1K ref.)
DQ0 - DQ63	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{OE}$	Output Enable
$\overline{RAS0}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
**SDA	Serial Address / Data I/O
**SCL	Serial Clock
RSVD	Reserved Use
RFU	Reserved for Future Use

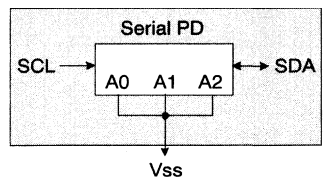
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

FUNCTIONAL BLOCK DIAGRAM



* A10 & A11 are used for only KMM466F104CT1-L (4K ref.)





ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	4	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70 °C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V at pulse width≤15ns, which is measured at V_{CC}.
*2 : -1.3V at pulse width≤15ns, which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM466F104CT1-L		KMM466F124CT1-L		Unit
		Min	Max	Min	Max	
I_{CC1}	-L5	-	360	-	560	mA
	-L6	-	320	-	520	mA
I_{CC2}	Don't care	-	4	-	4	mA
I_{CC3}	-L5	-	360	-	560	mA
	-L6	-	320	-	520	mA
I_{CC4}	-L5	-	400	-	400	mA
	-L6	-	360	-	360	mA
I_{CC5}	Don't care	-	0.8	-	0.8	mA
I_{CC6}	-L5	-	360	-	560	mA
	-L6	-	320	-	520	mA
I_{CC7}	Don't care	-	1.2	-	0.8	mA
I_{CCS}	Don't care	-	0.6	-	0.6	mA
$I_{I(L)}$	Don't care	-20	20	-20	20	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)
I_{CC2}: Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})
I_{CC3}: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)
I_{CC4}: Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)
I_{CC5}: Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)
I_{CC6}: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)
I_{CC7}: Battery back-up current. Average power supply, Battery back-up mode.
Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$,$\overline{LCAS}$=0.2V,
DQ=Don't care, t_{RC}=31.25us, t_{RAS}=t_{RAS}min~300ns
I_{CCS}: Self Refresh Current, $\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0~A1=V_{CC}-0.2V or 0.2V, DQ~DQ63=V_{CC}-0.2V or Open
$I_{I(L)}$: Input Leakage Current (Any input 0 ≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)
$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V ≤V_{OUT}≤V_{CC})
V_{OH}: Output High Voltage Level (I_{OH} = -2mA)
V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one page mode cycle, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11(A9)]	C_{IN1}	-	30	pF
Input capacitance[$\overline{W}$, $\overline{OE}$]	C_{IN2}	-	38	pF
Input capacitance[$\overline{RAS0}$]	C_{IN3}	-	38	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	17	pF
Input/Output capacitance[DQ0 - 63]	C_{DQ}	-	17	pF

AC CHARACTERISTICS (0°C≤TA≤70°C, See notes 1,2.)

Test condition : V_{CC}=3.3V±0.3V, V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	130		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	
Access time from $\overline{CAS}$	t_{CAC}		15		17	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,9
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	15	ns	3,11
Transition time(rise and fall)	t_T	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		17		ns	
$\overline{CAS}$ hold time	t_{CSH}	40		50		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	35	20	43	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	12
Column address hold time	t_{CAH}	8		10		ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	7
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	7
Write command set-up time	t_{WCS}	0		0		ns	6
Write command hold time	t_{WCH}	10		10		ns	6
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	15
Data set-up time	t_{DS}	0		0		ns	8
Data hold time	t_{DH}	8		10		ns	8
Refresh period	t_{REF}		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	38		42		ns	6,14
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		85		ns	6

AC CHARACTERISTICS (Countinued)

Test condition : V_{CC}=3.3V±0.3V, V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	6
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	16
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3
Hyper page mode cycle time	t_{HPC}	20		25		ns	10
Hyper page mode read-modify write cycle time	t_{HPRWC}	68		77		ns	10
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	8		10		ns	13
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{OE}$ access time	t_{OEA}		13		15	ns	3
$\overline{OE}$ to data delay	t_{OED}	13		15		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	13	3	15	ns	
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	11
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width	t_{WPE}	5		5		ns	
$\overline{RAS}$ pulse width (C-B-R self refresh)	t_{RASS}	100		100		us	17,18,19
$\overline{RAS}$ precharge time (C-B-R self refresh)	t_{RPS}	90		110		ns	17,18,19
$\overline{CAS}$ hold time (C-B-R self refresh)	t_{CHS}	-50		-50		ns	17,18,19

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not-restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

7. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

8. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

9. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit access time is controlled by t_{AA}.

10. $t_{ASC} \geq 6$ns, Assume t_T=2.0ns

11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

12. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.

13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ tradition low.

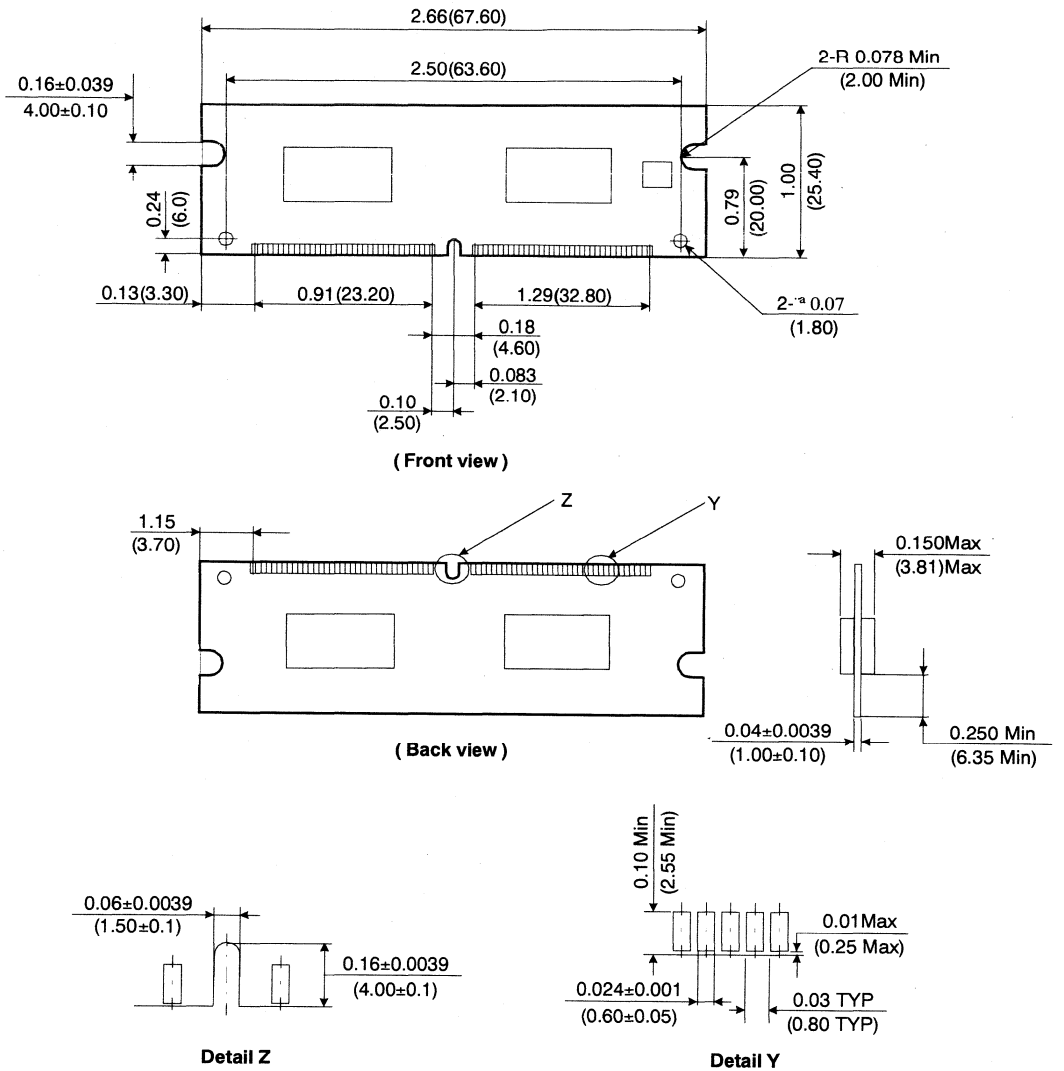
17. If $t_{RASS} \geq 100$us, then $\overline{RAS}$ precharge time must use t_{RPS} instead of t_{RP}.

18. For $\overline{RAS}$-only refresh and burst $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 4096 cycles of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.

19. For distributed $\overline{CAS}$-before-$\overline{RAS}$ with 15.6us interval $\overline{CAS}$-before-$\overline{RAS}$ should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

PACKAGE DIMENSIONS

Units : Inches (millimeters)



Tolerances : ±.005(.13) unless otherwise specified

The used device is 1Mx16 DRAM with EDO mode, TSOP
DRAM Part No. : KMM466F104CT1-L -- KM416V1004CT-L
KMM466F124CT1-L -- KM416V1204CT-L

KMM466F203CS1-L & KMM466F213CS1-L EDO Mode

2M x 64 DRAM SODIMM using 2MX8, 2K & 4K Refresh, 3.3V, Low power/Self-Refresh

GENERAL DESCRIPTION

The Samsung KMM466F20(1)3CS1-L is a 2Mx64bits Dynamic RAM high density memory module. The Samsung KMM466F20(1)3CS1-L consists of eight CMOS 2Mx8bits DRAMs in TSOP 400mil packages and a 1K or 2K EEPROM in 8-pin TSSOP package mounted on a 144-pin glass-epoxy substrate. A 0.1uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM466F20(1)3CS1-L is a Small Out-line Dual in-line Memory Module and is intended for mounting into 144 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-L5	50ns	13ns	90ns	25ns
-L6	60ns	15ns	110ns	30ns

FEATURES

- Part Identification
  - KMM466F203CS1-L(4096 cycles/128ms, TSOP, L-ver)
  - KMM466F213CS1-L(2048 cycles/128ms, TSOP, L-ver)
- Extended Data Out Mode Operation
- New JEDEC standard proposal with EEPROM
- Serial Presense Detect with EEPROM
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Self -refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), Double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	49	DQ13	50	DQ45	97	DQ22	98	DQ54
3	DQ0	4	DQ32	51	DQ14	52	DQ46	99	DQ23	100	DQ55
5	DQ1	6	DQ33	53	DQ15	54	DQ47	101	Vcc	102	Vcc
7	DQ2	8	DQ34	55	Vss	56	Vss	103	A6	104	A7
9	DQ3	10	DQ35	57	RSVD	58	RSVD	105	A8	106	N.C
11	Vcc	12	Vcc	59	RSVD	60	RSVD	107	Vss	108	Vss
13	DQ4	14	DQ36	61	RFU	62	RFU	109	A9	110	NC
15	DQ5	16	DQ37	63	Vcc	64	Vcc	111	A10	112	A11
17	DQ6	18	DQ38	65	RFU	66	RFU	113	Vcc	114	Vcc
19	DQ7	20	DQ39	67	$\overline{W}$	68	RFU	115	$\overline{CAS2}$	116	$\overline{CAS6}$
21	Vss	22	Vss	69	$\overline{RAS0}$	70	RFU	117	$\overline{CAS3}$	118	$\overline{CAS7}$
23	$\overline{CAS0}$	24	$\overline{CAS4}$	71	NC	72	RFU	119	Vss	120	Vss
25	$\overline{CAS1}$	26	$\overline{CAS5}$	73	$\overline{OE}$	74	RFU	121	DQ24	122	DQ56
27	Vcc	28	Vcc	75	Vss	76	Vss	123	DQ25	124	DQ57
29	A0	30	A3	77	RSVD	78	RSVD	125	DQ26	126	DQ58
31	A1	32	A4	79	RSVD	80	RSVD	127	DQ27	128	DQ59
33	A2	34	A5	81	Vcc	82	Vcc	129	Vcc	130	Vcc
35	Vss	36	Vss	83	DQ16	84	DQ48	131	DQ28	132	DQ60
37	DQ8	38	DQ40	85	DQ17	86	DQ49	133	DQ29	134	DQ61
39	DQ9	40	DQ41	87	DQ18	88	DQ50	135	DQ30	136	DQ62
41	DQ10	42	DQ42	89	DQ19	90	DQ51	137	DQ31	138	DQ63
43	DQ11	44	DQ43	91	Vss	92	Vss	139	Vss	140	Vss
45	Vcc	46	Vcc	93	DQ20	94	DQ52	141	**SDA	142	**SCL
47	DQ12	48	DQ44	95	DQ21	96	DQ53	143	Vcc	144	Vcc

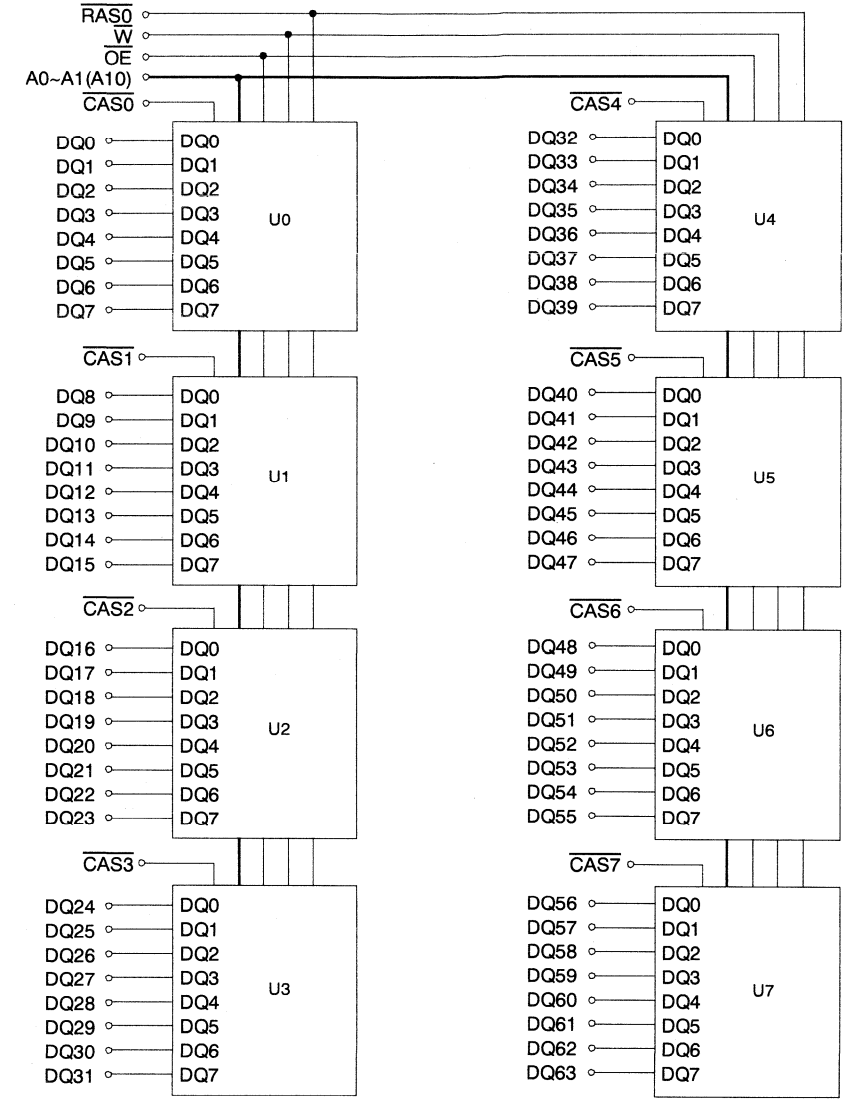
Note : A11 is used for only KMM466F203CS1-L (4K ref.)

PIN NAMES

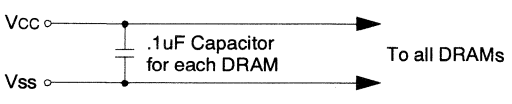
Pin Name	Function
A0 to 11	Address Inputs (4K ref.)
A0 to 10	Address Inputs (2K ref.)
DQ0 - DQ63	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{OE}$	Output Enable
$\overline{RAS0}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Colume Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
**SDA	Serial Address / Data I/O
**SCL	Serial Clock
RSVD	Reserved Use
RFU	Reserved for Future Use

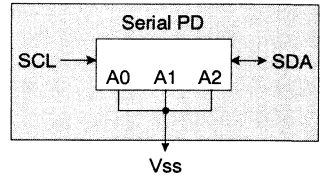
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

FUNCTIONAL BLOCK DIAGRAM



*A11 is used for only KMM466F203CS1-L (4K ref.)





ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V at pulse width≤15ns, which is measured at V_{CC}.

*2 : -1.3V at pulse width ≤15ns, which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM466F203CS1-L		KMM466F213CS1-L		Unit
		Min	Max	Min	Max	
I_{CC1}	-L5	-	720	-	880	mA
	-L6	-	640	-	800	
I_{CC2}	Don't care	-	8	-	8	mA
I_{CC3}	-L5	-	720	-	880	mA
	-L6	-	640	-	800	mA
I_{CC4}	-L5	-	640	-	720	mA
	-L6	-	560	-	640	mA
I_{CC5}	Don't care	-	1.6	-	1.6	mA
I_{CC6}	-L5	-	720	-	880	mA
	-L6	-	640	-	800	mA
I_{CC7}	-	-	2.0	-	2.0	mA
I_{CCS}	-	-	1.6	-	1.6	mA
$I_{I(L)}$	Don't care	-40	40	-40	40	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @ t_{RC}=min)

I_{CC7} : Battery back-up current. Average power supply, Battery back-up mode.
Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$,$\overline{LCAS}$=0.2V,
Din=Don't care, t_{RC}=31.25us(4K/L-ver), 62.5us(2K/L-ver), t_{RAS}=t_{RAS}min~300ns)

I_{CCS} : Self Refresh Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0~A1=V_{CC}-0.2V or 0.2V, DQ~DQ63=V_{CC}-0.2V or Open)

$I_{I(L)}$: Input Leakage Current (Any input 0 ≤V_{IN}≤V_{CC}+0.3V, all other pins not under test=0 V)

$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V¡ÂV_{OUT} ¡ÂV_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one page mode cycle, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A10]	C_{IN1}	-	50	pF
Input capacitance[$\overline{W}$, $\overline{OE}$]	C_{IN2}	-	66	pF
Input capacitance[$\overline{RAS0}$]	C_{IN3}	-	66	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	17	pF
Input/Output capacitance[DQ0 - 63]	C_{DQ}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See notes 1,2.)

Test condition : V_{CC}=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	131		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,9
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	15	ns	3,12
Transition time(rise and fall)	t_T	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		45		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	13
Column address hold time	t_{CAH}	8		10		ns	13
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	7
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	7
Write command set-up time	t_{WCS}	0		0		ns	6
Write command hold time	t_{WCH}	10		10		ns	6
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	16
Data set-up time	t_{DS}	0		0		ns	8
Data hold time	t_{DH}	8		10		ns	8
Refresh period	t_{REF}		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ dealy time	t_{CWD}	36		40		ns	6,15
$\overline{RAS}$ to $\overline{W}$ dealy time	t_{RWD}	73		85		ns	6

AC CHARACTERISTICS (Countinued)

Test condition : V_{CC}=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	6
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
$\overline{CAS}$ precharge time (CBR counter test cycle)	t_{CPT}	20		20		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3
Hyper page mode cycle time	t_{HPC}	25		30		ns	10
Hyper page mode read-modify write cycle time	t_{HPRWC}	68		77		ns	10
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	8		10		ns	14
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{OE}$ access time	t_{OEA}		13		15	ns	3
$\overline{OE}$ to data delay	t_{OED}	13		15		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	13	3	15	ns	
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	12
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width	t_{WPE}	5		5		ns	
$\overline{RAS}$ pulse width (C-B-R self refresh)	t_{RASS}	100		100		ns	11
$\overline{RAS}$ precharge time (C-B-R self refresh)	t_{RPS}	90		110		ns	11
$\overline{CAS}$ hold time (C-B-R self refresh)	t_{CHS}	-50		-50		ns	11

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not-restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminated.

7. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

8. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

9. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit access time is controlled by t_{AA}.

10. $t_{ASC} \geq 6$ns, Assume tT=2.0ns

11. For all of the refresh mode except distributed $\overline{CAS}$-before-$\overline{RAS}$ refresh, 4096 cycles of burst refresh must be executed withtin 16ms before and after self-refresh in order to meet refresh specification.

12. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

13. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.

14. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

15. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

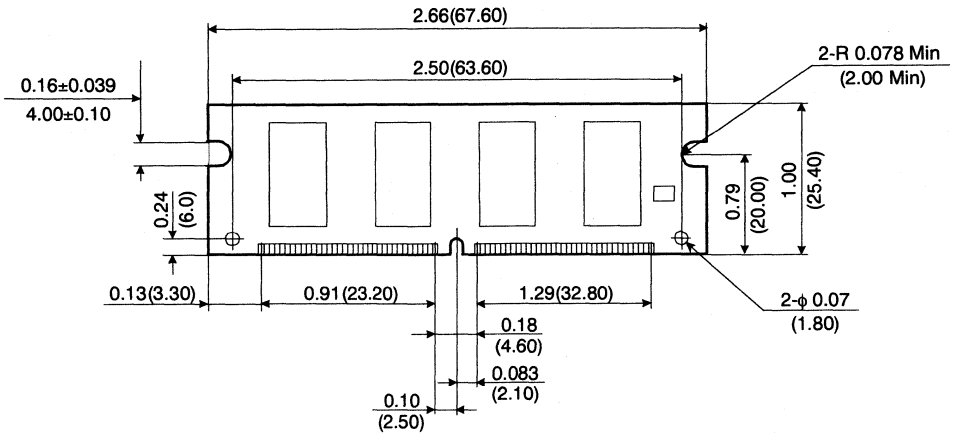
16. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

17. t_{CSR} is referenced to earlier $\overline{CAS}$ falling edge to the $\overline{RAS}$ falling edge.

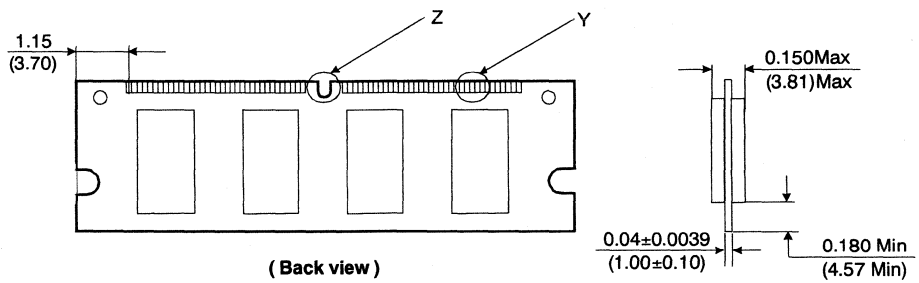
3

PACKAGE DIMENSIONS

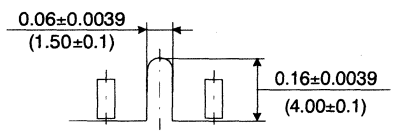
Units : Inches (millimeters)



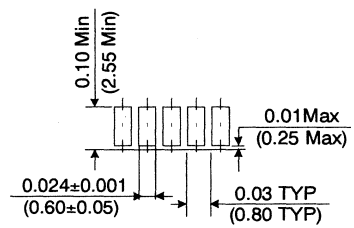
(Front view)



(Back view)



Detail Z



Detail Y

Tolerances : ±.005(.13) unless otherwise specified

The used device is 2MX8 DRAM with EDO mode, TSOP
DRAM Part No. : KMM466F203CS1-L -- KM48V2004CS-L
KMM466F213CS1-L -- KM48V2104CS-L

Revision History
Rev 0.0 : Aug. 1997

KMM466F404CS2-L EDO Mode

4M x 64 DRAM SODIMM Using 4Mx16, 4K Refresh 3.3V, Low power/Self-Refresh

GENERAL DESCRIPTION

The Samsung KMM466F404CS2-L is a 4Mx64bits Dynamic RAM high density memory module. The Samsung KMM466F404CS2-L consists of four CMOS 4Mx16bits DRAMs in TSOP 400mil packages and a 2K EEPROM in 8-pin TSSOP package mounted on a 144-pin glass-epoxy substrate. A 0.1uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM466F404CS2-L is a Small Out-line Dual in-line Memory Module and is intended for mounting into 144 pin edge connector sockets.

FEATURES

- Part Identification
  - KMM466F404CS2-L(4096 cycles/128ms, TSOP, L-ver)
- Extended Data Out Mode Operation
- New JEDEC standard proposal with EEPROM
- Serial Presense Detect with EEPROM
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Self -refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), double sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

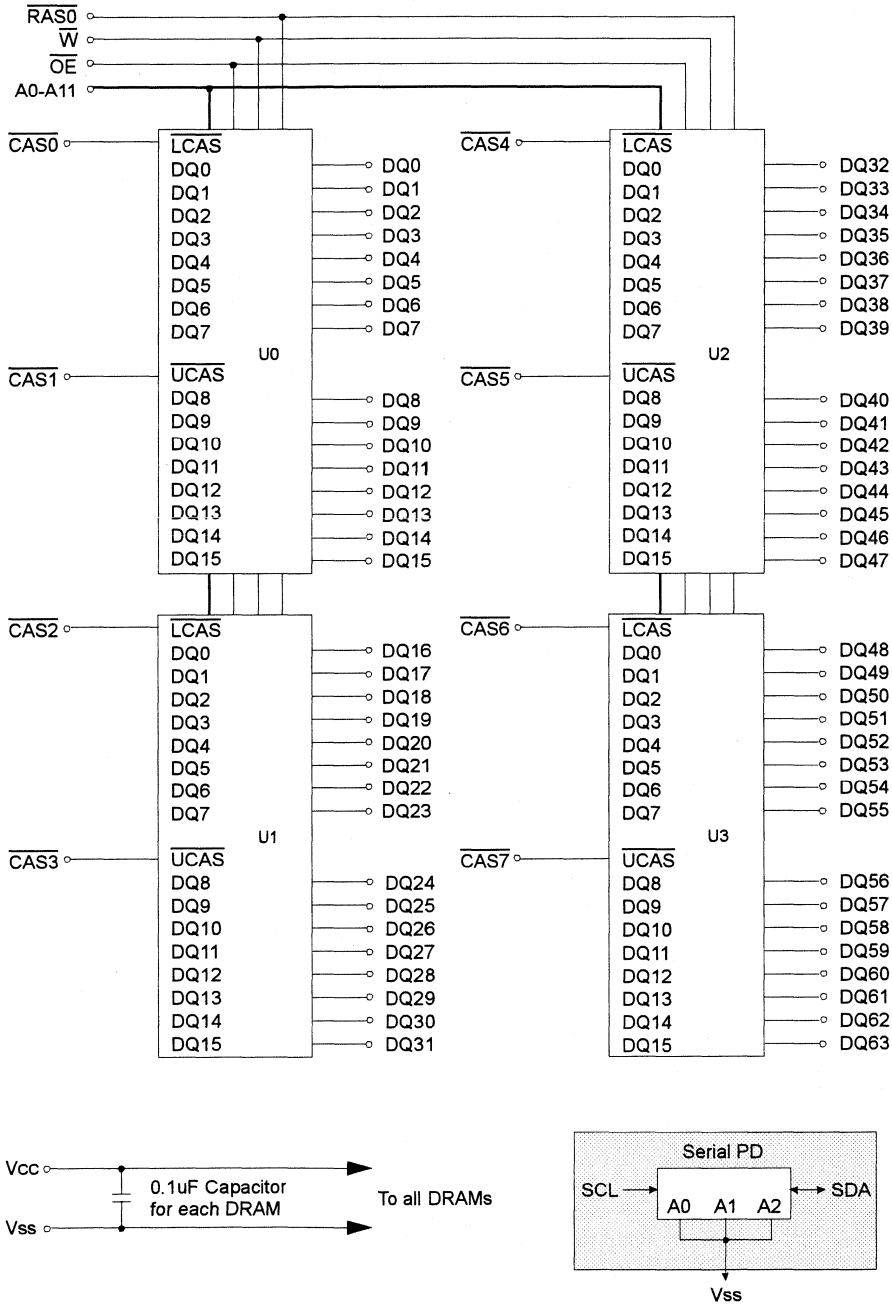
PIN CONFIGURATIONS

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	49	DQ13	50	DQ45	97	DQ22	98	DQ54
3	DQ0	4	DQ32	51	DQ14	52	DQ46	99	DQ23	100	DQ55
5	DQ1	6	DQ33	53	DQ15	54	DQ47	101	Vcc	102	Vcc
7	DQ2	8	DQ34	55	Vss	56	Vss	103	A6	104	A7
9	DQ3	10	DQ35	57	RSVD	58	RSVD	105	A8	106	A11
11	Vcc	12	Vcc	59	RSVD	60	RSVD	107	Vss	108	Vss
13	DQ4	14	DQ36	61	RFU	62	RFU	109	A9	110	NC
15	DQ5	16	DQ37	63	Vcc	64	Vcc	111	A10	112	NC
17	DQ6	18	DQ38	65	RFU	66	RFU	113	Vcc	114	Vcc
19	DQ7	20	DQ39	67	$\overline{W}$	68	RFU	115	$\overline{CAS2}$	116	$\overline{CAS6}$
21	Vss	22	Vss	69	$\overline{RAS0}$	70	RFU	117	$\overline{CAS3}$	118	$\overline{CAS7}$
23	$\overline{CAS0}$	24	$\overline{CAS4}$	71	NC	72	RFU	119	Vss	120	Vss
25	$\overline{CAS1}$	26	$\overline{CAS5}$	73	$\overline{OE}$	74	RFU	121	DQ24	122	DQ56
27	Vcc	28	Vcc	75	Vss	76	Vss	123	DQ25	124	DQ57
29	A0	30	A3	77	RSVD	78	RSVD	125	DQ26	126	DQ58
31	A1	32	A4	79	RSVD	80	RSVD	127	DQ27	128	DQ59
33	A2	34	A5	81	Vcc	82	Vcc	129	Vcc	130	Vcc
35	Vss	36	Vss	83	DQ16	84	DQ48	131	DQ28	132	DQ60
37	DQ8	38	DQ40	85	DQ17	86	DQ49	133	DQ29	134	DQ61
39	DQ9	40	DQ41	87	DQ18	88	DQ50	135	DQ30	136	DQ62
41	DQ10	42	DQ42	89	DQ19	90	DQ51	137	DQ31	138	DQ63
43	DQ11	44	DQ43	91	Vss	92	Vss	139	Vss	140	Vss
45	Vcc	46	Vcc	93	DQ20	94	DQ52	141	SDA	142	SCL
47	DQ12	48	DQ44	95	DQ21	96	DQ53	143	Vcc	144	Vcc

PIN NAMES

Pin Name	Function
A0 to A11	Address Inputs
DQ0 - DQ63	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{OE}$	Output Enable
$\overline{RAS0}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
SDA	Serial Address / Data I/O
SCL	Serial Clock
RSVD	Reserved Use
RFU	Reserved for Future Use

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	4	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V at pulse width≤15ns, which is measured at V_{CC}.
*2 : -1.3V at pulse width≤15ns, which is measured at Vss.

3

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM466F404CS2-L		Unit
		Min	Max	
I_{CC1}	-5	-	480	mA
	-6	-	440	mA
I_{CC2}	Don't care	-	4	mA
I_{CC3}	-5	-	480	mA
	-6	-	440	mA
I_{CC4}	-5	-	360	mA
	-6	-	320	mA
I_{CC5}	Don't care	-	0.8	mA
I_{CC6}	-5	-	480	mA
	-6	-	440	mA
I_{CC7}	Don't care	-	1.4	mA
I_{CCS}	Don't care	-	1.4	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)
I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})
I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)
I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)
I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)
I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)
I_{CC7} : Battery back-up current. Average power supply, Battery back-up mode.
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$,$\overline{LCAS}$=0.2V,
Din=Don't care, t_{RC}=31.25us, t_{RAS}=t_{RAS}min~300ns
I_{CCS} : Self Refresh Current, $\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0~A11=Vcc-0.2V or 0.2V, DQ~DQ63=Vcc-0.2V or Open
$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)
$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)
V_{OH} : Output High Voltage Level (I_{OH} = -2mA)
V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	30	pF
Input capacitance[$\overline{W}$, $\overline{OE}$]	C_{IN2}	-	38	pF
Input capacitance[$\overline{RAS0}$]	C_{IN3}	-	38	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	17	pF
Input/Output capacitance[DQ0 - 63]	C_{DQ}	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	128		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,9
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,9
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	3,11
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	8		10		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		40		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	17	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	12	25	15	30	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	7		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	12
Column address hold time	t_{CAH}	7		10		ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	7
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	7
Write command set-up time	t_{WCS}	0		0		ns	6
Write command hold time	t_{WCH}	7		10		ns	6
Write command pulse width	t_{WP}	7		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	8		10		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	7		10		ns	15
Data set-up time	t_{DS}	0		0		ns	8,18
Data hold time	t_{DH}	7		10		ns	8,18
Refresh period	t_{REF}		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	33		38		ns	6,14
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	70		84		ns	6

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.2/0.7V$, $V_{oh}/V_{ol}=2.0/0.8V$, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	45		53		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	47		58		ns	6
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	16
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	17
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3
Hyper page mode cycle time	t_{HPC}	20		25		ns	10
Hyper page mode read-modify write cycle time	t_{HPRWC}	67		73		ns	10
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	7		10		ns	13
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time (C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time (C-B-R refresh)	t_{WRH}	10		10		ns	
$\overline{OE}$ access time	t_{OEA}		13		15	ns	3
$\overline{OE}$ to data delay	t_{OED}	10		13		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	13	3	13	ns	
$\overline{OE}$ command hold time	t_{OEH}	5		5		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	11
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width(Hyper page cycle)	t_{WPE}	5		5		ns	
$\overline{RAS}$ pulse width (C-B-R self refresh)	t_{RASS}	100		100		us	19,20,21
$\overline{RAS}$ precharge time (C-B-R self refresh)	t_{RPS}	90		110		ns	19,20,21
$\overline{CAS}$ hold time (C-B-R self refresh)	t_{CHS}	-50		-50		ns	19,20,21

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are non-restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

7. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

8. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

9. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit access time is controlled by t_{AA}.

10. $t_{ASC} \geq 6$ns, Assume tT=2.0ns

11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

12. t_{ASC} is referenced to the earlier $\overline{CAS}$ falling edge and t_{CAH} is referenced to the later $\overline{CAS}$ falling edge.

13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling edge to the $\overline{RAS}$ falling edge.

17. t_{CHR} is referenced to the later $\overline{CAS}$ rising from $\overline{RAS}$ falling edge.

18. t_{DS}, t_{DH} is specified by the earlier $\overline{CAS}$ falling edge.

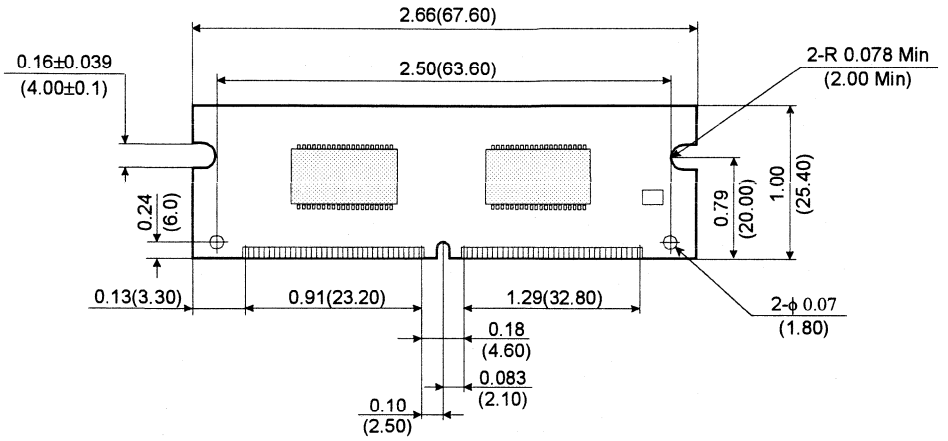
19. If $t_{RASS} \geq 100$us, then $\overline{RAS}$ precharge time must use t_{RPS} instead of t_{RP}.

20. For $\overline{RAS}$-only refresh and burst $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 4096 cycles of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.

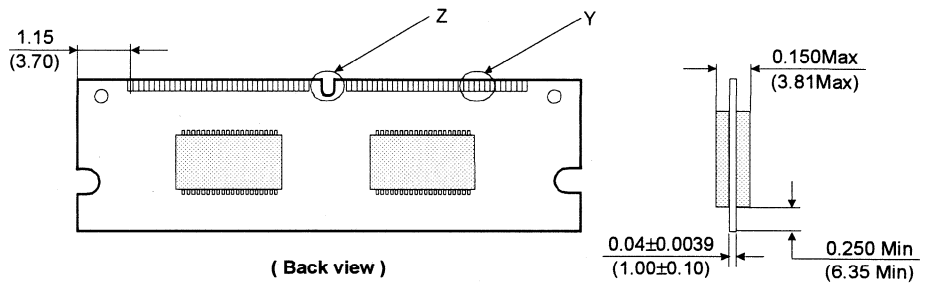
21. For distributed $\overline{CAS}$-before-$\overline{RAS}$ with 15.6us interval $\overline{CAS}$-before-$\overline{RAS}$ should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

PACKAGE DIMENSIONS

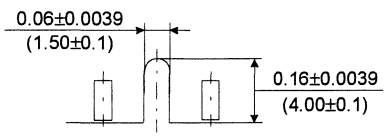
Units : Inches (millimeters)



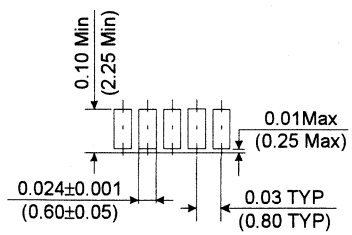
(Front view)



(Back view)



Detail Z



Detail Y

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 DRAM with EDO mode, TSOPII
DRAM Part No. : KM416V4104CS-L

KMM466F803CS2-L EDO Mode

8M x 64 DRAM SODIMM Using 8MX8, 4K Refresh 3.3V, Low power/Self-Refresh

GENERAL DESCRIPTION

The Samsung KMM466F803CS2-L is a 8Mx64bits Dynamic RAM high density memory module. The Samsung KMM466F803CS2-L consists of eight CMOS 8MX8bits DRAMs in TSOP 400mil packages and a 2K EEPROM in 8-pin TSSOP package mounted on a 144-pin glass-epoxy substrate. A 0.1uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM466F803CS2-L is a Small Out-line Dual in-line Memory Module and is intended for mounting into 144 pin edge connector sockets.

FEATURES

- Part Identification
  - KMM466F803CS2-L(4096 cycles/128ms, TSOP, L-ver)
- Extended Data Out Mode Operation
- New JEDEC standard proposal with EEPROM
- Serial Presense Detect with EEPROM
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Self -refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1,100mil), double sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

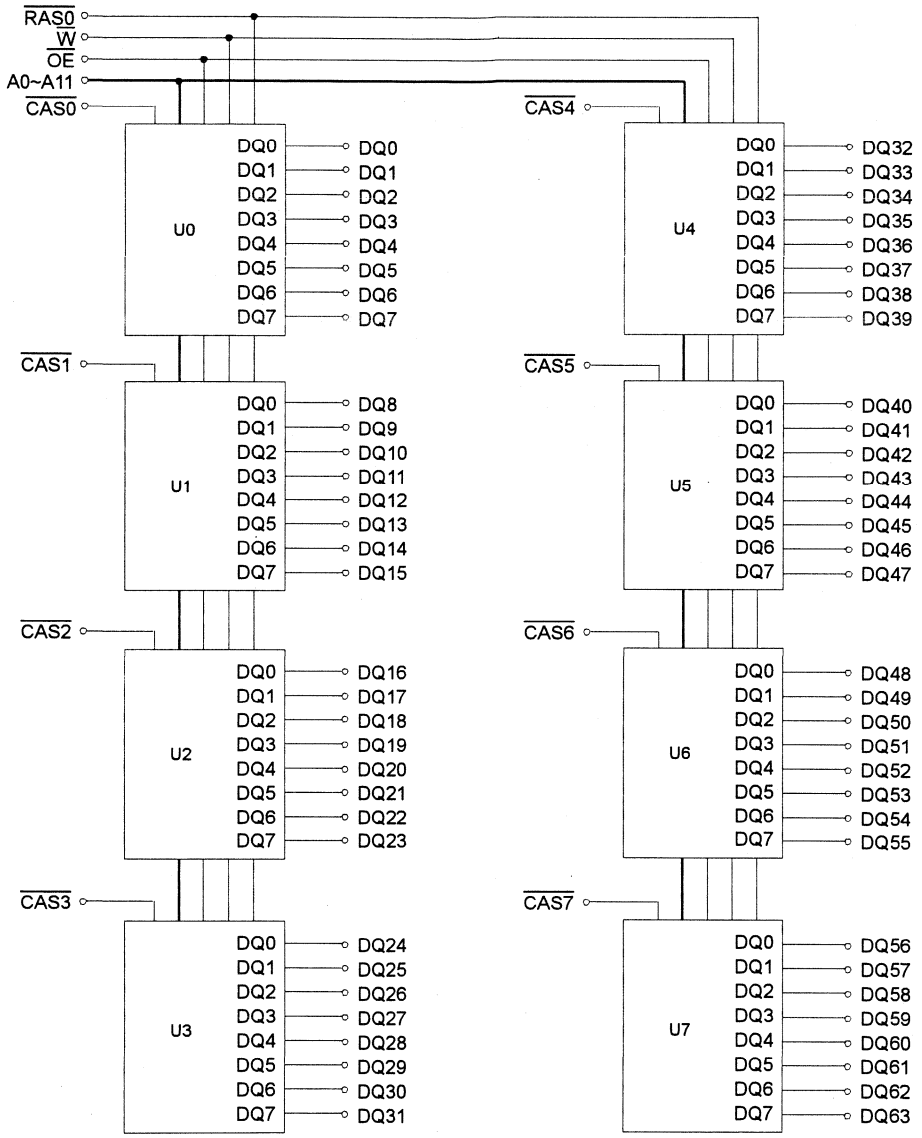
PIN CONFIGURATIONS

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	49	DQ13	50	DQ45	97	DQ22	98	DQ54
3	DQ0	4	DQ32	51	DQ14	52	DQ46	99	DQ23	100	DQ55
5	DQ1	6	DQ33	53	DQ15	54	DQ47	101	Vcc	102	Vcc
7	DQ2	8	DQ34	55	Vss	56	Vss	103	A6	104	A7
9	DQ3	10	DQ35	57	RSVD	58	RSVD	105	A8	106	A11
11	Vcc	12	Vcc	59	RSVD	60	RSVD	107	Vss	108	Vss
13	DQ4	14	DQ36	61	RFU	62	RFU	109	A9	110	NC
15	DQ5	16	DQ37	63	Vcc	64	Vcc	111	A10	112	NC
17	DQ6	18	DQ38	65	RFU	66	RFU	113	Vcc	114	Vcc
19	DQ7	20	DQ39	67	$\overline{W}$	68	RFU	115	$\overline{CAS2}$	116	$\overline{CAS6}$
21	Vss	22	Vss	69	$\overline{RAS0}$	70	RFU	117	$\overline{CAS3}$	118	$\overline{CAS7}$
23	$\overline{CAS0}$	24	$\overline{CAS4}$	71	NC	72	RFU	119	Vss	120	Vss
25	$\overline{CAS1}$	26	$\overline{CAS5}$	73	$\overline{OE}$	74	RFU	121	DQ24	122	DQ56
27	Vcc	28	Vcc	75	Vss	76	Vss	123	DQ25	124	DQ57
29	A0	30	A3	77	RSVD	78	RSVD	125	DQ26	126	DQ58
31	A1	32	A4	79	RSVD	80	RSVD	127	DQ27	128	DQ59
33	A2	34	A5	81	Vcc	82	Vcc	129	Vcc	130	Vcc
35	Vss	36	Vss	83	DQ16	84	DQ48	131	DQ28	132	DQ60
37	DQ8	38	DQ40	85	DQ17	86	DQ49	133	DQ29	134	DQ61
39	DQ9	40	DQ41	87	DQ18	88	DQ50	135	DQ30	136	DQ62
41	DQ10	42	DQ42	89	DQ19	90	DQ51	137	DQ31	138	DQ63
43	DQ11	44	DQ43	91	Vss	92	Vss	139	Vss	140	Vss
45	Vcc	46	Vcc	93	DQ20	94	DQ52	141	SDA	142	SCL
47	DQ12	48	DQ44	95	DQ21	96	DQ53	143	Vcc	144	Vcc

PIN NAMES

Pin Name	Function
A0 to A11	Address Inputs
DQ0 - DQ63	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{OE}$	Output Enable
$\overline{RAS0}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
SDA	Serial Address / Data I/O
SCL	Serial Clock
RSVD	Reserved Use
RFU	Reserved for Future Use

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1: Vcc+1.3V at pulse width≤15ns, which is measured at Vcc.
*2 : -1.3V at pulse width≤15ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM466F803CS2-L		Unit
		Min	Max	
I_{CC1}	-5	-	880	mA
	-6	-	800	mA
I_{CC2}	Don't care	-	8	mA
I_{CC3}	-5	-	880	mA
	-6	-	800	mA
I_{CC4}	-5	-	720	mA
	-6	-	640	mA
I_{CC5}	Don't care	-	1.6	mA
I_{CC6}	-5	-	880	mA
	-6	-	800	mA
I_{CC7}	Don't care	-	2.6	mA
I_{CCS}		-	2.6	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)
I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})
I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)
I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)
I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)
I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)
I_{CC7} : Battery back-up current. Average power supply, Battery back-up mode.
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=0.2V,
DQ=Don't care, t_{RC}=31.25us, t_{RAS}=t_{RAS}min~300ns
I_{CCS} : Self Refresh Current, $\overline{RAS}$=$\overline{CAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0~A11=Vcc-0.2V or 0.2V, DQ~DQ63=Vcc-0.2V or Open
$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)
$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)
V_{OH} : Output High Voltage Level (I_{OH} = -2mA)
V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	50	pF
Input capacitance[$\overline{W}$, $\overline{OE}$]	C_{IN2}	-	66	pF
Input capacitance[$\overline{RAS0}$]	C_{IN3}	-	66	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	17	pF
Input/Output capacitance[DQ0 - 63]	C_{DQ}	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	128		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,9
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,9
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	3,11
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	8		10		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		40		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	17	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	12	25	15	30	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	7		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	7		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	7
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	7
Write command set-up time	t_{WCS}	0		0		ns	6
Write command hold time	t_{WCH}	7		10		ns	6
Write command pulse width	t_{WP}	7		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	8		10		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	7		10		ns	
Data set-up time	t_{DS}	0		0		ns	8
Data hold time	t_{DH}	7		10		ns	8
Refresh period	t_{REF}		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	33		38		ns	6
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	70		84		ns	6

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.2/0.7V$, $V_{oh}/V_{ol}=2.0/0.8V$, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	45		53		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	47		58		ns	6
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3
Hyper page mode cycle time	t_{HPC}	20		25		ns	10
Hyper page mode read-modify write cycle time	t_{HPRWC}	67		73		ns	10
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	7		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time (C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time (C-B-R refresh)	t_{WRH}	10		10		ns	
$\overline{OE}$ access time	t_{OEA}		13		15	ns	3
$\overline{OE}$ to data delay	t_{OED}	10		13		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	13	3	13	ns	
$\overline{OE}$ command hold time	t_{OEH}	5		5		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	13	ns	11
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	13	ns	
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	
$\overline{RAS}$ pulse width (C-B-R self refresh)	t_{RASS}	100		100		us	12,13,14
$\overline{RAS}$ precharge time (C-B-R self refresh)	t_{RPS}	90		110		ns	12,13,14
$\overline{CAS}$ hold time (C-B-R self refresh)	t_{CHS}	-50		-50		ns	12,13,14

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are non-restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

7. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

8. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

9. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit access time is controlled by t_{AA}.

10. $t_{ASC} \geq 6$ns, Assume t_T=2.0ns

11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

12. If $t_{RASS} \geq 100$us, then $\overline{RAS}$ precharge time must use t_{RPS} instead of t_{RP}.

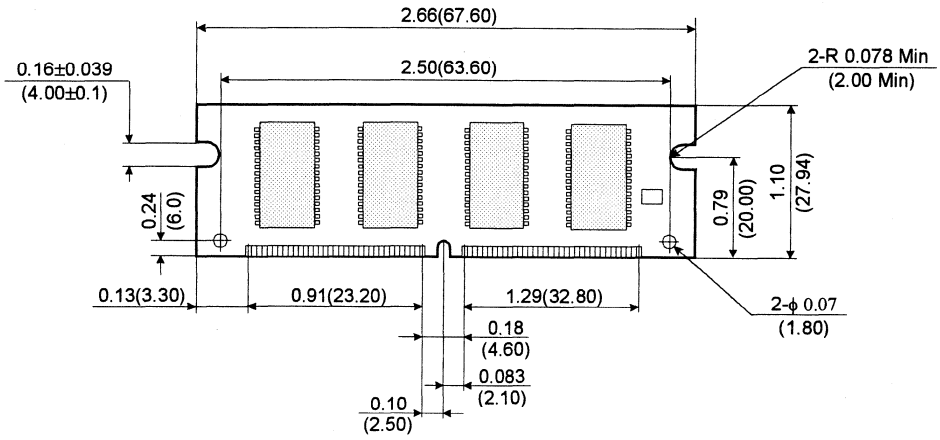
13. For $\overline{RAS}$-only refresh and burst $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 4096 cycles of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.

14. For distributed $\overline{CAS}$-before-$\overline{RAS}$ with 15.6us interval $\overline{CAS}$-before-$\overline{RAS}$ should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

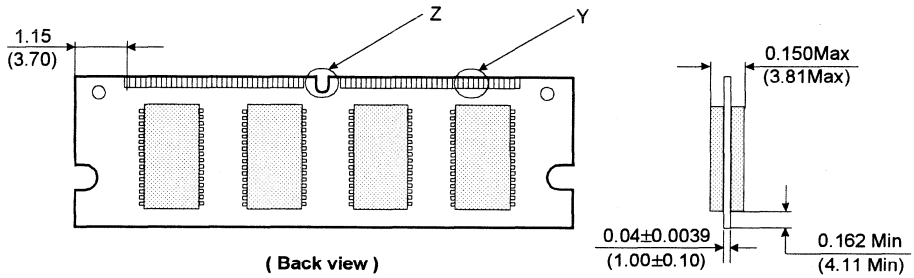
3

PACKAGE DIMENSIONS

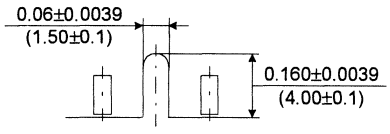
Units : Inches (millimeters)



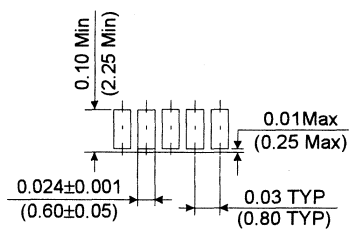
(Front view)



(Back view)



Detail Z



Detail Y

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8MX8 DRAM with EDO mode, TSOPII
DRAM Part No. : KM48V8104CS-L

KMM466F804CS1-L EDO Mode

8M x 64 DRAM SODIMM Using 4Mx16, 4K Refresh 3.3V, Low power/Self-Refresh

GENERAL DESCRIPTION

The Samsung KMM466F804CS1-L is a 8Mx64bits Dynamic RAM high density memory module. The Samsung KMM466F804CS1-L consists of eight CMOS 4Mx16bits DRAMs in TSOP 400mil packages and a 2K EEPROM in 8-pin TSSOP package mounted on a 144-pin glass-epoxy substrate. A 0.1uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM466F804CS1-L is a Small Out-line Dual in-line Memory Module and is intended for mounting into 144 pin edge connector sockets.

FEATURES

- Part Identification
  - KMM466F804CS1-L(4096 cycles/128ms, TSOP, L-ver)
- Extended Data Out Mode Operation
- New JEDEC standard proposal with EEPROM
- Serial Presense Detect with EEPROM
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Self -refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), double sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

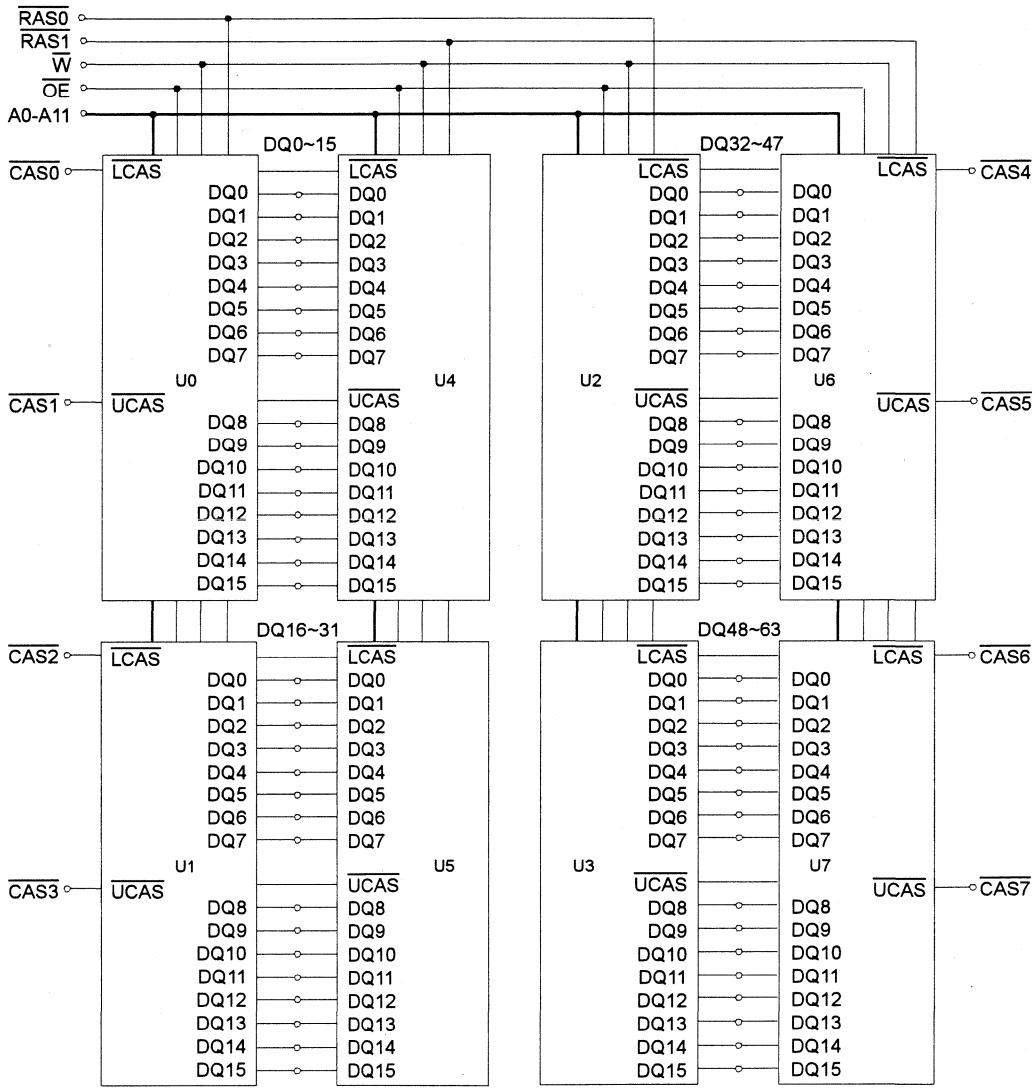
PIN CONFIGURATIONS

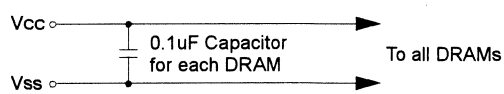
Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	49	DQ13	50	DQ45	97	DQ22	98	DQ54
3	DQ0	4	DQ32	51	DQ14	52	DQ46	99	DQ23	100	DQ55
5	DQ1	6	DQ33	53	DQ15	54	DQ47	101	Vcc	102	Vcc
7	DQ2	8	DQ34	55	Vss	56	Vss	103	A6	104	A7
9	DQ3	10	DQ35	57	RSVD	58	RSVD	105	A8	106	A11
11	Vcc	12	Vcc	59	RSVD	60	RSVD	107	Vss	108	Vss
13	DQ4	14	DQ36	61	RFU	62	RFU	109	A9	110	NC
15	DQ5	16	DQ37	63	Vcc	64	Vcc	111	A10	112	NC
17	DQ6	18	DQ38	65	RFU	66	RFU	113	Vcc	114	Vcc
19	DQ7	20	DQ39	67	$\overline{W}$	68	RFU	115	$\overline{CAS2}$	116	$\overline{CAS6}$
21	Vss	22	Vss	69	$\overline{RAS0}$	70	RFU	117	$\overline{CAS3}$	118	$\overline{CAS7}$
23	$\overline{CAS0}$	24	$\overline{CAS4}$	71	$\overline{RAS1}$	72	RFU	119	Vss	120	Vss
25	$\overline{CAS1}$	26	$\overline{CAS5}$	73	$\overline{OE}$	74	RFU	121	DQ24	122	DQ56
27	Vcc	28	Vcc	75	Vss	76	Vss	123	DQ25	124	DQ57
29	A0	30	A3	77	RSVD	78	RSVD	125	DQ26	126	DQ58
31	A1	32	A4	79	RSVD	80	RSVD	127	DQ27	128	DQ59
33	A2	34	A5	81	Vcc	82	Vcc	129	Vcc	130	Vcc
35	Vss	36	Vss	83	DQ16	84	DQ48	131	DQ28	132	DQ60
37	DQ8	38	DQ40	85	DQ17	86	DQ49	133	DQ29	134	DQ61
39	DQ9	40	DQ41	87	DQ18	88	DQ50	135	DQ30	136	DQ62
41	DQ10	42	DQ42	89	DQ19	90	DQ51	137	DQ31	138	DQ63
43	DQ11	44	DQ43	91	Vss	92	Vss	139	Vss	140	Vss
45	Vcc	46	Vcc	93	DQ20	94	DQ52	141	SDA	142	SCL
47	DQ12	48	DQ44	95	DQ21	96	DQ53	143	Vcc	144	Vcc

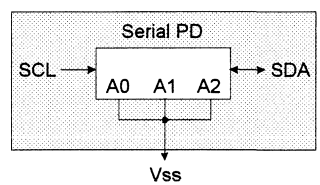
PIN NAMES

Pin Name	Function
A0 to A11	Address Inputs
DQ0 - DQ63	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{OE}$	Output Enable
$\overline{RAS0}$, $\overline{RAS1}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
SDA	Serial Address / Data I/O
SCL	Serial Clock
RSVD	Reserved Use
RFU	Reserved for Future Use

FUNCTIONAL BLOCK DIAGRAM







ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width≤15ns, which is measured at Vcc.
*2 : -1.3V at pulse width≤15ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM466F804CS1-L		Unit
		Min	Max	
I_{CC1}	-5 -6	- -	484 444	mA mA
I_{CC2}	Don't care	-	8	mA
I_{CC3}	-5 -6	- -	484 444	mA mA
I_{CC4}	-5 -6	- -	364 324	mA mA
I_{CC5}	Don't care	-	1.6	mA
I_{CC6}	-5 -6	- -	484 444	mA mA
I_{CC7} I_{CCS}	Don't care	- -	2.8 2.8	mA mA
$I_{I(L)}$ $I_{O(L)}$	Don't care	-10 -10	10 10	uA uA
V_{OH} V_{OL}	Don't care	2.4 -	- 0.4	V V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)
I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})
I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)
I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)
I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)
I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)
I_{CC7} : Battery back-up current. Average power supply, Battery back-up mode.
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$,$\overline{LCAS}$=0.2V,
DQ=Don't care, t_{RC}=31.25us, t_{RAS}=t_{RAS}min~300ns
I_{CCS} : Self Refresh Current, $\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0~A11=Vcc-0.2V or 0.2V, DQ~DQ63=Vcc-0.2V or Open
$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)
$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)
V_{OH} : Output High Voltage Level (I_{OH} = -2mA)
V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	50	pF
Input capacitance[$\overline{W}$, $\overline{OE}$]	C_{IN2}	-	66	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS1}$]	C_{IN3}	-	38	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	24	pF
Input/Output capacitance[DQ0 - 63]	C_{DQ}	-	24	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	128		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,9
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,9
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	3,11
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	8		10		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		40		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	17	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	12	25	15	30	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	7		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	12
Column address hold time	t_{CAH}	7		10		ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	7
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	7
Write command set-up time	t_{WCS}	0		0		ns	6
Write command hold time	t_{WCH}	7		10		ns	6
Write command pulse width	t_{WP}	7		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	8		10		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	7		10		ns	15
Data set-up time	t_{DS}	0		0		ns	8,18
Data hold time	t_{DH}	7		10		ns	8,18
Refresh period	t_{REF}		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ dealy time	t_{CWD}	33		38		ns	6,14
$\overline{RAS}$ to $\overline{W}$ dealy time	t_{RWD}	70		84		ns	6

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.2/0.7V$, $V_{oh}/V_{ol}=2.0/0.8V$, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	45		53		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	47		58		ns	6
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	16
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	17
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3
Hyper page mode cycle time	t_{HPC}	20		25		ns	10
Hyper page mode read-modify write cycle time	t_{HPRWC}	67		73		ns	10
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	7		10		ns	13
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time (C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time (C-B-R refresh)	t_{WRH}	10		10		ns	
$\overline{OE}$ access time	t_{OEA}		13		15	ns	3
$\overline{OE}$ to data delay	t_{OED}	10		13		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	13	3	13	ns	
$\overline{OE}$ command hold time	t_{OEH}	5		5		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	11
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width(Hyper page cycle)	t_{WPE}	5		5		ns	
$\overline{RAS}$ pulse width (C-B-R self refresh)	t_{RASS}	100		100		us	19,20,21
$\overline{RAS}$ precharge time (C-B-R self refresh)	t_{RPS}	90		110		ns	19,20,21
$\overline{CAS}$ hold time (C-B-R self refresh)	t_{CHS}	-50		-50		ns	19,20,21

3

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are non-restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

7. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

8. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

9. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit access time is controlled by t_{AA}.

10. $t_{ASC} \geq 6$ns, Assume tT=2.0ns

11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

12. t_{ASC} is referenced to the earlier $\overline{CAS}$ falling edge and t_{CAH} is referenced to the later $\overline{CAS}$ falling edge.

13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling edge to the $\overline{RAS}$ falling edge.

17. t_{CHR} is referenced to the later $\overline{CAS}$ rising from $\overline{RAS}$ falling edge.

18. t_{DS}, t_{DH} is specified by the earlier $\overline{CAS}$ falling edge.

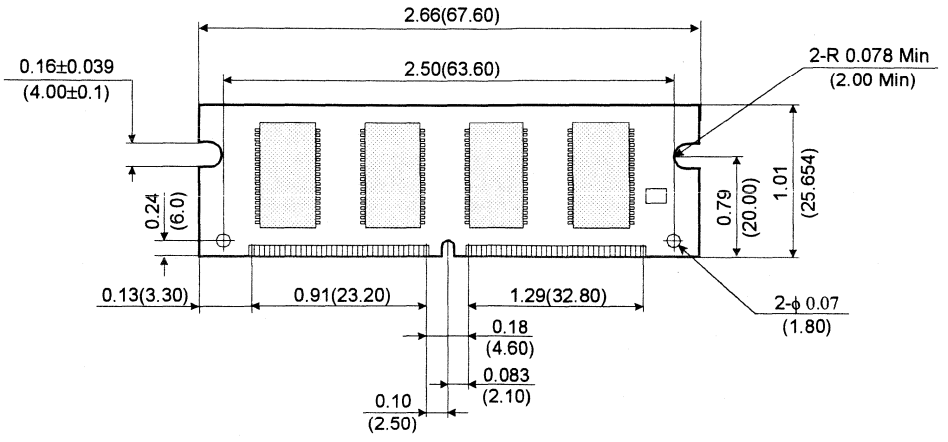
19. If $t_{RASS} \geq 100$us, then $\overline{RAS}$ precharge time must use t_{RPS} instead of t_{RP}.

20. For $\overline{RAS}$-only refresh and burst $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 4096 cycles of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.

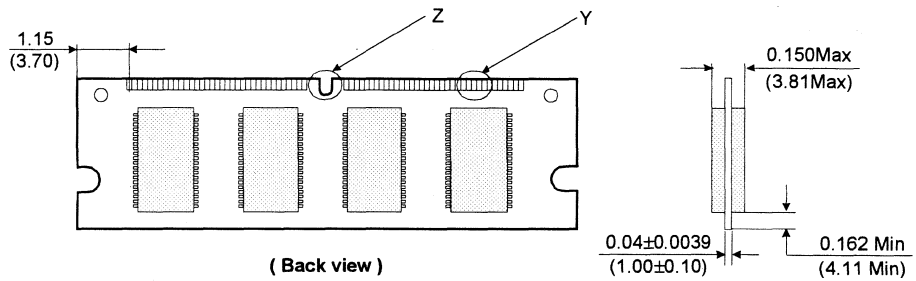
21. For distributed $\overline{CAS}$-before-$\overline{RAS}$ with 15.6us interval $\overline{CAS}$-before-$\overline{RAS}$ should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

PACKAGE DIMENSIONS

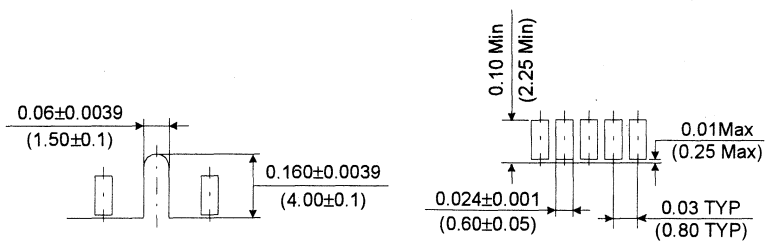
Units : Inches (millimeters)



(Front view)



(Back view)

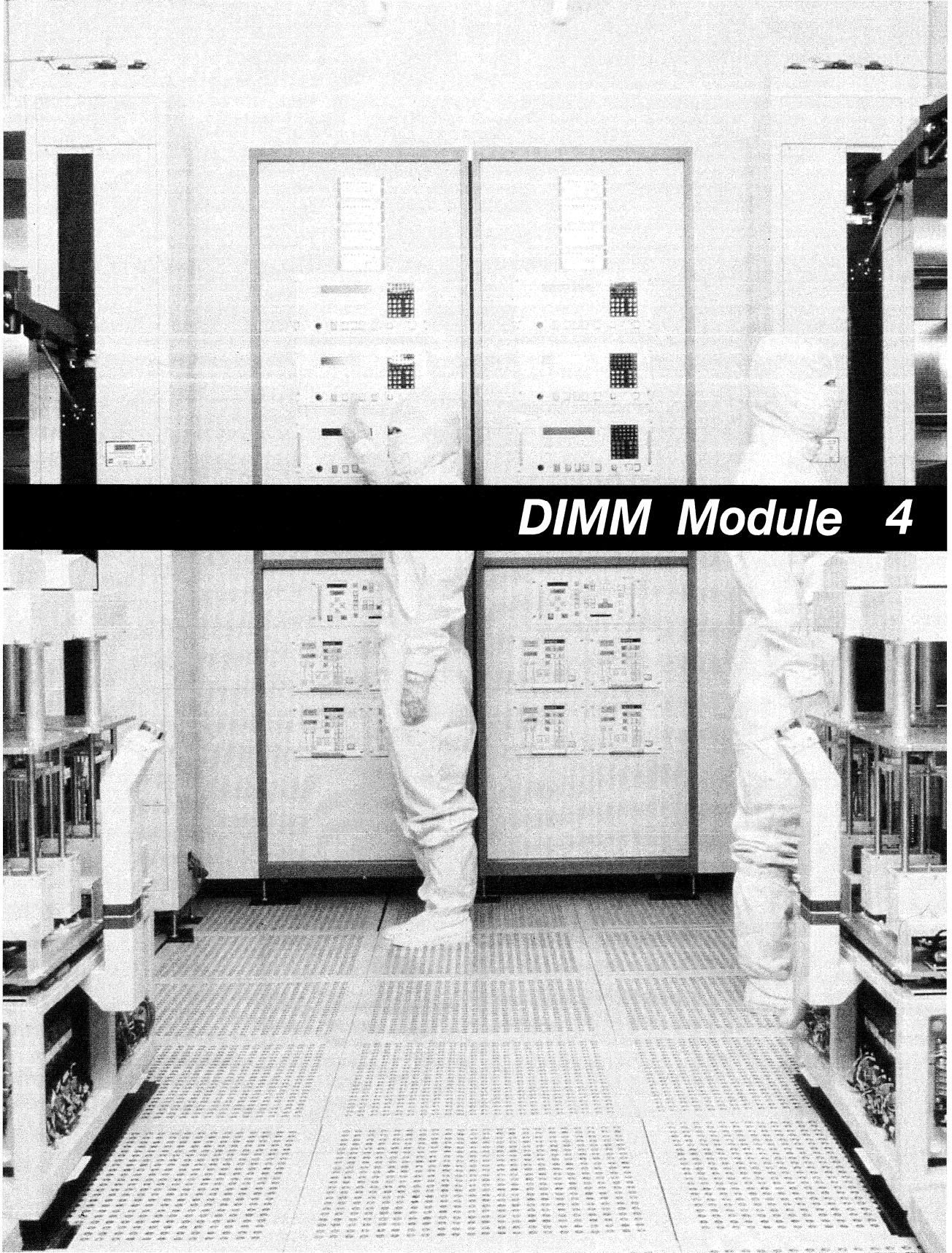


Detail Z **Detail Y**

Tolerances : ±.005(.13) unless otherwise specified

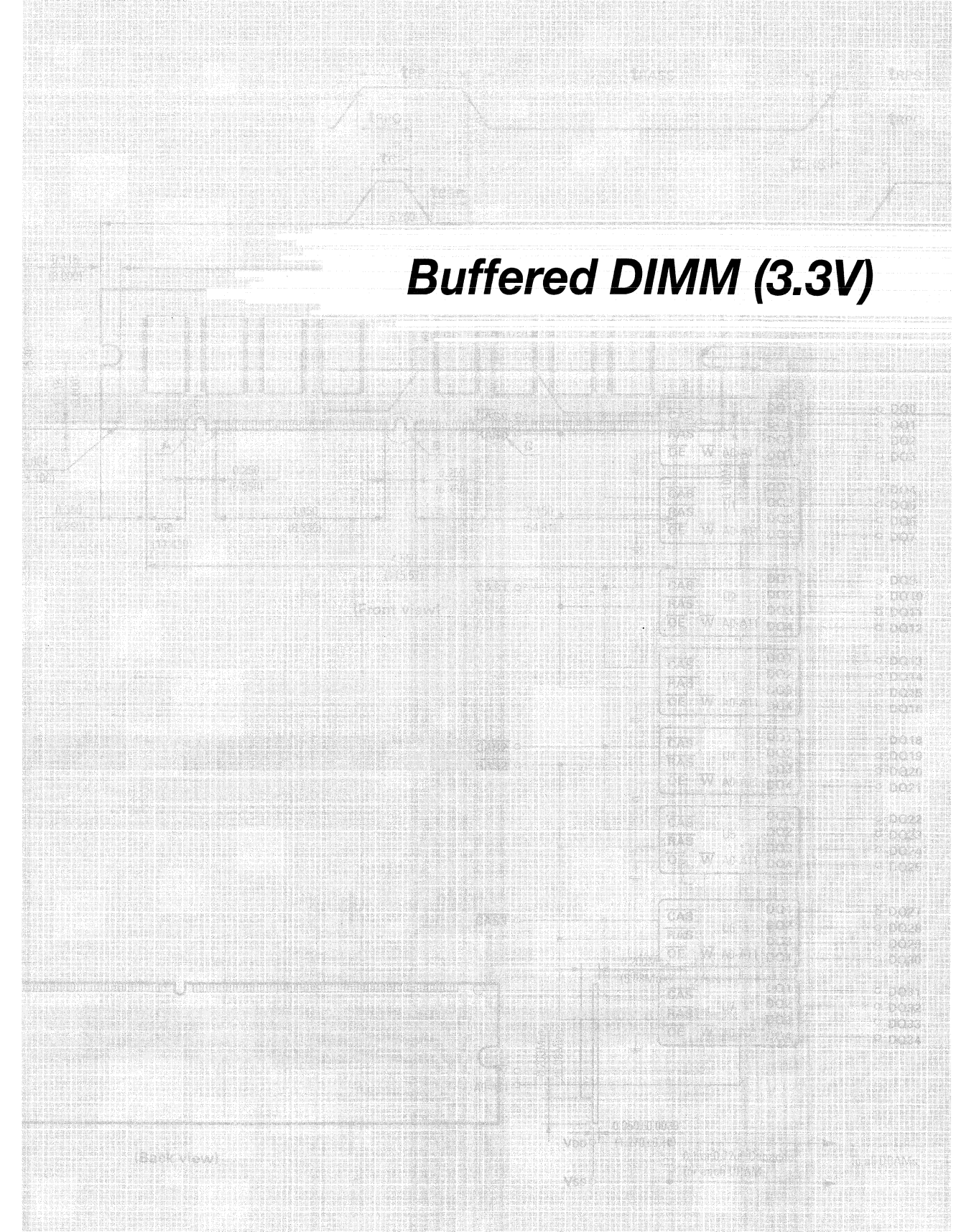
The used device is 4Mx16 DRAM with EDO mode, TSOP II
DRAM Part No. : KM416V4104CS-L

NOTES



DIMM Module 4

Buffered DIMM (3.3V)



KMM372V124CT with Fast Page Mode

1M x 72 DRAM DIMM with ECC using 1Mx16 & 1Mx4, 1K Refresh , 3.3V

GENERAL DESCRIPTION

The Samsung KMM372V124CT is a 1Mx72bits Dynamic RAM high density memory module. The Samsung KMM372V124CT consists of four CMOS 1Mx16bits DRAMs in TSOP-II 400mil package, two CMOS 1Mx4bits DRAMs in TSOP-II 300mil package and two 16bits driver IC in 48pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372V124CT is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-6	60ns	20ns	110ns	40ns

FEATURES

- Part Identification
  - KMM372V124CT (1024 cycles/16ms Ref. TSOP-II)
- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), Single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{RSVD}$	57	DQ22	85	Vss	113	$\overline{RSVD}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	*A10	66	DQ26	94	DQ43	122	*A11	150	DQ62
11	DQ8	39	*A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	*$\overline{CAS5}$	158	DQ68
19	DQ14	47	RSVD	75	DQ33	103	DQ50	131	RSVD	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	*$\overline{CAS1}$	140	DQ57	168	Vcc

PD Note : PD & ID Terminals must each be pulled up through a resister to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A9	Address Input
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future

Pins marked '*' are not used in this module.

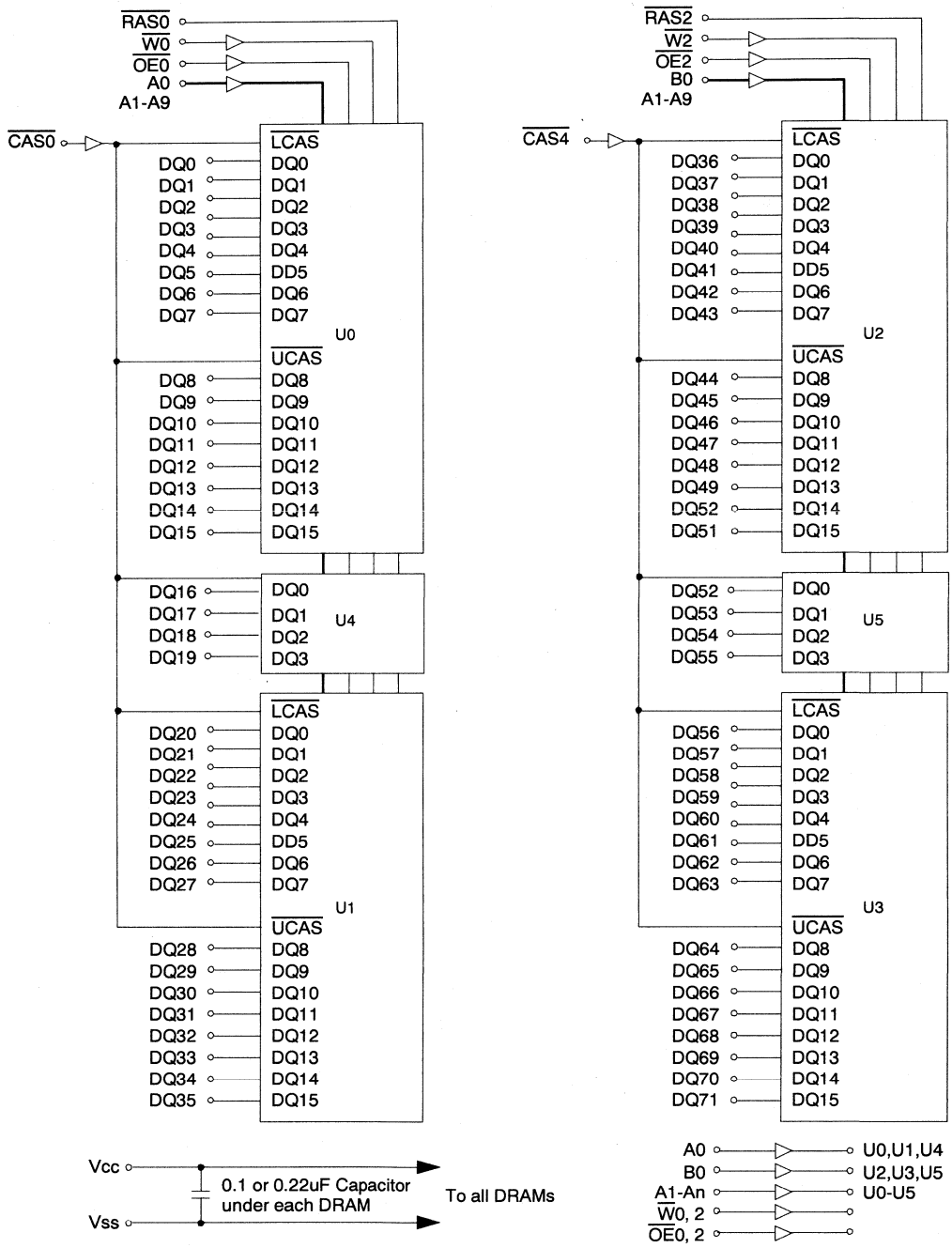
PD & ID Table

Pin	60NS	70NS
PD1	0	0
PD2	0	0
PD3	1	1
PD4	0	0
PD5	0	0
PD6	1	0
PD7	1	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	5.2	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V/15ns, Pulse width is measured at V_{CC}.
*2 : -1.3V/15ns, Pulse width is is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372V124CT		Unit
		Min	Max	
I_{CC1}	-6	-	740	mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-6	-	740	mA
I_{CC4}	-6	-	510	mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-6	-	740	mA
$I_{I(L)}$ $I_{O(L)}$	Don't care	-15 -5	15 5	uA uA
V_{OH} V_{OL}	Don't care	2.4 -	- 0.4	V V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)
I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})
I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)
I_{CC4}*: Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)
I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)
I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)
$I_{I(L)}$: Input Leakage Current (Any input 0≤ V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)
$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V≤ V_{OUT}≤Vcc)
V_{OH} : Output High Voltage Level (I_{OH} = -2mA)
V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

*** NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one page mode cycle, t_{PC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A9, B0]	C_{IN1}	-	15	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	17	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	31	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS4}$]	C_{IN4}	-	17	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ1}	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, Output loading CL=100pF

Parameter	Symbol	-6		Unit	Note
		Min	Max		
Random read or write cycle time	t_{RC}	110		ns	
Read-modify-write cycle time	t_{RWC}	155		ns	
Access time from $\overline{RAS}$	t_{RAC}		60	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		20	ns	3,4,5,11
Access time from column address	t_{AA}		35	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		ns	3,11
Output buffer turn-off delay	t_{OFF}	5	20	ns	6,11
Transition time(rise and fall)	t_T	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		ns	11
$\overline{CAS}$ hold time	t_{CSH}	58		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	40	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	13	25	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		ns	11
Row address set-up time	t_{ASR}	5		ns	11
Row address hold time	t_{RAH}	8		ns	11
Column address set-up time	t_{ASC}	0		ns	
Column address hold time	t_{CAH}	10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		ns	11
Read command set-up time	t_{RCS}	0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		ns	8,11
Write command hold time	t_{WCH}	10		ns	
Write command pulse width	t_{WP}	10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		ns	
Data set-up time	t_{DS}	-2		ns	9,11
Data hold time	t_{DH}	20		ns	9,11
Refresh period	t_{REF}		16	ms	
Write command set-up time	t_{WCS}	0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	55		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	60		ns	7

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Parameter	Symbol	-6		Unit	Note
		Min	Max		
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	83		ns	7,11
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		ns	11
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		ns	11
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	3		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		40	ns	3,11
Fast page mode cycle time	t_{PC}	40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	80		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	t_{RASP}	60	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	15		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	8		ns	11
$\overline{OE}$ access time	t_{OEA}		20	ns	
$\overline{OE}$ to data delay	t_{OED}	20		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	20	ns	11
$\overline{OE}$ command hold time	t_{OEH}	15		ns	11
Present Detect Read Cycle					
$\overline{PDE}$ to Valid PD bit	t_{PD}		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS} is not restrictive operating parameter. It included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

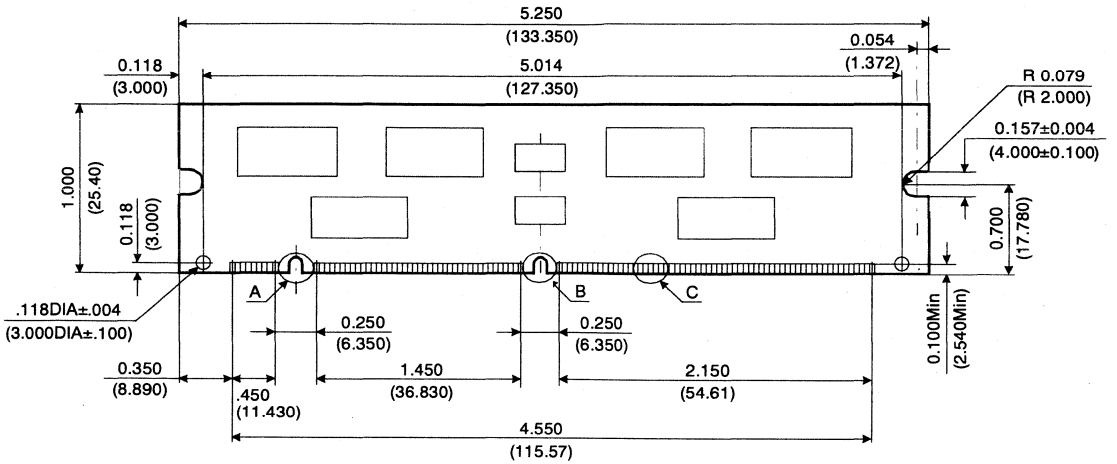
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

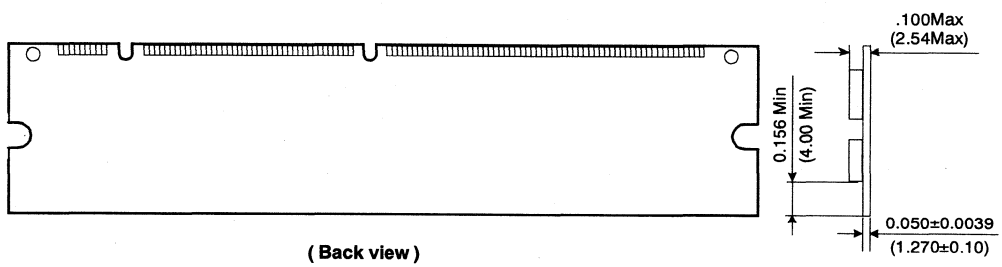
11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

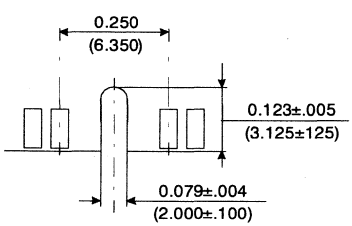
Units : Inches (millimeters)



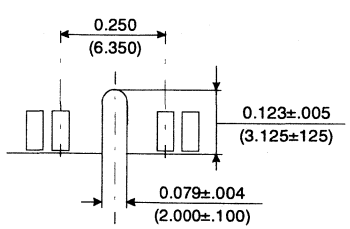
(Front view)



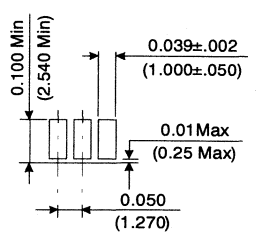
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 1Mx16 DRAM with FP mode, TSOP and 1Mx4 DRAM with FP mode, TSOP.
DRAM Part No. : KMM372V124CT - KM416V1200CT and KM44V1000DT

KMM372F124CT EDO Mode

1M x 72 DRAM DIMM with ECC using 1Mx16 & 1Mx4, 1K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM372F124CT is a 1Mx72bits Dynamic RAM high density memory module. The Samsung KMM372F124CT consists of four CMOS 1Mx16bits DRAMs in TSOP-II 400mil package, two CMOS 1Mx4bit DRAMs in TSOP-II 300mil package and two 16bits driver IC in 48pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372F124CT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

FEATURES

- Part Identification
  - KMM372F124CT (1024 cycles/16ms Ref., TSOP-II)
- Fast Page Mode with Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), Single sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-6	60ns	22ns	104ns	25ns

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{RSVD}$	57	DQ22	85	Vss	113	$\overline{RSVD}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	*A10	66	DQ26	94	DQ43	122	*A11	150	DQ62
11	DQ8	39	*A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	*$\overline{CAS5}$	158	DQ68
19	DQ14	47	$\overline{RSVD}$	75	DQ33	103	DQ50	131	$\overline{RSVD}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	$\overline{RFU}$	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	*$\overline{CAS1}$	140	DQ57	168	Vcc

PIN NAMES

Pin Names	Function
A0, B0, A1 - A9	Address Input
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

PD & ID Table

Pin	60NS	70NS
PD1	0	0
PD2	0	0
PD3	1	1
PD4	0	0
PD5	1	1
PD6	1	0
PD7	1	1
PD8	0	0
ID0	0	0
ID1	0	0

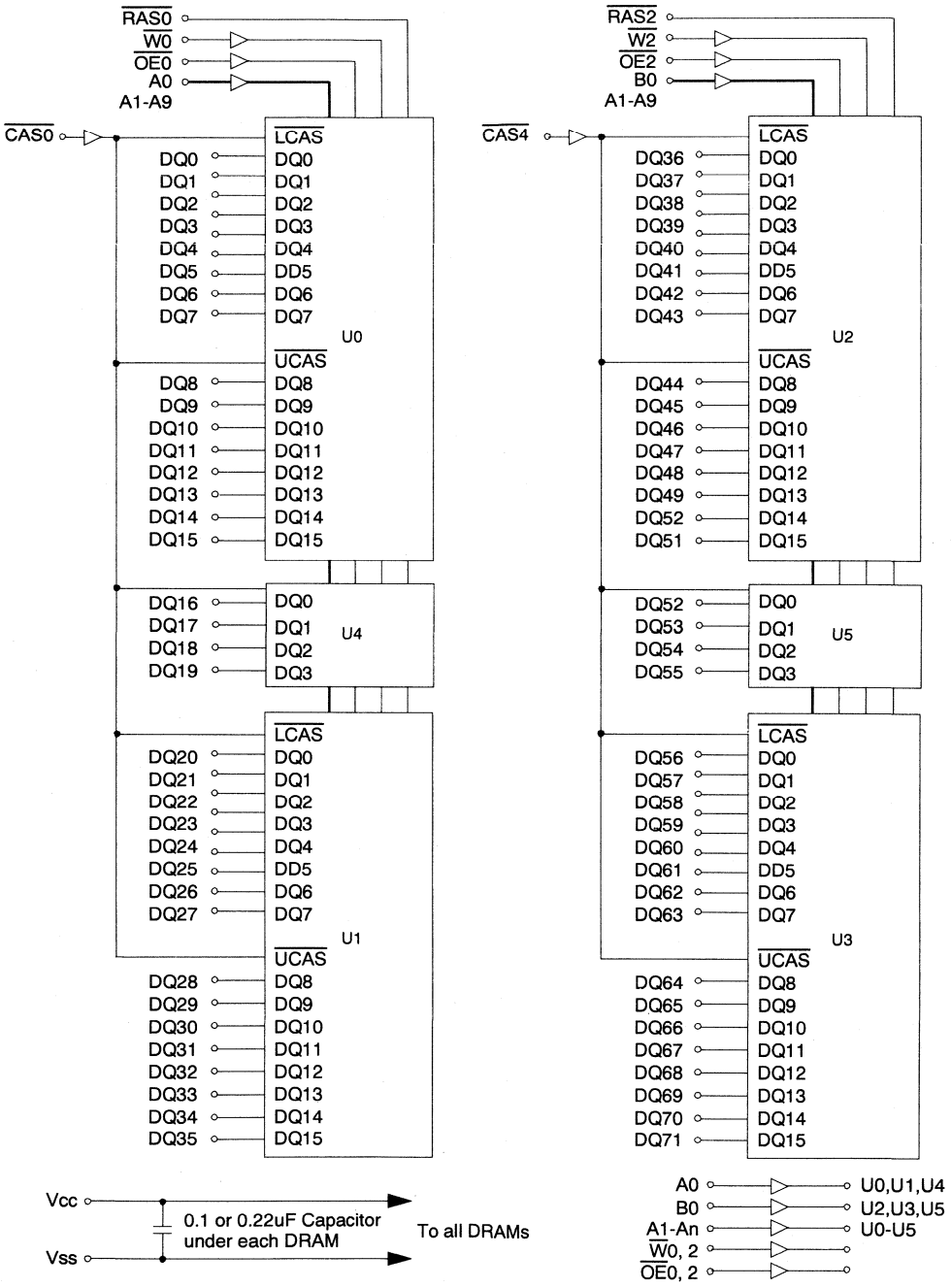
PD Note : PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vssvia on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	5.2	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V/15ns, Pulse width is measured at V_{CC}.

*2 : -1.3V/15ns, Pulse width is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372F124CT		Unit
		Min	Max	
I_{CC1}	-6	-	740	mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-6	-	740	mA
I_{CC4}	-6	-	580	mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-6	-	740	mA
$I_{I(L)}$ $I_{O(L)}$	Don't care	-15 -5	15 5	uA uA
V_{OH} V_{OL}	Don't care	2.4 -	- 0.4	V V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: EDO Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{I(L)}$: Input Leakage Current (Any input 0≤ V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)

$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V≤ V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page mode cycle, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A9, B0]	C_{IN1}	-	15	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	17	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	31	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS4}$]	C_{IN4}	-	17	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ1}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, Output loading CL=100pF

Parameter	Symbol	-6		Unit	Note
		Min	Max		
Random read or write cycle time	t_{RC}	104		ns	
Read-modify-write cycle time	t_{RWC}	155		ns	
Access time from $\overline{RAS}$	t_{RAC}		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		22	ns	3,4,5,14
Access time from column address	t_{AA}		35	ns	3,10,14
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		ns	3,14
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		ns	3,14
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	20	ns	6,11,12,14
Transition time(rise and fall)	t_T	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		ns	14
$\overline{CAS}$ hold time	t_{CSH}	48		ns	14
$\overline{CAS}$ pulse width	t_{CAS}	10	10K	ns	13
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	40	ns	4,14
$\overline{RAS}$ to column address delay time	t_{RAD}	13	25	ns	10,14
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		ns	14
Row address set-up time	t_{ASR}	5		ns	14
Row address hold time	t_{RAH}	8		ns	14
Column address set-up time	t_{ASC}	0		ns	
Column address hold time	t_{CAH}	10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		ns	14
Read command set-up time	t_{RCS}	0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		ns	8,14
Write command hold time	t_{WCH}	10		ns	
Write command pulse width	t_{WP}	10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		ns	14
Write command to $\overline{CAS}$ lead time	t_{CWL}	10		ns	
Data set-up time	t_{DS}	-2		ns	9,14
Data hold time	t_{DH}	15		ns	9,14
Refresh period(1K Ref.)	t_{REF}		16	ms	
Write command set-up time	t_{WCS}	0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	83		ns	7,14

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Parameter	Symbol	-6		Unit	Note
		Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	55		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	60		ns	
$\overline{CAS}$ set-up time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		ns	14
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		ns	14
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		ns	14
Access time from $\overline{CAS}$ precharge	t_{CPA}		40	ns	3,14
Hyper page cycle time	t_{HPC}	25		ns	13
Hyper page read-modify-write cycle time	t_{HPRWC}	79		ns	13
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		ns	14
$\overline{OE}$ access time	t_{OEA}		20	ns	14
$\overline{OE}$ to data delay	t_{OED}	20		ns	14
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	20	ns	6,11,14
$\overline{OE}$ command hold time	t_{OEH}	15		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		ns	14
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		ns	14
Output data hold time	t_{DOH}	10		ns	14
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	15	ns	6,11,12
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	3	20	ns	6,11,14
$\overline{W}$ to data delay	t_{WED}	20		ns	14
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		ns	
$\overline{W}$ pulse width(Hyper page cycle)	t_{WPE}	5		ns	
Present Detect Read Cycle					
$\overline{PDE}$ to Valid PD bit	t_{PD}		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF. Voh=2.0V and Vol=0.8V.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

   If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data output will contain data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out(at access time) is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. t_{CEZ}(max), t_{REZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ high going.

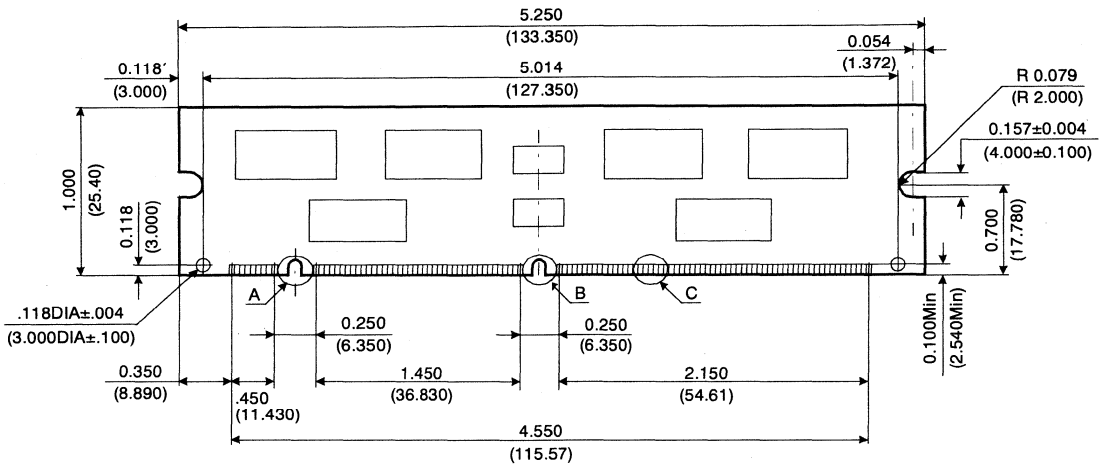
13. $t_{ASC} \geq t_{CP}$ min

14. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

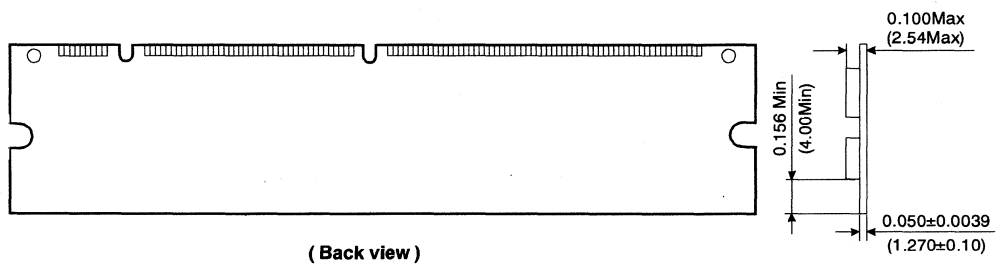
4

PACKAGE DIMENSIONS

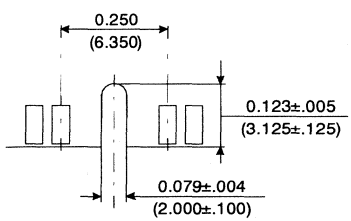
Units : Inches (millimeters)



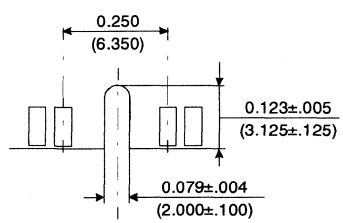
(Front view)



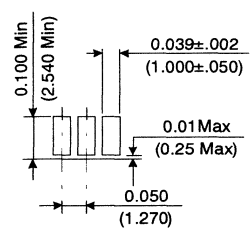
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 1Mx16 DRAM with EDO mode, TSOP and 1Mx4 DRAM with EDO mode,TSOP.
DRAM Part No. : KMM372F124CT - KM416V1204CT and KM44V1004DT

KMM372F124BJ EDO Mode

1M x 72 DRAM DIMM with ECC using 1Mx16 & 1Mx4, 1K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM372F124CJ is a 1Mx72bits Dynamic RAM high density memory module. The Samsung KMM372F124CJ consists of four CMOS 1Mx16bits DRAMs in SOJ 400mil package, two CMOS 1Mx4bit DRAMs in SOJ 300mil package and two 16bits driver IC in 48pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372F124CJ is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-6	60ns	22ns	104ns	25ns

FEATURES

- Part Identification
  - KMM372F124CJ (1024 cycles/16ms Ref., SOJ)
- Fast Page Mode with Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), Single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{RSVD}$	57	DQ22	85	Vss	113	$\overline{RSVD}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	*A10	66	DQ26	94	DQ43	122	*A11	150	DQ62
11	DQ8	39	*A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	$\overline{Vss}$	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	$\overline{RFU}$	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	*$\overline{CAS5}$	158	DQ68
19	DQ14	47	$\overline{RSVD}$	75	DQ33	103	DQ50	131	$\overline{RSVD}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	$\overline{Vcc}$	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	$\overline{RFU}$	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	*$\overline{CAS1}$	140	DQ57	168	Vcc

PD Note : PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vssvia on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A9	Address Input
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

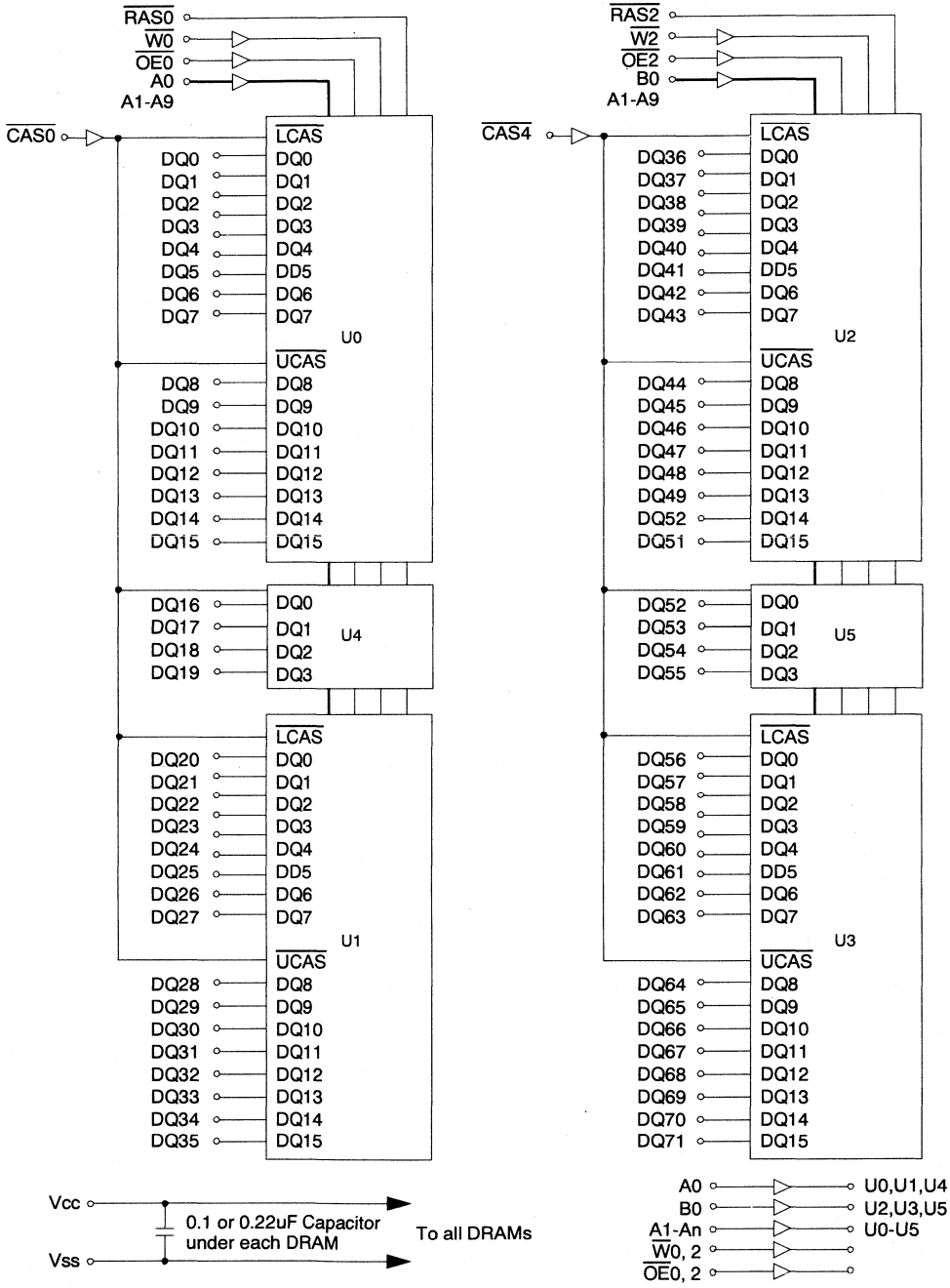
PD & ID Table

Pin	60NS	70NS
PD1	0	0
PD2	0	0
PD3	1	1
PD4	0	0
PD5	1	1
PD6	1	0
PD7	1	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	5.2	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V/15ns, Pulse width is measured at V_{CC}.

*2 : -1.3V/15ns, Pulse width is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372F124CJ		Unit
		Min	Max	
I_{CC1}	-6	-	740	mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-6	-	740	mA
I_{CC4}	-6	-	580	mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-6	-	740	mA
$I_{I(L)}$ $I_{O(L)}$	Don't care	-15 -5	15 5	uA uA
V_{OH} V_{OL}	Don't care	2.4 -	- 0.4	V V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: EDO Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{I(L)}$: Input Leakage Current (Any input 0≤ V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)

$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V≤ V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

*** NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page mode cycle, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A9, B0]	C_{IN1}	-	15	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	17	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	31	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS4}$]	C_{IN4}	-	17	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ1}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, Output loading CL=100pF

Parameter	Symbol	-6		Unit	Note
		Min	Max		
Random read or write cycle time	t_{RC}	104		ns	
Read-modify-write cycle time	t_{RWC}	155		ns	
Access time from $\overline{RAS}$	t_{RAC}		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		22	ns	3,4,5,14
Access time from column address	t_{AA}		35	ns	3,10,14
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		ns	3,14
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		ns	3,14
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	20	ns	6,11,12,14
Transition time(rise and fall)	t_T	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		ns	14
$\overline{CAS}$ hold time	t_{CSH}	48		ns	14
$\overline{CAS}$ pulse width	t_{CAS}	10	10K	ns	13
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	40	ns	4,14
$\overline{RAS}$ to column address delay time	t_{RAD}	13	25	ns	10,14
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		ns	14
Row address set-up time	t_{ASR}	5		ns	14
Row address hold time	t_{RAH}	8		ns	14
Column address set-up time	t_{ASC}	0		ns	
Column address hold time	t_{CAH}	10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		ns	14
Read command set-up time	t_{RCS}	0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		ns	8,14
Write command hold time	t_{WCH}	10		ns	
Write command pulse width	t_{WP}	10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		ns	14
Write command to $\overline{CAS}$ lead time	t_{CWL}	10		ns	
Data set-up time	t_{DS}	-2		ns	9,14
Data hold time	t_{DH}	15		ns	9,14
Refresh period(1K Ref.)	t_{REF}		16	ms	
Write command set-up time	t_{WCS}	0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	83		ns	7,14

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Parameter	Symbol	-6		Unit	Note
		Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	55		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	60		ns	
$\overline{CAS}$ set-up time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		ns	14
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		ns	14
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		ns	14
Access time from $\overline{CAS}$ precharge	t_{CPA}		40	ns	3,14
Hyper page cycle time	t_{HPC}	25		ns	13
Hyper page read-modify-write cycle time	t_{HPRWC}	79		ns	13
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		ns	14
$\overline{OE}$ access time	t_{OEA}		20	ns	14
$\overline{OE}$ to data delay	t_{OED}	20		ns	14
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	20	ns	6,11,14
$\overline{OE}$ command hold time	t_{OEH}	15		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		ns	14
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		ns	14
Output data hold time	t_{DOH}	10		ns	14
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	15	ns	6,11,12
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	3	20	ns	6,11,14
$\overline{W}$ to data delay	t_{WED}	20		ns	14
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		ns	
$\overline{W}$ pulse width(Hyper page cycle)	t_{WPE}	5		ns	
Present Detect Read Cycle					
$\overline{PDE}$ to Valid PD bit	t_{PD}		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF. Voh=2.0V and Vol=0.8V.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

   If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data output will contain data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out(at access time) is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. t_{CEZ}(max), t_{REZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

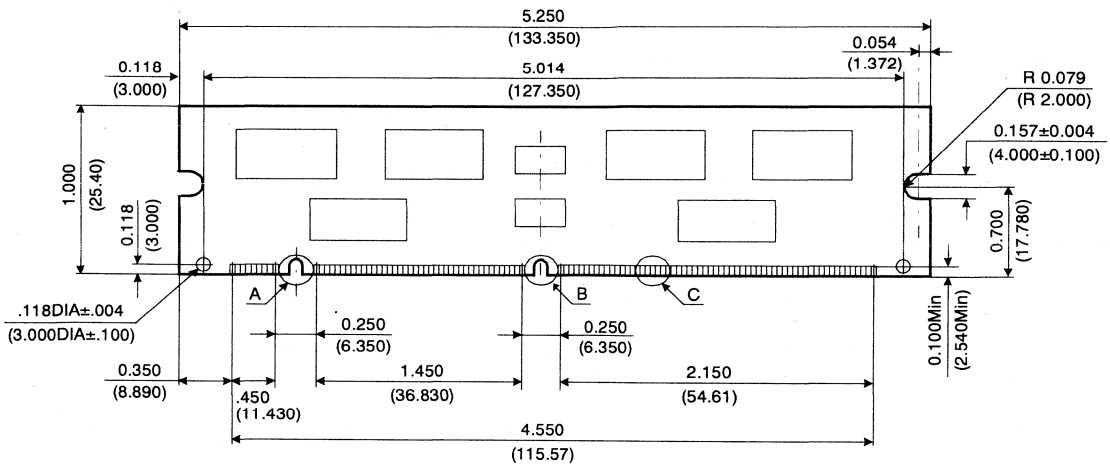
12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ high going.

13. $t_{ASC} \geq t_{CP}$ min

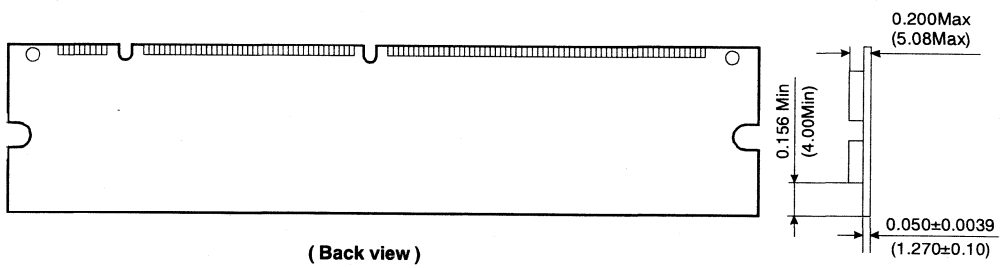
14. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

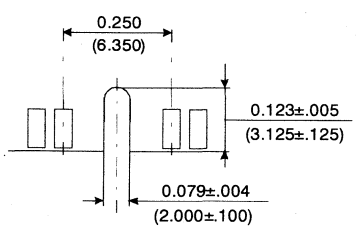
Units : Inches (millimeters)



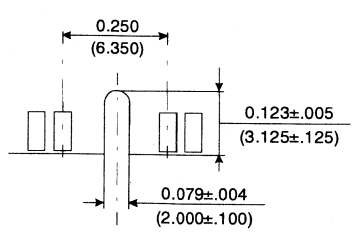
(Front view)



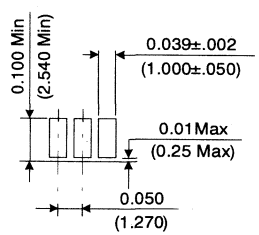
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 1Mx16 DRAM with EDO mode, SOJ and 1Mx4 DRAM with EDO mode,SOJ.
DRAM Part No. : KMM372F124CJ - KM416V1204CJ and KM44V1004DJ

KMM372V213CK/CS Fast Page Mode

2M x 72 DRAM DIMM with ECC using 2Mx8, 2K Refresh , 3.3V

GENERAL DESCRIPTION

The Samsung KMM372V213C is a 2Mx72bits Dynamic RAM high density memory module. The Samsung KMM372V213C consists of nine CMOS 2Mx8bits DRAMs in SOJ/TSOP-II 300mil package, and two 16bits driver IC in 48pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372V213C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	18ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

FEATURES

- Part Identification
  - KMM372V213CK (2048 cycles/32ms Ref. SOJ)
  - KMM372V213CS (2048 cycles/32ms Ref. TSOP)
- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), Single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{RSVD}$	57	DQ22	85	Vss	113	$\overline{RSVD}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	*A11	150	DQ62
11	DQ8	39	*A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	$\overline{RFU}$	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	*$\overline{CAS5}$	158	DQ68
19	DQ14	47	$\overline{RSVD}$	75	DQ33	103	DQ50	131	$\overline{RSVD}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	$\overline{RFU}$	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	*$\overline{CAS1}$	140	DQ57	168	Vcc

PIN NAMES

Pin Names	Function
A0, B0, A1 - A10	Address Input
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	0	0
PD4	1	1
PD5	0	0
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

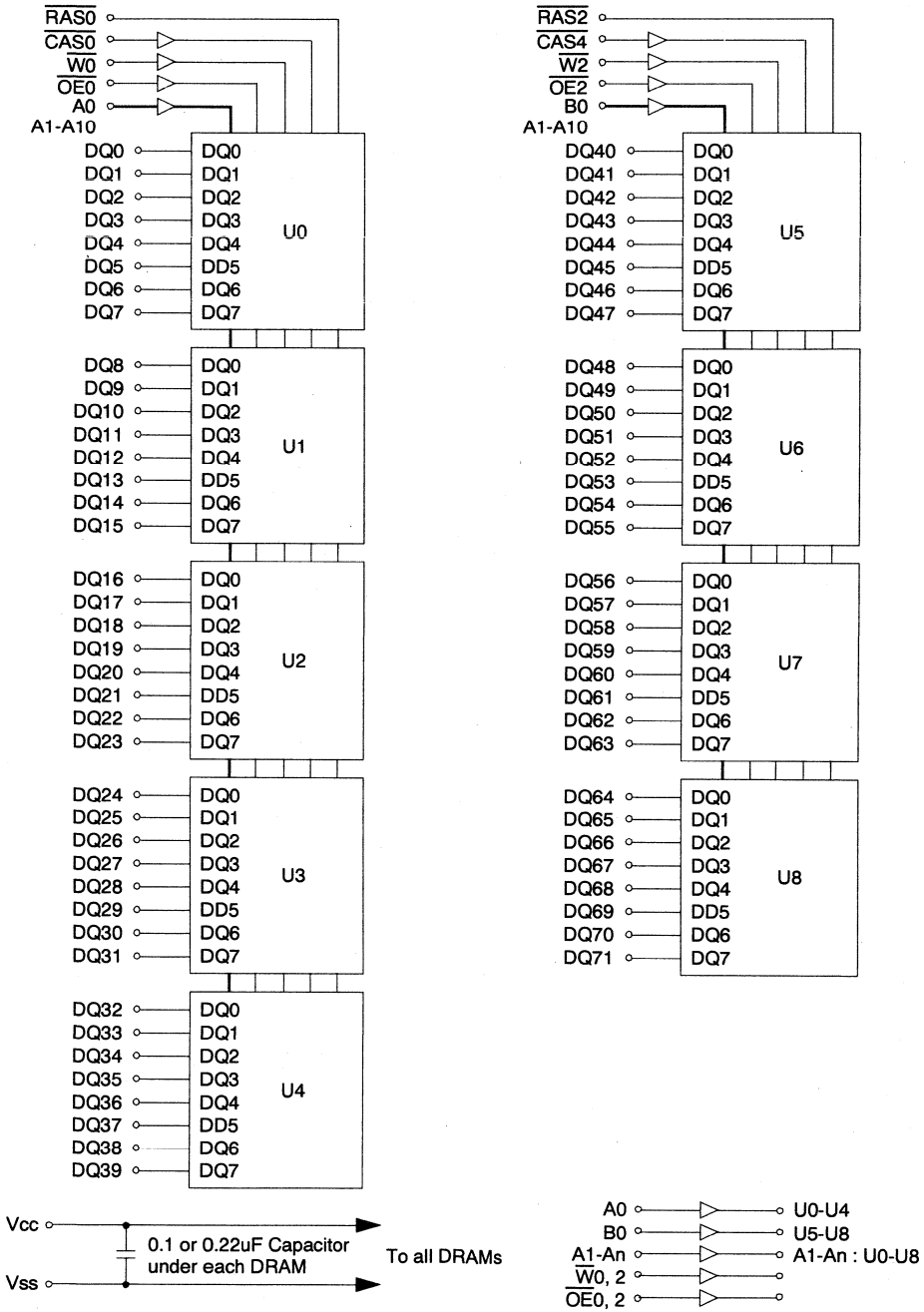
PD Note : PD & ID Terminals must each be pulled up through a resister to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	9	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V/15ns, Pulse width is measured at V_{CC}.
*2 : -1.3V/15ns, Pulse width is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372V213CK/CS		Unit
		Min	Max	
I_{CC1}	-5	-	990	mA
	-6	-	900	mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-5	-	990	mA
	-6	-	900	mA
I_{CC4}	-5	-	810	mA
	-6	-	720	mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-5	-	990	mA
	-6	-	900	mA
$I_{I(L)}$	Don't care	-25	25	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)
I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})
I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)
I_{CC4}*: Fast Page Mode Current * ($\overline{RAS}$=V_{IL} , $\overline{CAS}$ cycling : t_{PC}=min)
I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)
I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)
$I_{I(L)}$: Input Leakage Current (Any Input 0 ≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)
$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V ≤V_{OUT}≤Vcc)
V_{OH} : Output High Voltage Level (I_{OH} = -2mA)
V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one page mode cycle, t_{PC}.

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A10, B0]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	45	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS4}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ1}	-	20	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,11
Access time from column address	t_{AA}		30		35	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,11
Output buffer turn-off delay	t_{OFF}	5	18	5	20	ns	6,11
Transition time(rise and fall)	t_T	2	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	11
$\overline{CAS}$ hold time	t_{CSH}	48		58		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	11
Row address set-up time	t_{ASR}	5		5		ns	11
Row address hold time	t_{RAH}	8		8		ns	11
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	11
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,11
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	18		20		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,11
Data hold time	t_{DH}	15		20		ns	9,11
Refresh period (2K refresh)	t_{REF}		32		32	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.0/0.8V$, $V_{oh}/V_{ol}=2.0/0.8V$, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	71		83		ns	7,11
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	11
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	11
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	3		3		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3,11
Fast page mode cycle time	t_{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	75		80		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	8		8		ns	11
$\overline{OE}$ access time	t_{OEA}		18		20	ns	11
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	11
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF. Voh=2.0V and Vol=0.8V.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS} is not restrictive operating parameter. It included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

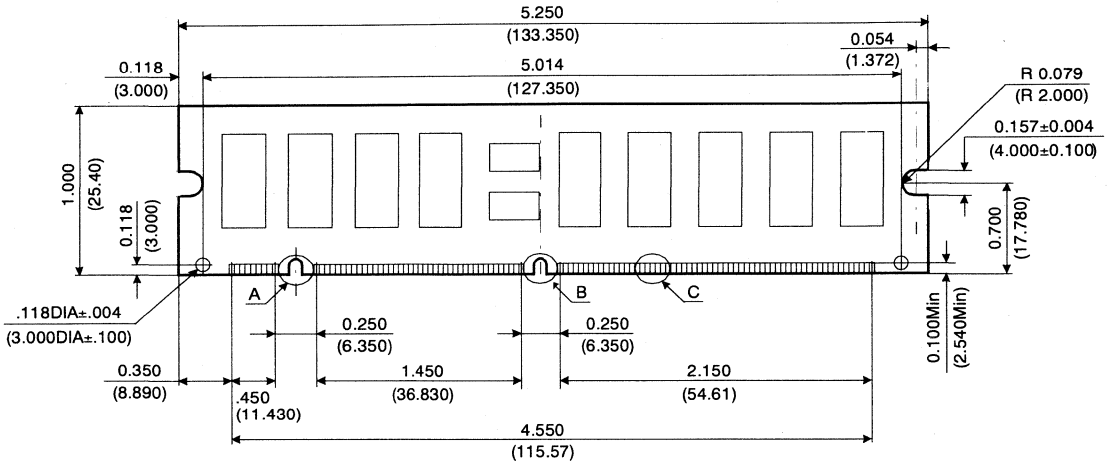
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

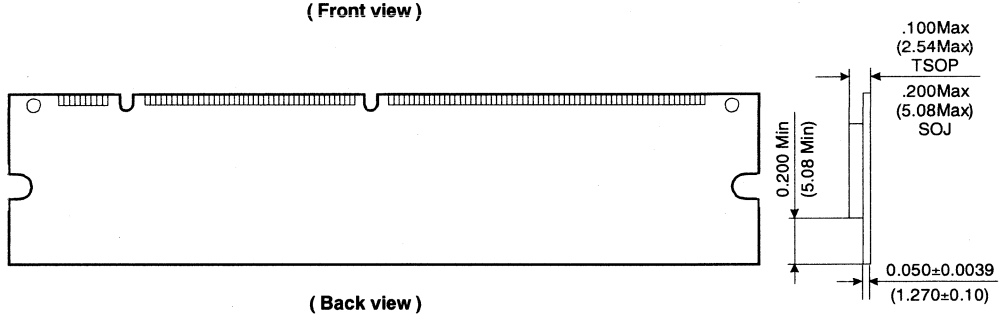
4

PACKAGE DIMENSIONS

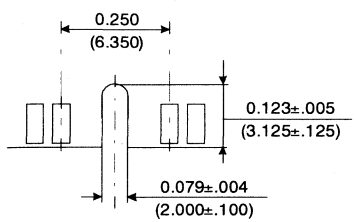
Units : Inches (millimeters)



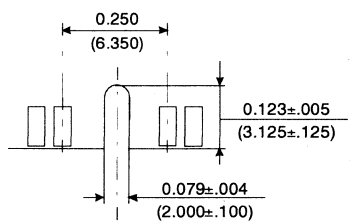
(Front view)



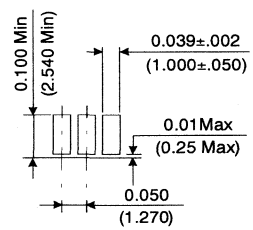
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 2Mx8 DRAM with Fast Page mode, SOJ or TSOP II. (Forward)
DRAM Part No. : KMM372V213CK/CS - KM48V2100CK and KM48V2100CS.

KMM372F213CK/CS EDO Mode

2M x 72 DRAM DIMM with ECC using 2Mx8, 2K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM372F213C is a 2Mx72bits Dynamic RAM high density memory module. The Samsung KMM372F213C consists of nine CMOS 2Mx8bits DRAMs in SOJ/TSOP-II 300mil package, and two 16bits driver IC in 48pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372F213C is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	18ns	84ns	20ns
-6	60ns	20ns	104ns	25ns

FEATURES

- Part Identification
  - KMM372F213CK (2048 cycles/32ms Ref., SOJ)
  - KMM372F213CS (2048 cycles/32ms Ref., TSOP)
- Fast Page Mode with Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), Single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	RSVD	57	DQ22	85	Vss	113	RSVD	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	*A11	150	DQ62
11	DQ8	39	*A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	*$\overline{CAS5}$	158	DQ68
19	DQ14	47	RSVD	75	DQ33	103	DQ50	131	RSVD	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	*$\overline{CAS1}$	140	DQ57	168	Vcc

PD Note : PD & ID Terminals must each be pulled up through a resister to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vssvia on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A10	Address Input
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

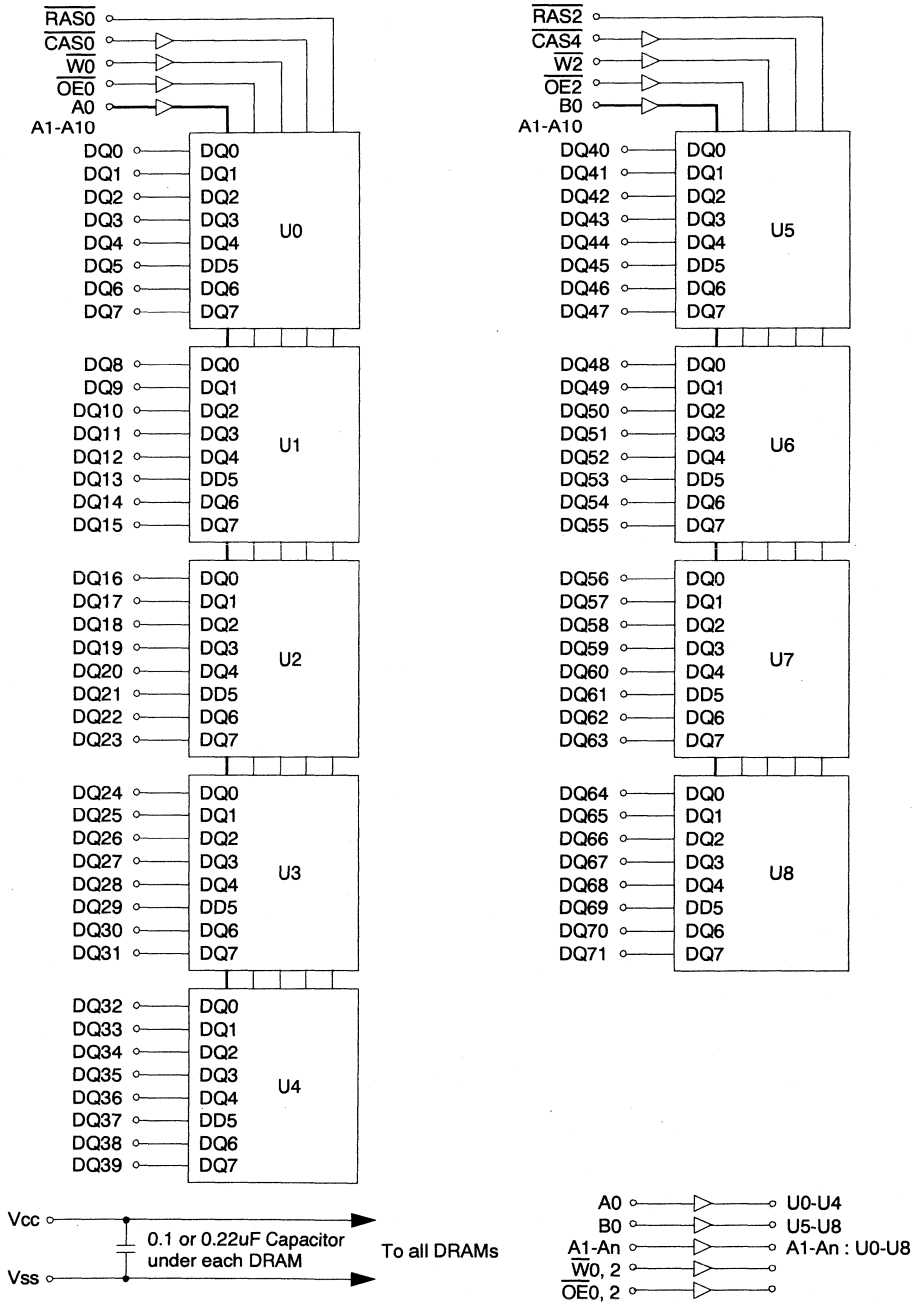
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	0	0
PD4	1	1
PD5	1	1
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	9	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V/15ns, Pulse width is measured at V_{CC}.

*2 : -1.3V/15ns, Pulse width is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372F213CK/CS		Unit
		Min	Max	
I_{CC1}	-5	-	990	mA
	-6	-	900	mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-5	-	990	mA
	-6	-	900	mA
I_{CC4}	-5	-	810	mA
	-6	-	720	mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-5	-	990	mA
	-6	-	900	mA
$I_{I(L)}$	Don't care	-25	25	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: EDO Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{I(L)}$: Input Leakage Current (Any input 0≤ V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)

$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V≤ V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page mode cycle, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A10, B0]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	45	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS4}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ1}	-	20	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	131		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,14
Access time from column address	t_{AA}		30		35	ns	3,10,14
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,14
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,14
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	20	ns	6,11,12,14
Transition time(rise and fall)	t_T	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	14
$\overline{CAS}$ hold time	t_{CSH}	36		43		ns	14
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	13
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,14
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,14
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	14
Row address set-up time	t_{ASR}	5		5		ns	14
Row address hold time	t_{RAH}	8		8		ns	14
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	14
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,14
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	18		20		ns	14
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,14
Data hold time	t_{DH}	13		15		ns	9,14
Refresh period(2K Ref.)	t_{REF}		32		32	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	71		83		ns	7,14

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.0/0.8V$, $V_{oh}/V_{ol}=2.0/0.8V$, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	
$\overline{CAS}$ set-up time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	14
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	14
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	14
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,14
Hyper page cycle time	t_{HPC}	20		25		ns	12
Hyper page read-modify-write cycle time	t_{HPRWC}	68		77		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	14
$\overline{OE}$ access time	t_{OEA}		18		20	ns	14
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	14
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	6,11,14
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	14
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	14
Output data hold time	t_{DOH}	10		10		ns	14
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	6.11.12
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	3	18	3	20	ns	6.11.14
$\overline{W}$ to data delay	t_{WED}	20		20		ns	14
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width(Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF. Voh=2.0V and Vol=0.8V.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

   If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data output will contain data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. t_{CEZ}(max), t_{REZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

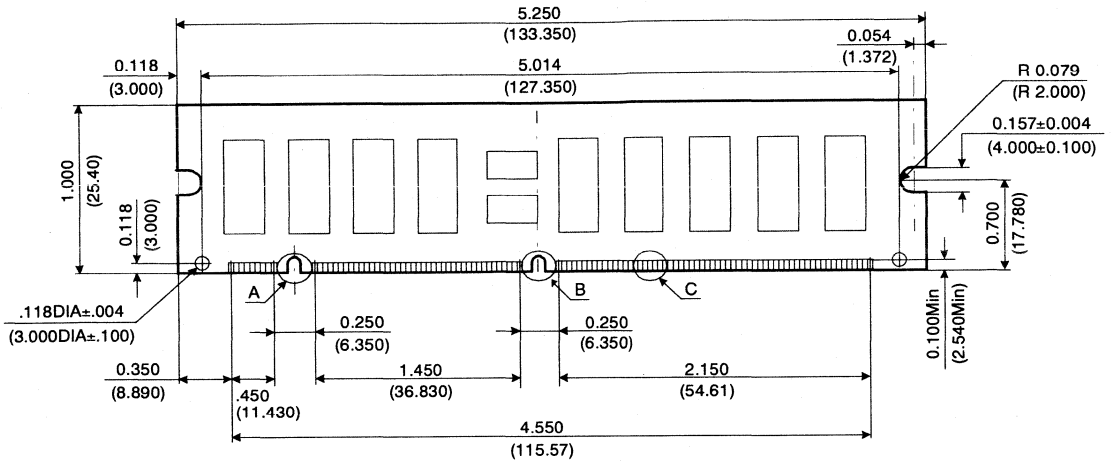
12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ high going.

13. $t_{ASC} \geq t_{CP}$ min

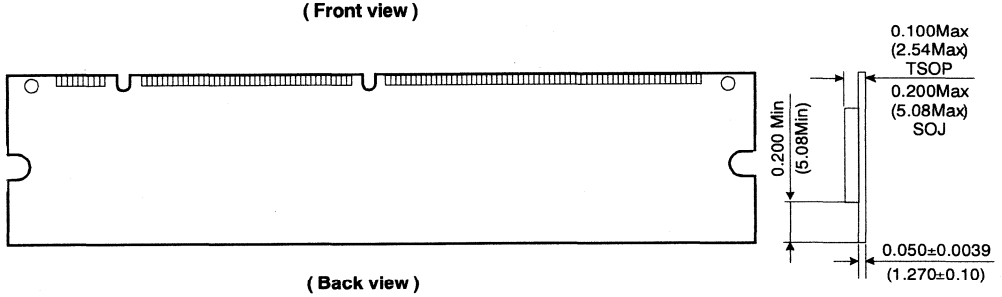
14. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

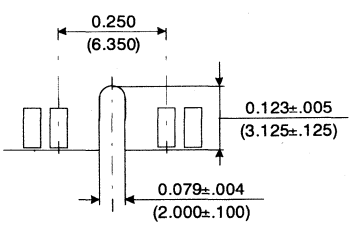
Units : Inches (millimeters)



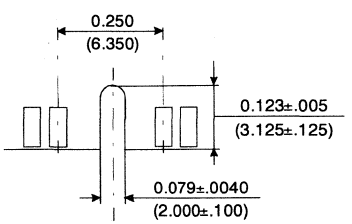
(Front view)



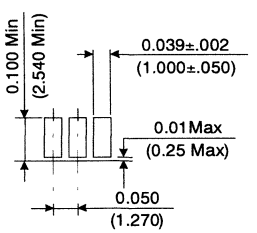
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 2Mx8 DRAM with EDO mode, SOJ or TSOP II. (Forward)
DRAM Part No. : KMM372F213CK/CS - KM48V2104CK and KM48V2104CS.

KMM372V404CS Fast Page Mode

4M x 72 DRAM DIMM with ECC Using 4Mx16 & 4Mx4 , 4K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM372V404C is a 4Mx72bits Dynamic RAM high density memory module. The Samsung KMM372V404C consists of four 4Mx16bits & two 4Mx4bits CMOS DRAMs in TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372V404C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	18ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

FEATURES

- Part Identification
- KMM372V404CS(4096cycles/64ms Ref. TSOP II)
- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	$\overline{RFU}$	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	*$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	$\overline{RFU}$	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	*$\overline{CAS1}$	140	DQ57	168	Vcc

PD Note :PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

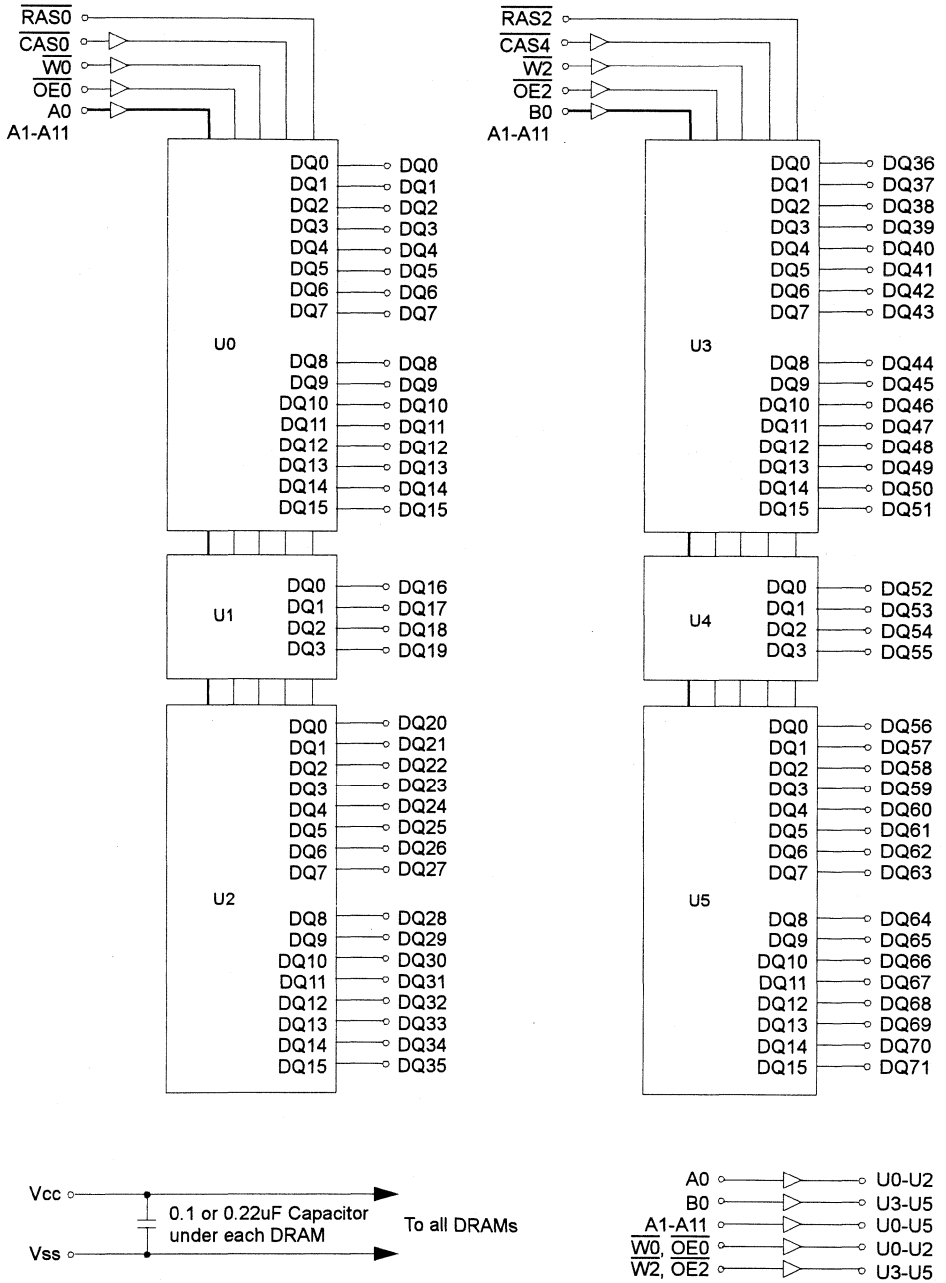
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	1	1
PD3	0	0
PD4	1	1
PD5	0	0
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	6	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width≤15ns, which is measured at Vcc.

*2 : -1.3V at pulse width≤15ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372V404CS		Unit
		Min	Max	
I_{CC1}	-5	-	500	mA
	-6	-	440	mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-5	-	500	mA
	-6	-	440	mA
I_{CC4}	-5	-	400	mA
	-6	-	340	mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-5	-	660	mA
	-6	-	600	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1}* : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}* : Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast Page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A11]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	31	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS4}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,11
Access time from column address	t_{AA}		30		35	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,11
Output buffer turn-off delay	t_{OFF}	5	18	5	20	ns	6,11
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	11
$\overline{CAS}$ hold time	t_{CSH}	48		58		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	11
Row address set-up time	t_{ASR}	5		5		ns	11
Row address hold time	t_{RAH}	8		8		ns	11
Column address set-up time	t_{ASC}	0		0		ns	12
Column address hold time	t_{CAH}	10		10		ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	11
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referencde to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,11
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	15
Data in set-up time	t_{DS}	-2		-2		ns	9,11
Data in hold time	t_{DH}	15		15		ns	9,11
Refresh period	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7,14
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ prechange to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7

4

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{RAS}$ ro $\overline{W}$ delay time	t_{RWD}	71		83		ns	7,11
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	11,16
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	11
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3,11
Fast page mode cycle time	t_{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	76		85		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	13
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	11
$\overline{OE}$ access time	t_{OEA}		18		20	ns	11
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	11
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes tha $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

12. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.

13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

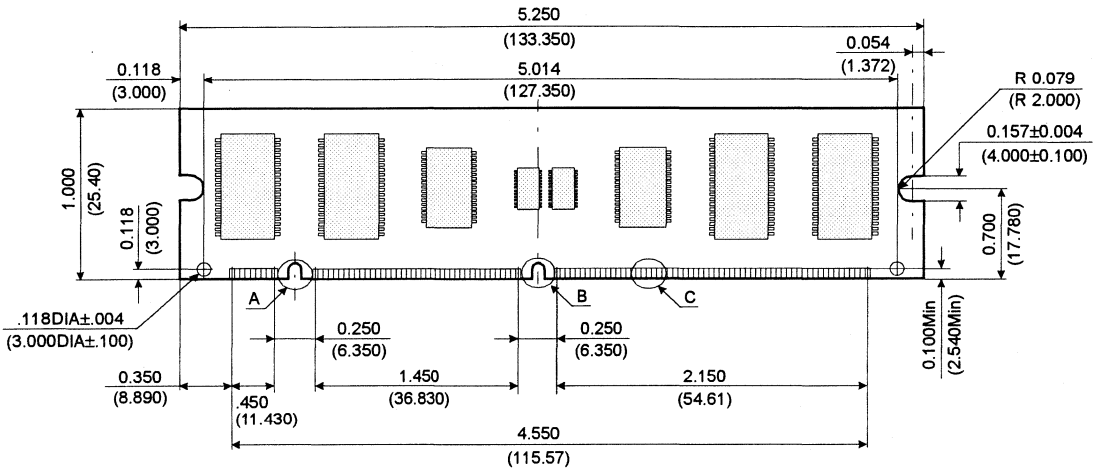
15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.

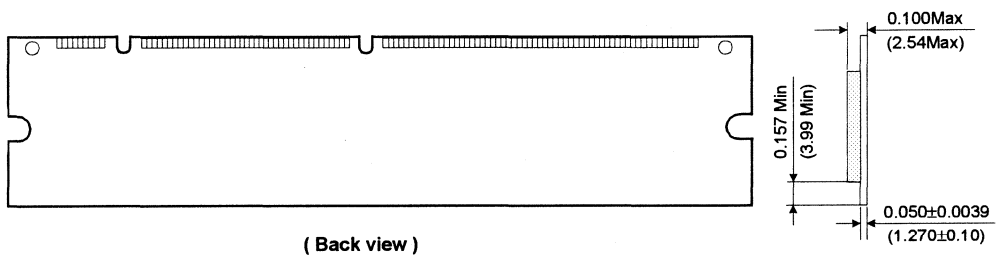
4

PACKAGE DIMENSIONS

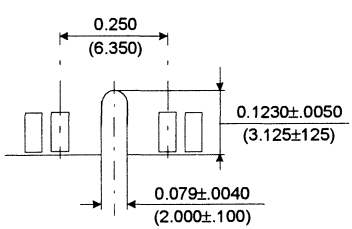
Units : Inches (millimeters)



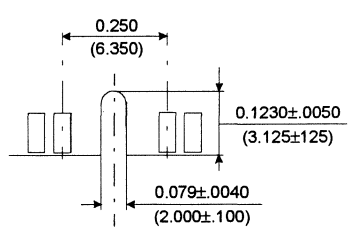
(Front view)



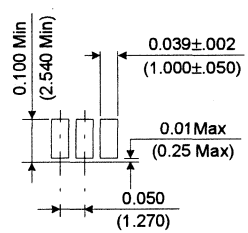
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 & 4Mx4 DRAM with Fast Page mode, TSOP II.
DRAM Part No. : KMM372V404CS -KM416V4100CS & KM44V4000CS

KMM372F404CS EDO Mode

4M x 72 DRAM DIMM with ECC Using 4Mx16 & 4Mx4, 4K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM372F404C is a 4Mx72bits Dynamic RAM high density memory module. The Samsung KMM372F404C consists of four 4Mx16bits & two 4Mx4bits CMOS DRAMs in TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372F404C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

FEATURES

- Part Identification
  - KMM372F404CS(4096cycles/64ms Ref. TSOP II)
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), single sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	18ns	84ns	20ns
-6	60ns	20ns	104ns	25ns

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	*$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	*$\overline{CAS1}$	140	DQ57	168	Vcc

PD Note :PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

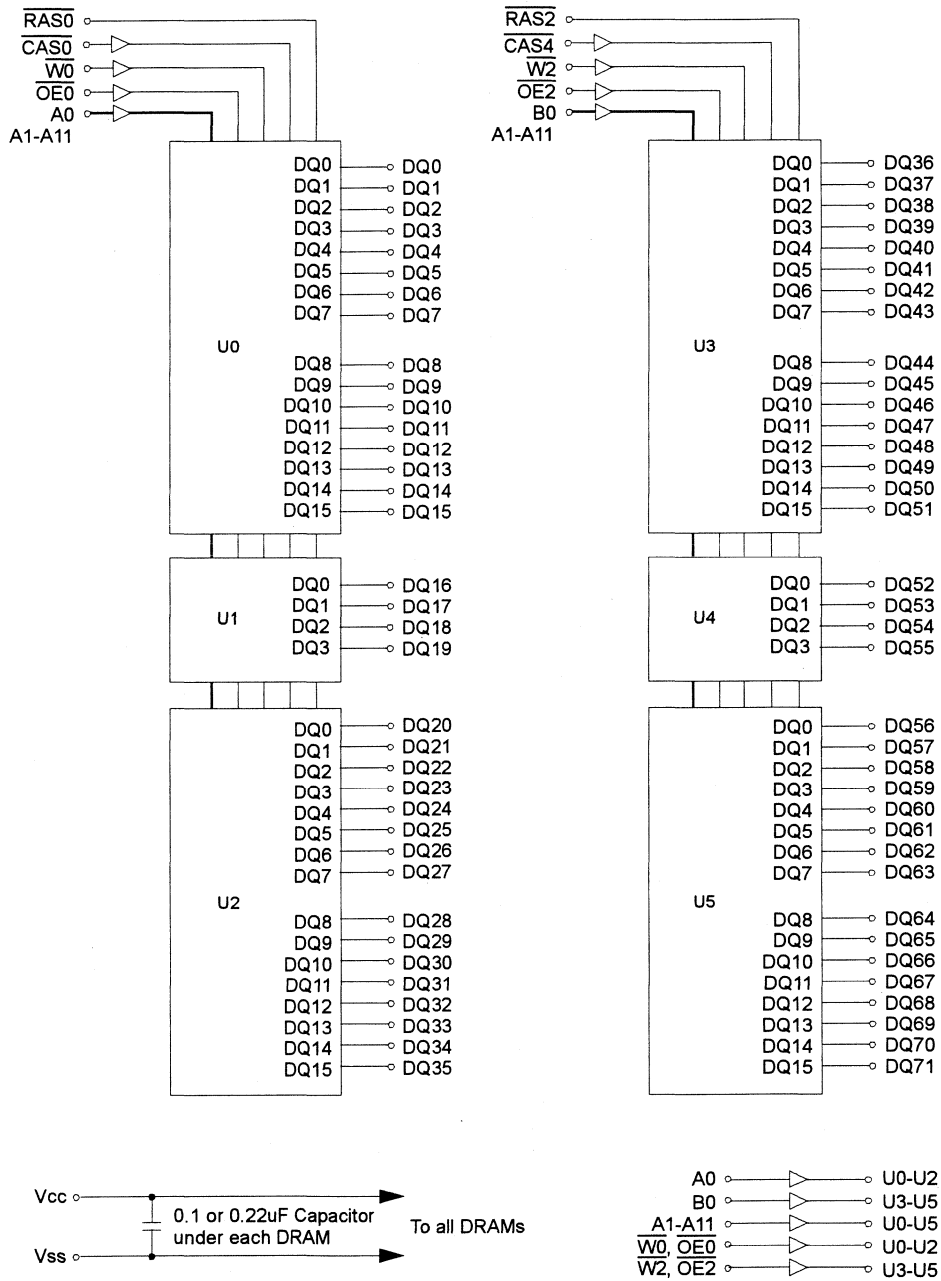
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	1	1
PD3	0	0
PD4	1	1
PD5	1	1
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	6	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width≤15ns, which is measured at Vcc.

*2 : -1.3V at pulse width≤15ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372F404CS		Unit
		Min	Max	
I_{CC1}	-5 -6	- -	660 600	mA mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-5 -6	- -	660 600	mA mA
I_{CC4}	-5 -6	- -	520 460	mA mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-5 -6	- -	660 600	mA mA
$I_{I(L)}$ $I_{O(L)}$	Don't care	-10 -5	10 5	uA uA
V_{OH} V_{OL}	Don't care	2.4 -	- 0.4	V V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A11]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	31	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS4}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	128		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,13
Access time from column address	t_{AA}		30		35	ns	3,10,13
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,13
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,13
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	18	ns	6,11,13
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	13
$\overline{CAS}$ hold time	t_{CSH}	36		38		ns	13
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	15	32	18	40	ns	4,13
$\overline{RAS}$ to column address delay time	t_{RAD}	10	20	13	25	ns	10,13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	13
Row address set-up time	t_{ASR}	5		5		ns	13
Row address hold time	t_{RAH}	5		8		ns	13
Column address set-up time	t_{ASC}	0		0		ns	14
Column address hold time	t_{CAH}	7		10		ns	14
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	13
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,13
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	7		10		ns	
Write command pulse width	t_{WP}	7		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	13
Write command to $\overline{CAS}$ lead time	t_{CWL}	7		10		ns	17
Data set-up time	t_{DS}	-2		-2		ns	9,13
Data hold time	t_{DH}	13		15		ns	9,13
Refresh period	t_{REF}		64		64	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	33		38		ns	7,16
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	68		82		ns	7,13

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	45		53		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	47		58		ns	
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	13,18
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	13
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,13
Hyper page cycle time	t_{HPC}	20		25		ns	12
Hyper page read-modify-write cycle time	t_{HPRWC}	70		77		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	7		10		ns	15
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	13
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	13
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	13
$\overline{OE}$ access time	t_{OEA}		18		20	ns	13
$\overline{OE}$ to data delay	t_{OED}	15		18		ns	13
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	8	18	8	18	ns	13
$\overline{OE}$ command hold time	t_{OEH}	5		5		ns	
Output data hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{DOH}	10		10		ns	13
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	13	3	13	ns	6,11
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	8	18	8	18	ns	6,13
$\overline{W}$ to data delay	t_{WED}	20		20		ns	13
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{IH}/V_{IL}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes tha $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

12. $t_{ASC} \geq 6$ns.

13. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

14. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.

15. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

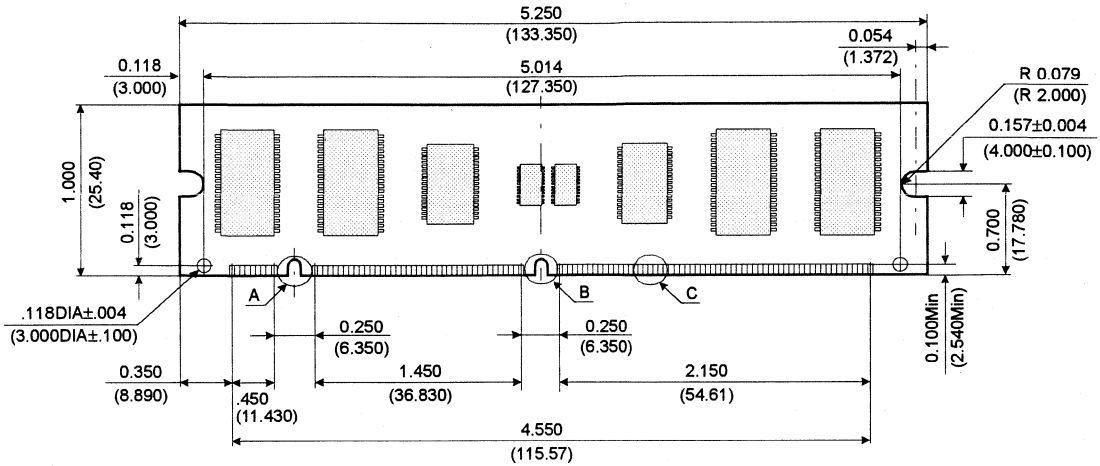
16. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

17. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

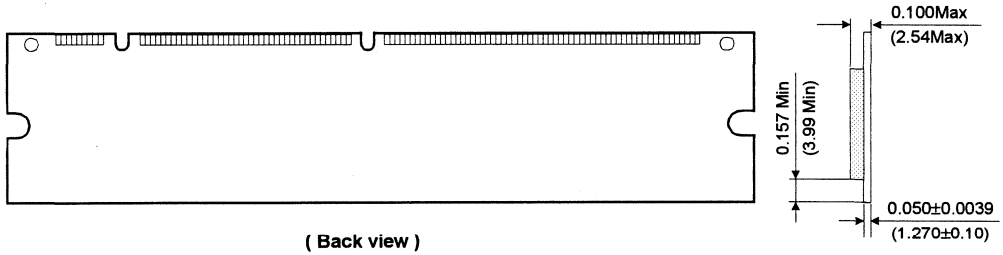
18. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.

PACKAGE DIMENSIONS

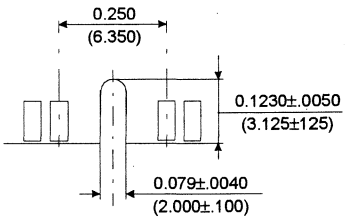
Units : Inches (millimeters)



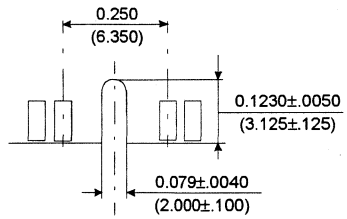
(Front view)



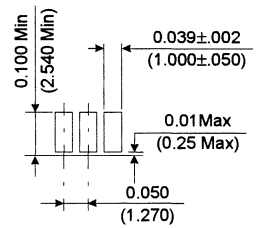
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 & 4Mx4 DRAM with EDO mode, TSOP II.
DRAM Part No. : KMM372F404CS -KM416V4104CS & KM44V4004CS

KMM372V80(8)3CK/CS Fast Page Mode

8Mx72 DRAM DIMM with ECC Using 8Mx8, 4K & 8K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM372V80(8)3C is a 8Mx72bits Dynamic RAM high density memory module. The Samsung KMM372V80(8)3C consists of nine CMOS 8Mx8bits DRAMs in SOJ/TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372V80(8)3C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	18ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM372V803CK	SOJ	4K	4K/64ms	
KMM372V803CS	TSOP			
KMM372V883CK	SOJ	8K	4K/64ms	8K/64ms
KMM372V883CS	TSOP			

- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1250mil), single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	$\overline{Vss}$	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	$\overline{RFU}$	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	*$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	$\overline{Vcc}$	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	$\overline{RFU}$	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	*$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM372V883CK/CS (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
A0, B0, A1 - A12	Address Input(8K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

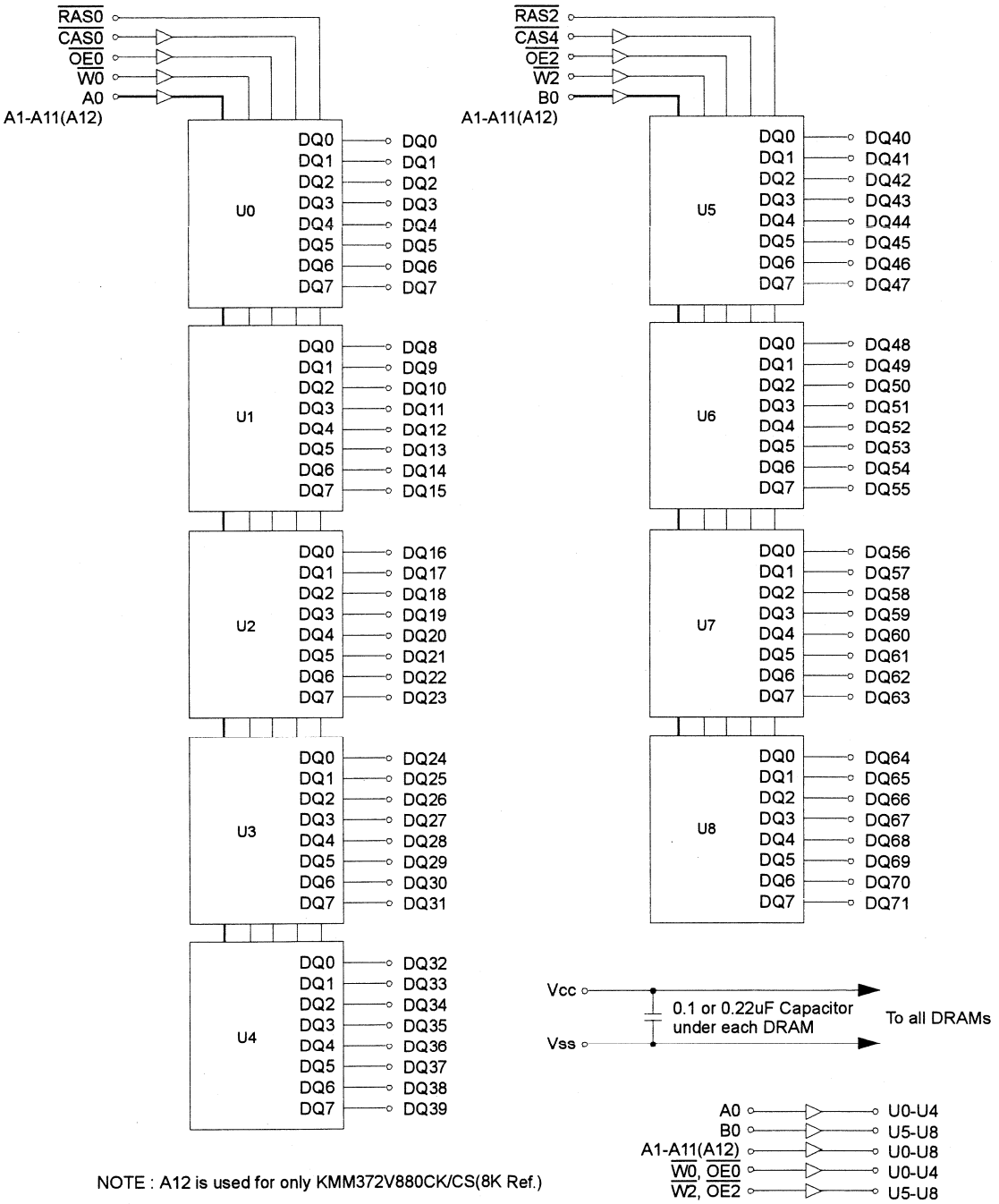
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	1	1
PD4	1	1
PD5	0	0
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM372V880CK/CS(8K Ref.)

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	9	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width≤15ns, which is measured at Vcc.
*2 : -1.3V at pulse width≤15ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372V803CK/CS		KMM372V883CK/CS		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	990	-	720	mA
	-6	-	900	-	630	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	990	-	720	mA
	-6	-	900	-	630	mA
I_{CC4}	-5	-	540	-	540	mA
	-6	-	450	-	450	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	990	-	990	mA
	-6	-	900	-	900	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}* : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}* Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	45	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS4}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,11
Access time from column address	t_{AA}		30		35	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,11
Output buffer turn-off delay	t_{OFF}	5	18	5	20	ns	6,11
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	11
$\overline{CAS}$ hold time	t_{CSH}	48		58		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	11
Row address set-up time	t_{ASR}	5		5		ns	11
Row address hold time	t_{RAH}	8		8		ns	11
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	11
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referencde to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,11
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data in set-up time	t_{DS}	-2		-2		ns	9,11
Data in hold time	t_{DH}	15		15		ns	9,11
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ prechange to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7
$\overline{RAS}$ ro $\overline{W}$ delay time	t_{RWD}	71		83		ns	7,11

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	11
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	11
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3,11
Fast page mode cycle time	t_{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	76		85		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	11
$\overline{OE}$ access time	t_{OEA}		18		20	ns	11
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	11
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{IH}/V_{IL}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes tha $t_{RCD} \ge t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \ge t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \ge t_{RWD}$(min), $t_{CWD} \ge t_{CWD}$(min), $t_{AWD} \ge t_{AWD}$(min) and $t_{CPWD} \ge t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

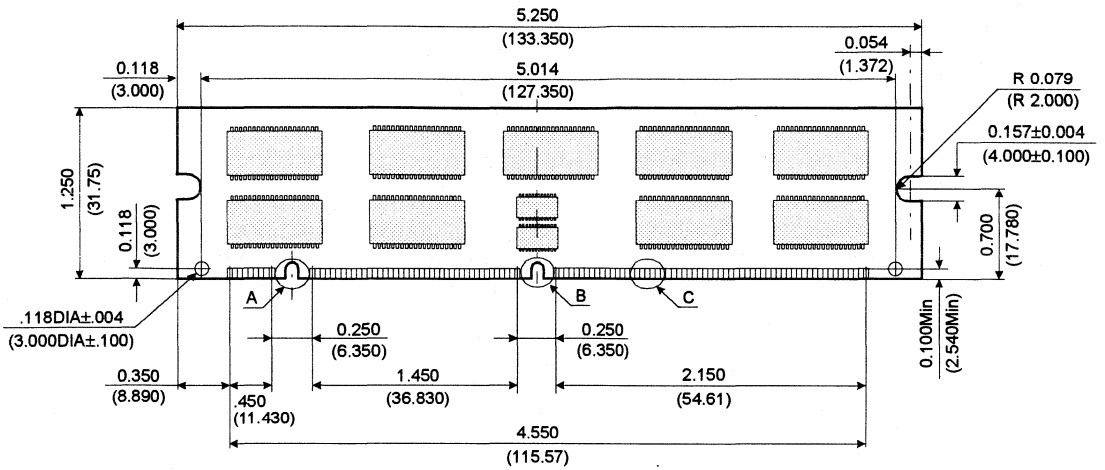
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

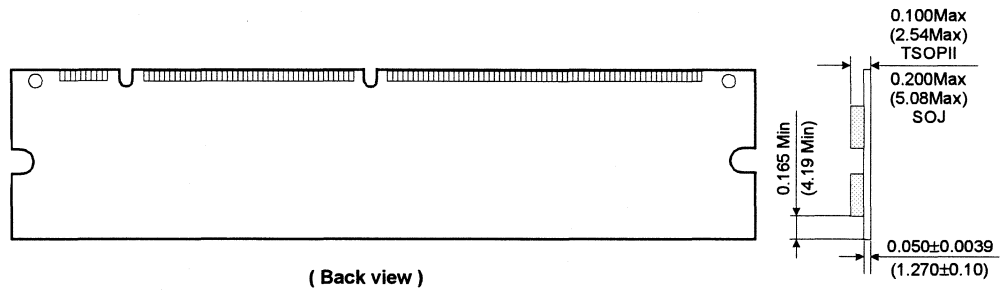
11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

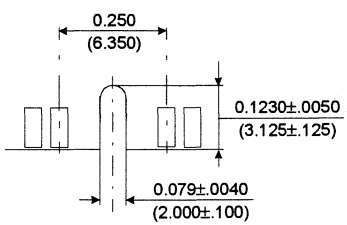
Units : Inches (millimeters)



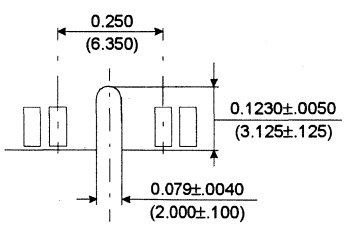
(Front view)



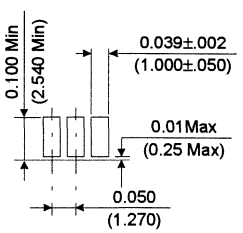
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 DRAM with Fast Page mode, SOJ or TSOPII.
DRAM Part No. : KMM372V803CK/CS - KM48V8100CK, KM48V8100CS.
KMM372V883CK/CS - KM48V8000CK, KM48V8000CS.

KMM372F80(8)3CK/CS EDO Mode

8M x 72 DRAM DIMM with ECC Using 8Mx8, 4K & 8K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM372F80(8)3C is a 8Mx72bits Dynamic RAM high density memory module. The Samsung KMM372F80(8)3C consists of nine CMOS 8Mx8bits DRAMs in SOJ/TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372F80(8)3C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	18ns	84ns	20ns
-6	60ns	20ns	104ns	25ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM372F803CK	SOJ	4K	4K/64ms	
KMM372F803CS	TSOP			
KMM372F883CK	SOJ	8K	4K/64ms	8K/64ms
KMM372F883CS	TSOP			

- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1250mil), single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	*$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	$\overline{RFU}$	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	*$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM372F883CK/CS (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
A0, B0, A1 - A12	Address Input(8K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

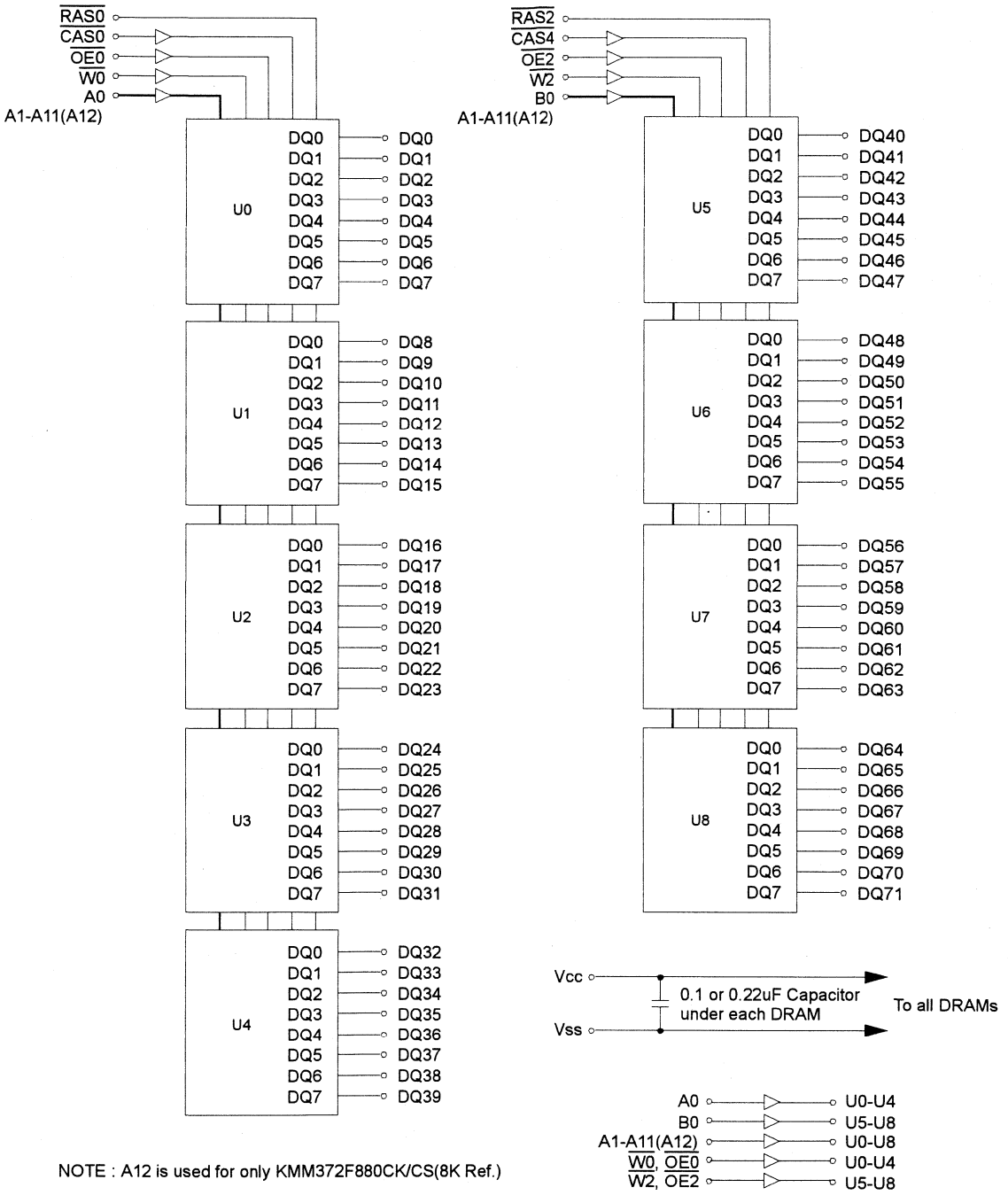
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	1	1
PD4	1	1
PD5	1	1
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM372F880CK/CS(8K Ref.)

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	9	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width≤15ns, which is measured at Vcc.
*2 : -1.3V at pulse width≤15ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372F803CK/CS		KMM372F883CK/CS		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	990	-	720	mA
	-6	-	900	-	630	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	990	-	720	mA
	-6	-	900	-	630	mA
I_{CC4}	-5	-	810	-	810	mA
	-6	-	720	-	720	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	990	-	990	mA
	-6	-	900	-	900	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	45	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS4}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	128		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,13
Access time from column address	t_{AA}		30		35	ns	3,10,13
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,13
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,13
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	18	ns	6,11,13
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	13
$\overline{CAS}$ hold time	t_{CSH}	36		38		ns	13
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	15	32	18	40	ns	4,13
$\overline{RAS}$ to column address delay time	t_{RAD}	10	20	13	25	ns	10,13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	13
Row address set-up time	t_{ASR}	5		5		ns	13
Row address hold time	t_{RAH}	5		8		ns	13
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	7		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	13
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,13
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	7		10		ns	
Write command pulse width	t_{WP}	7		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	13
Write command to $\overline{CAS}$ lead time	t_{CWL}	7		10		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,13
Data hold time	t_{DH}	13		15		ns	9,13
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	33		38		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	68		82		ns	7,13

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	45		53		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	47		58		ns	
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	13
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	13
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,13
Hyper page cycle time	t_{HPC}	20		25		ns	12
Hyper page read-modify-write cycle time	t_{HPRWC}	70		77		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	7		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	13
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	13
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	13
$\overline{OE}$ access time	t_{OEA}		18		20	ns	13
$\overline{OE}$ to data delay	t_{OED}	15		18		ns	13
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	8	18	8	18	ns	13
$\overline{OE}$ command hold time	t_{OEH}	5		5		ns	
Output data hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{DOH}	10		10		ns	13
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	13	3	13	ns	6,11
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	8	18	8	18	ns	6,13
$\overline{W}$ to data delay	t_{WED}	20		20		ns	13
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes tha $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

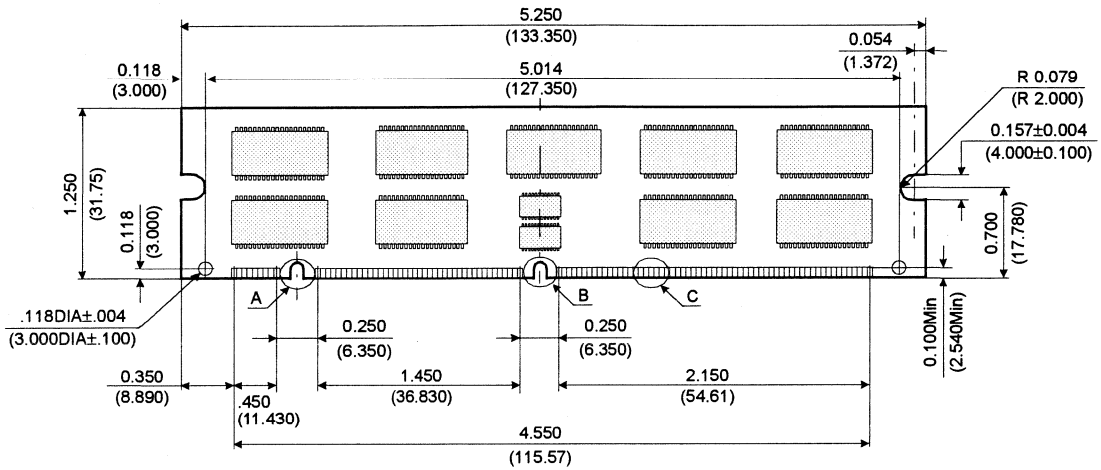
12. $t_{ASC} \geq 6$ns.

13. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

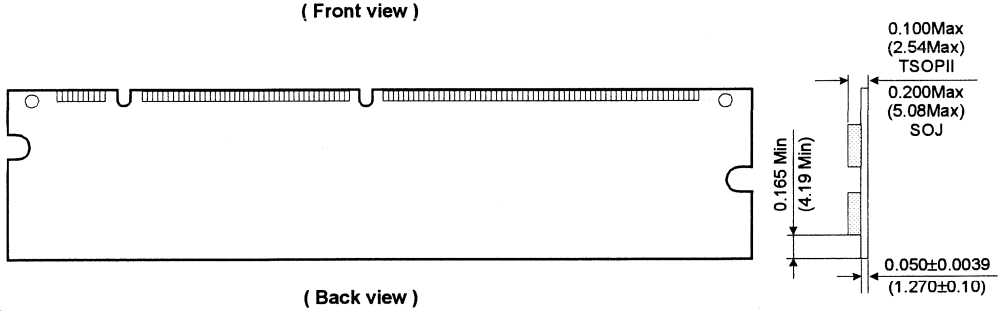
4

PACKAGE DIMENSIONS

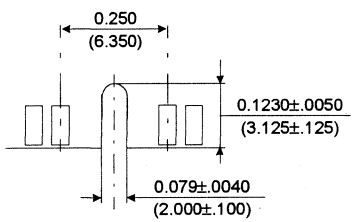
Units : Inches (millimeters)



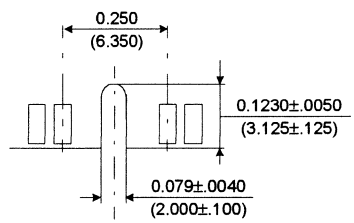
(Front view)



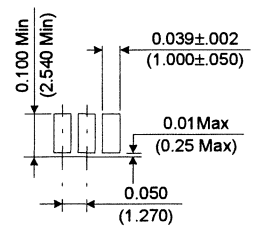
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 DRAM with EDO mode, SOJ or TSOPII.
DRAM Part No. : KMM372F803CK/CS - KM48V8104CK, KM48V8104CS.
KMM372F883CK/CS - KM48V8004CK, KM48V8004CS.

KMM372V804CS Fast Page Mode

8M x 72 DRAM DIMM with ECC Using 4Mx16 & 4Mx4, 4K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM372V804C is a 8Mx72bits Dynamic RAM high density memory module. The Samsung KMM372V804C consists of eight 4Mx16bits & four 4Mx4bits CMOS DRAMs in TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372V804C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

FEATURES

- Part Identification
  - KMM372V804CS(4096cycles/64ms Ref. TSOP II)
- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), double sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	18ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

PD Note :PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$, 1,4,5	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

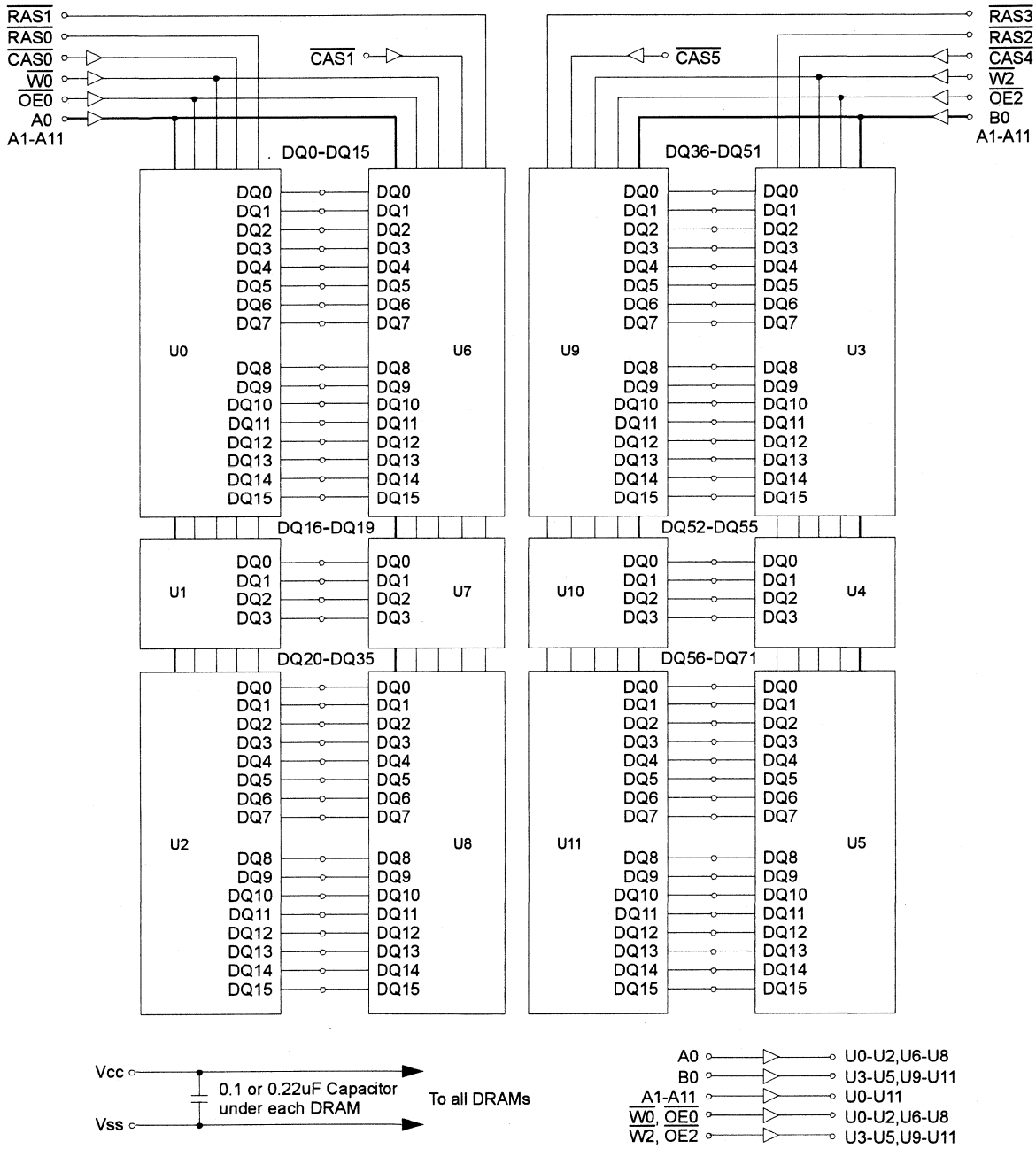
PD & ID Table

Pin	50NS	60NS
PD1	0	0
PD2	0	0
PD3	1	1
PD4	1	1
PD5	0	0
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	12	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V at pulse width≤15ns, which is measured at V_{CC}.
*2 : -1.3V at pulse width≤15ns, which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372V804CS		Unit
		Min	Max	
I_{CC1}	-5 -6	- -	666 606	mA mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-5 -6	- -	666 606	mA mA
I_{CC4}	-5 -6	- -	406 346	mA mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-5 -6	- -	666 606	mA mA
$I_{I(L)}$ $I_{O(L)}$	Don't care	-10 -10	10 10	uA uA
V_{OH} V_{OL}	Don't care	2.4 -	- 0.4	V V

I_{CC1}* : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)
I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})
I_{CC3}* : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)
I_{CC4}* : Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)
I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)
I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)
$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)
$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)
V_{OH} : Output High Voltage Level (I_{OH} = -2mA)
V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast Page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A11]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	31	pF
Input capacitance[$\overline{CAS0}$, 1,4,5]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	24	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5,11
Access time from column address	t_{AA}		30		35	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,11
Output buffer turn-off delay	t_{OFF}	5	18	5	20	ns	6,11
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	11
$\overline{CAS}$ hold time	t_{CSH}	48		58		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	11
Row address set-up time	t_{ASR}	5		5		ns	11
Row address hold time	t_{RAH}	8		8		ns	11
Column address set-up time	t_{ASC}	0		0		ns	12
Column address hold time	t_{CAH}	10		10		ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	11
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referencde to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,11
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	15
Data in set-up time	t_{DS}	-2		-2		ns	9,11
Data in hold time	t_{DH}	15		15		ns	9,11
Refresh period	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7,14
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ prechange to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{RAS}$ ro $\overline{W}$ delay time	t_{RWD}	71		83		ns	7,11
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	11,16
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	11
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3,11
Fast page mode cycle time	t_{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	76		85		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	13
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	11
$\overline{OE}$ access time	t_{OEA}		18		20	ns	11
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	11
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes tha $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

12. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.

13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

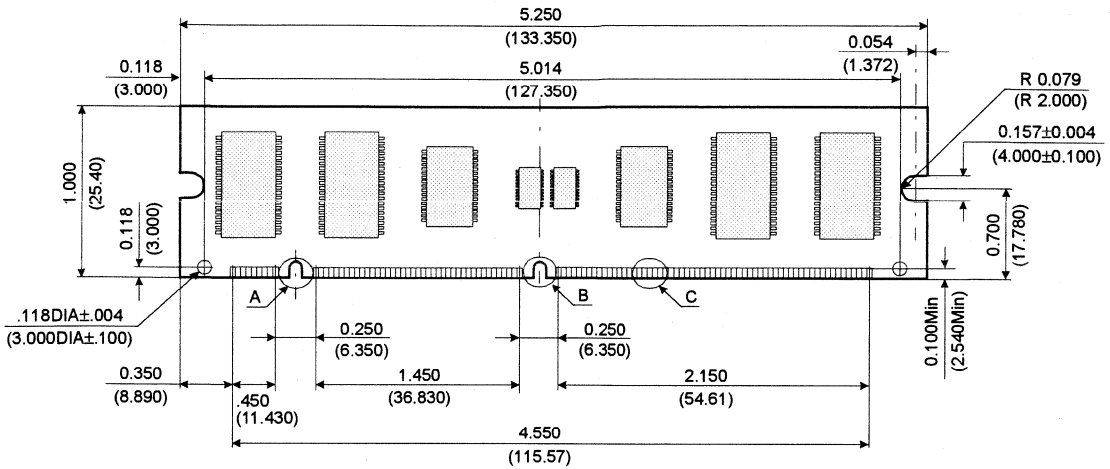
14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

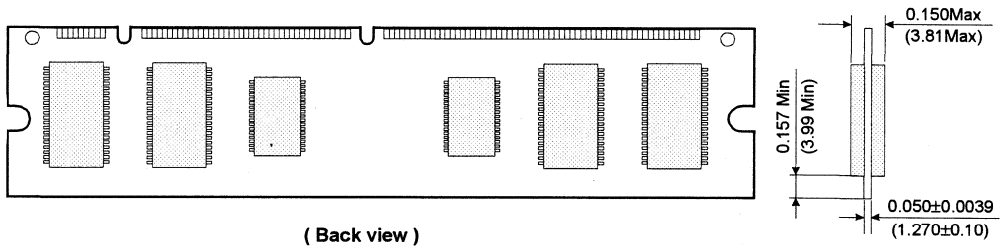
16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.

PACKAGE DIMENSIONS

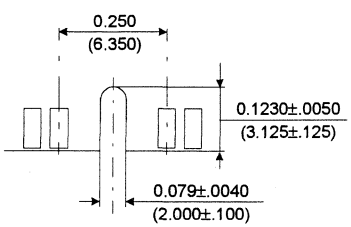
Units : Inches (millimeters)



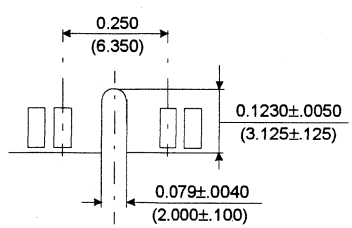
(Front view)



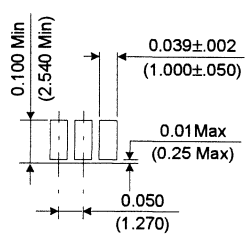
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 & 4Mx4 DRAM with Fast Page mode, TSOP II.
DRAM Part No. : KMM372V804CS -KM416V4100CS & KM44V4000CS

KMM372F804CS EDO Mode

8M x 72 DRAM DIMM with ECC Using 4Mx16 & 4Mx4, 4K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM372F804C is a 8Mx72bits Dynamic RAM high density memory module. The Samsung KMM372F804C consists of eight 4Mx16bits & four 4Mx4bits CMOS DRAMs in TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372F804C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	18ns	84ns	20ns
-6	60ns	20ns	104ns	25ns

FEATURES

- Part Identification
  - KMM372F804CS(4096cycles/64ms Ref. TSOP II)
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

PD Note :PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$, 1,4,5	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

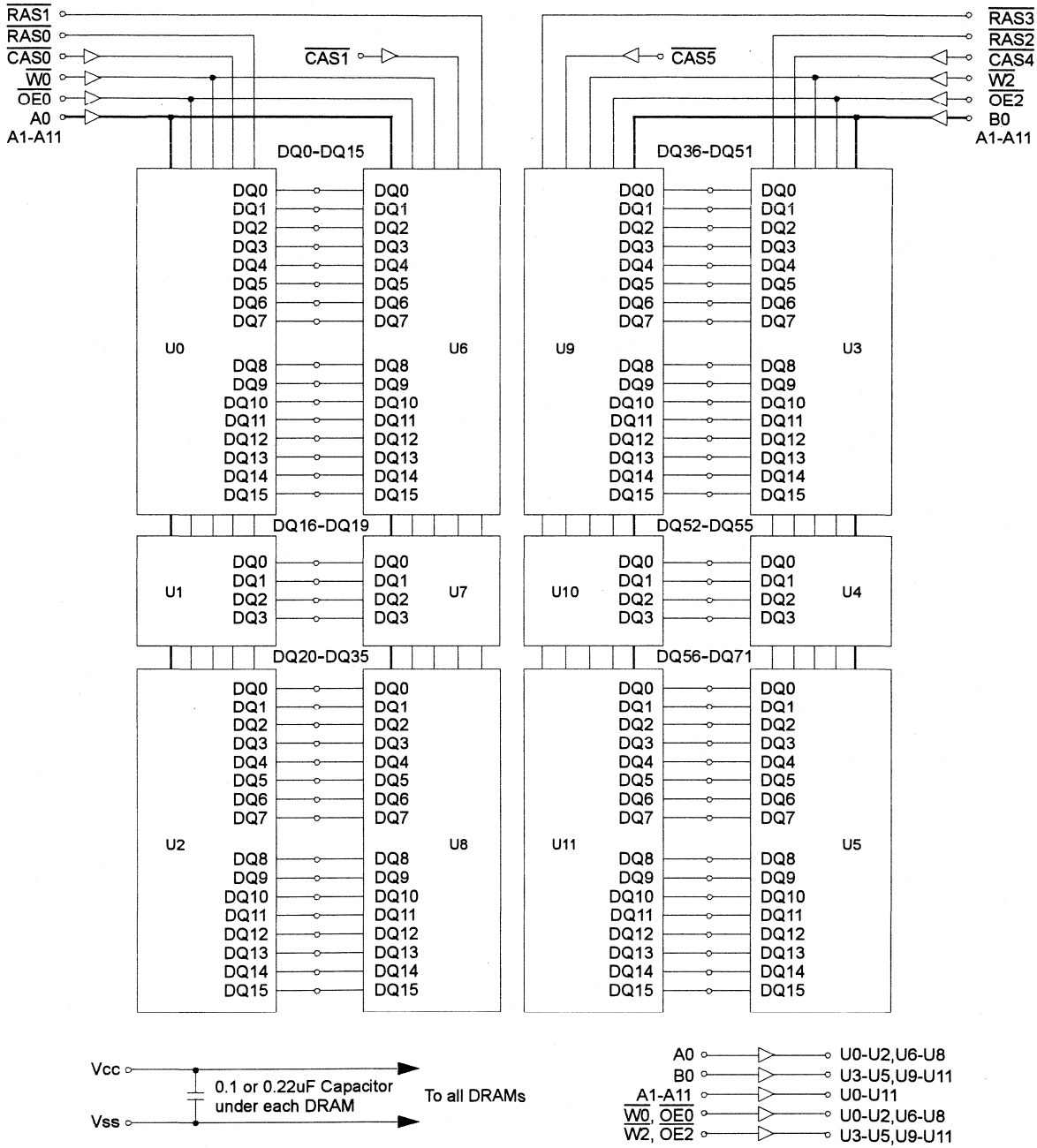
PD & ID Table

Pin	50NS	60NS
PD1	0	0
PD2	0	0
PD3	1	1
PD4	1	1
PD5	1	1
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	12	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width≤15ns, which is measured at Vcc.

*2 : -1.3V at pulse width≤15ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372F804CS		Unit
		Min	Max	
I_{CC1}	-5	-	666	mA
	-6	-	606	mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-5	-	666	mA
	-6	-	606	mA
I_{CC4}	-5	-	526	mA
	-6	-	466	mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-5	-	666	mA
	-6	-	606	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-10	10	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1}* : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}* : Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A11]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	31	pF
Input capacitance[$\overline{CAS0}$, 1,4,5]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	24	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	128		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,13
Access time from column address	t_{AA}		30		35	ns	3,10,13
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,13
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,13
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	18	ns	6,11,13
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	13
$\overline{CAS}$ hold time	t_{CSH}	36		38		ns	13
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	15	32	18	40	ns	4,13
$\overline{RAS}$ to column address delay time	t_{RAD}	10	20	13	25	ns	10,13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	13
Row address set-up time	t_{ASR}	5		5		ns	13
Row address hold time	t_{RAH}	5		8		ns	13
Column address set-up time	t_{ASC}	0		0		ns	14
Column address hold time	t_{CAH}	7		10		ns	14
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	13
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,13
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	7		10		ns	
Write command pulse width	t_{WP}	7		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	13
Write command to $\overline{CAS}$ lead time	t_{CWL}	7		10		ns	17
Data set-up time	t_{DS}	-2		-2		ns	9,13
Data hold time	t_{DH}	13		15		ns	9,13
Refresh period	t_{REF}		64		64	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	33		38		ns	7,16
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	68		82		ns	7,13

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	45		53		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	47		58		ns	
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	13,18
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	13
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,13
Hyper page cycle time	t_{HPC}	20		25		ns	12
Hyper page read-modify-write cycle time	t_{HPRWC}	70		77		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	7		10		ns	15
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	13
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	13
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	13
$\overline{OE}$ access time	t_{OEA}		18		20	ns	13
$\overline{OE}$ to data delay	t_{OED}	15		18		ns	13
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	8	18	8	18	ns	13
$\overline{OE}$ command hold time	t_{OEH}	5		5		ns	
Output data hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{DOH}	10		10		ns	13
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	13	3	13	ns	6,11
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	8	18	8	18	ns	6,13
$\overline{W}$ to data delay	t_{WED}	20		20		ns	13
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes tha $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

12. $t_{ASC} \geq 6$ns.

13. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

14. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.

15. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

16. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

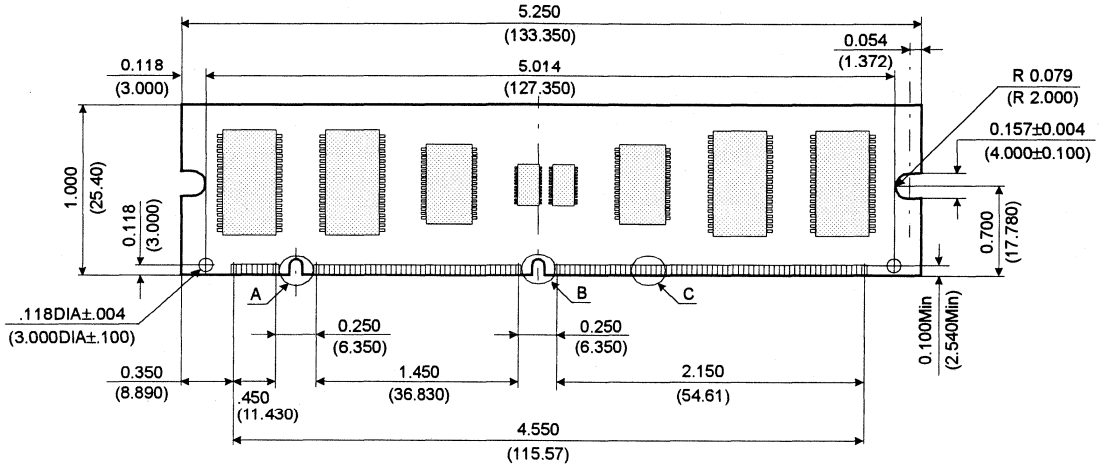
17. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

18. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.

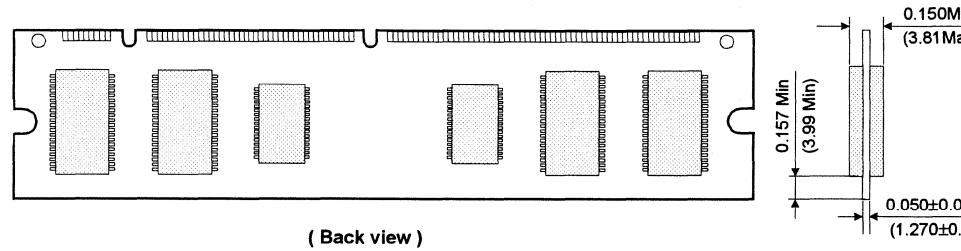
4

PACKAGE DIMENSIONS

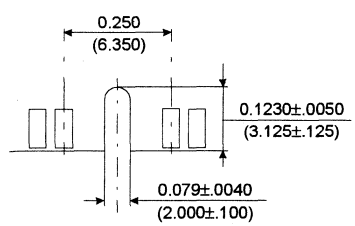
Units : Inches (millimeters)



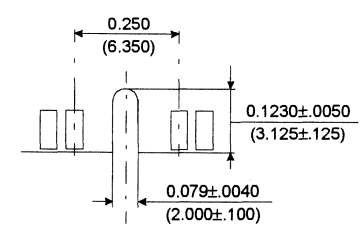
(Front view)



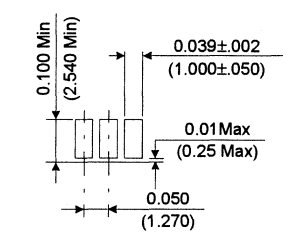
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 & 4Mx4 DRAM with EDO mode, TSOP II.
DRAM Part No. : KMM372F804CS -KM416V4104CS & KM44V4004CS

KMM372V160(8)0CK/CS Fast Page Mode

16M x 72 DRAM DIMM with ECC Using 16Mx4, 4K & 8K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM372V160(8)0C is a 16Mx72bits Dynamic RAM high density memory module. The Samsung KMM372V160(8)0C consists of eighteen CMOS 16Mx4bits DRAMs in SOJ/TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372V160(8)0C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	tRAC	tCAC	tRC	tPC
-5	50ns	18ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM372V1600CK	SOJ	4K	4K/64ms	
KMM372V1600CS	TSOP			
KMM372V1680CK	SOJ	8K	4K/64ms	8K/64ms
KMM372V1680CS	TSOP			

- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1250mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	RSVD
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	*$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	RSVD	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	RSVD	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	*$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM372V1680CK/CS (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref)
A0, B0, A1 - A12	Address Input(8K ref)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

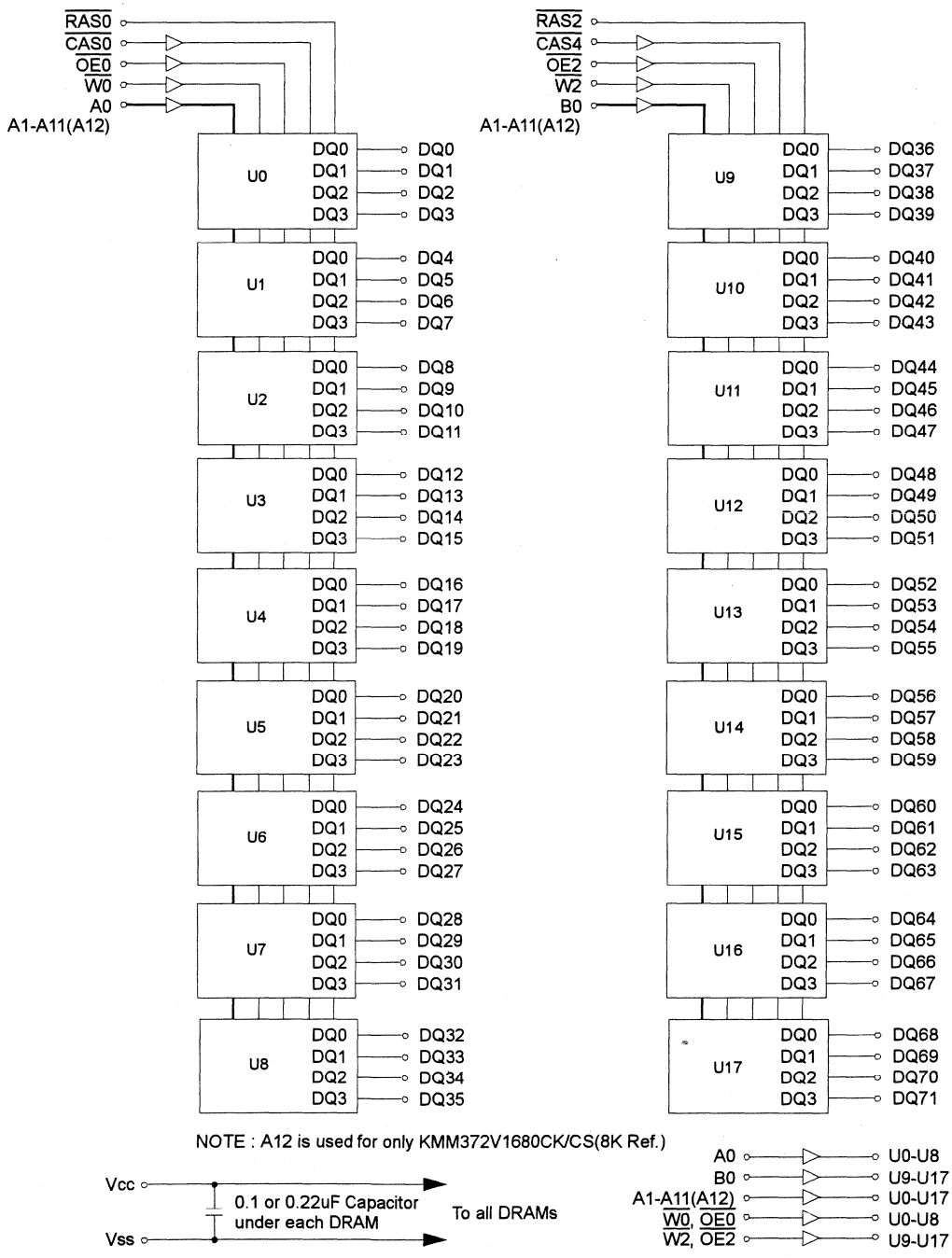
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	1	1
PD3	1	1
PD4	1	1
PD5	0	0
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	18	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width≤15ns, which is measured at Vcc.
*2 : -1.3V at pulse width≤15ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372V1600CK/CS		KMM372V1680CK/CS		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	1980	-	1440	mA
	-6	-	1800	-	1260	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	1980	-	1440	mA
	-6	-	1800	-	1260	mA
I_{CC4}	-5	-	1080		1080	mA
	-6	-	900	-	900	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	1980	-	1980	mA
	-6	-	1800	-	1800	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)
I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})
I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)
I_{CC4}*: Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)
I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)
I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)
$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)
$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)
V_{OH} : Output High Voltage Level (I_{OH} = -2mA)
V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	73	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS4}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,11
Access time from column address	t_{AA}		30		35	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,11
Output buffer turn-off delay	t_{OFF}	5	18	5	20	ns	6,11
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	11
$\overline{CAS}$ hold time	t_{CSH}	48		58		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	11
Row address set-up time	t_{ASR}	5		5		ns	11
Row address hold time	t_{RAH}	8		8		ns	11
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	11
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referencde to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,11
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data in set-up time	t_{DS}	-2		-2		ns	9,11
Data in hold time	t_{DH}	15		15		ns	9,11
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delaly time	t_{CWD}	36		40		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ prechange to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7
$\overline{RAS}$ ro $\overline{W}$ delay time	t_{RWD}	71		83		ns	7,11

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	11
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	11
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		35	ns	3,11
Fast page mode cycle time	t_{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	85		76		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	11
$\overline{OE}$ access time	t_{OEA}		18		20	ns	11
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	11
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{IH}/V_{IL}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes tha $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

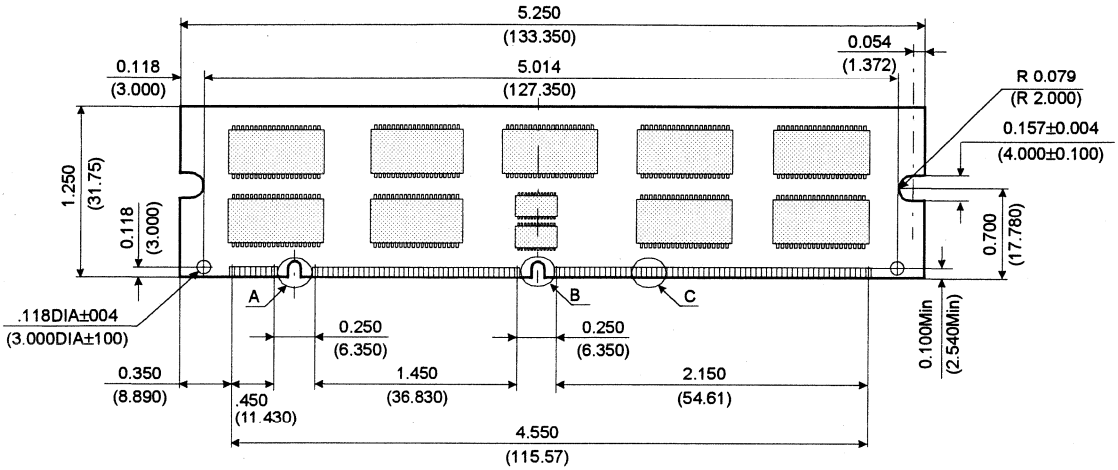
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

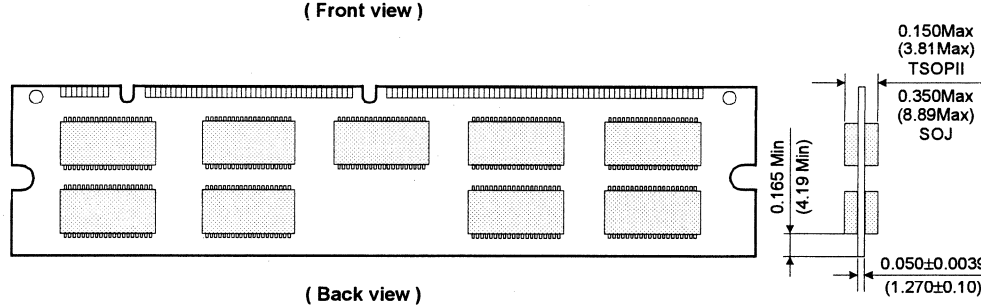
11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

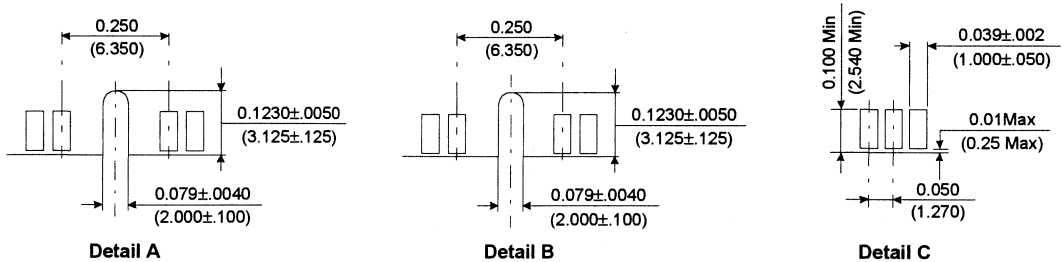
Units : Inches (millimeters)



(Front view)



(Back view)



Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx4 DRAM with Fast Page mode, SOJ or TSOPII.
DRAM Part No. : KMM372V1600CK/CS - KM44V16100CK, KM44V16100CS.
KMM372V1680CK/CS - KM44V16000CK, KM44V16000CS.

KMM372F160(8)0CK/CS EDO Mode

16M x 72 DRAM DIMM with ECC Using 16Mx4, 4K & 8K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM372F160(8)0C is a 16Mx72bits Dynamic RAM high density memory module. The Samsung KMM372F160(8)0C consists of eighteen CMOS 16Mx4bits DRAMs in SOJ/TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372F160(8)0C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	18ns	84ns	20ns
-6	60ns	20ns	104ns	25ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM372F1600CK	SOJ	4K	4K/64ms	
KMM372F1600CS	TSOP			
KMM372F1680CK	SOJ	8K	4K/64ms	8K/64ms
KMM372F1680CS	TSOP			

- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1250mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	*$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	*$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM372F1680CK/CS (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
A0, B0, A1 - A12	Address Input(8K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

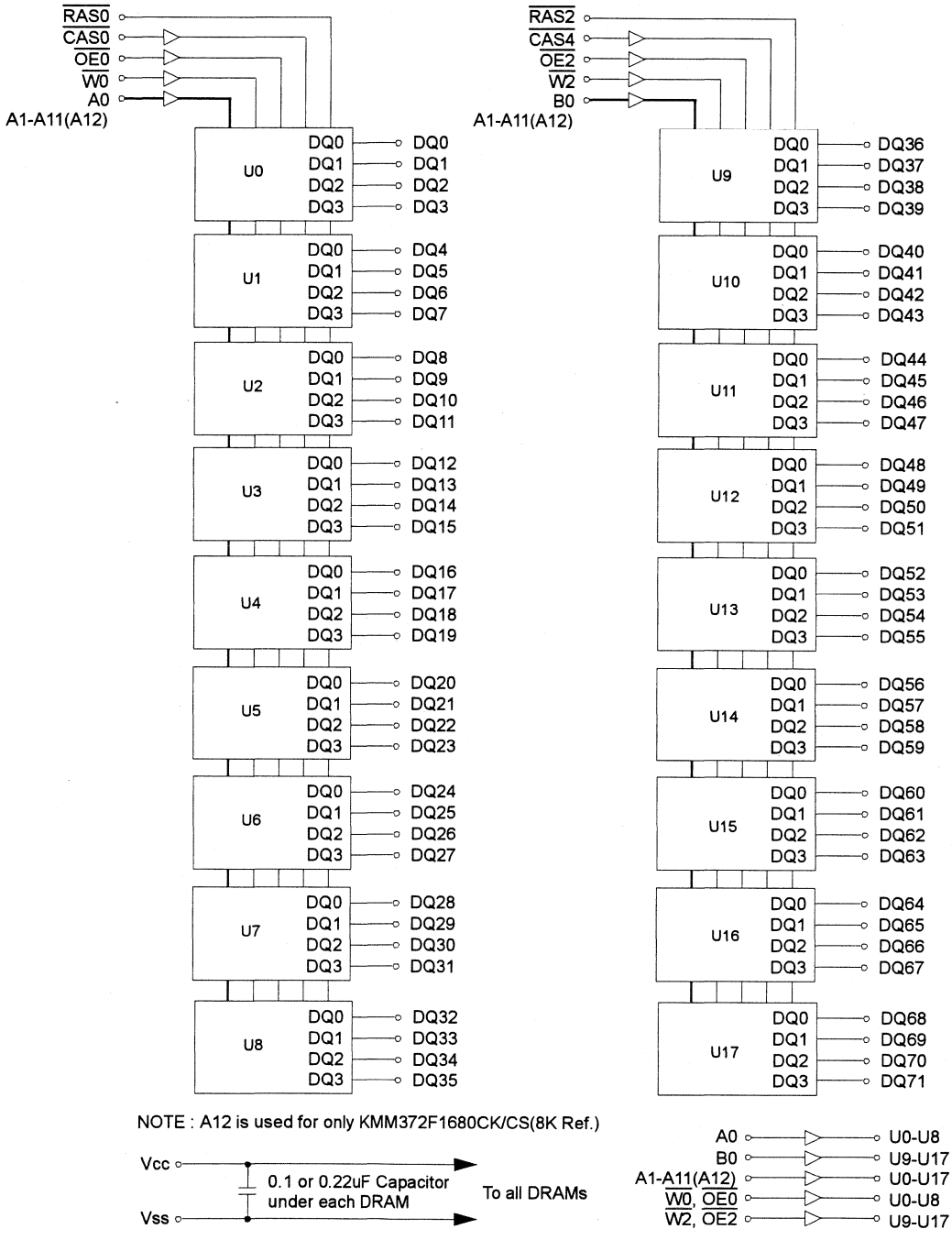
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	1	1
PD3	1	1
PD4	1	1
PD5	1	1
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	18	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width≤15ns, which is measured at Vcc.
*2 : -1.3V at pulse width≤15ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372F1600CK/CS		KMM372F1680CK/CS		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	1980	-	1440	mA
	-6	-	1800	-	1260	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	1980	-	1440	mA
	-6	-	1800	-	1260	mA
I_{CC4}	-5	-	1620	-	1620	mA
	-6	-	1440	-	1440	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	1980	-	1980	mA
	-6	-	1800	-	1800	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	73	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS4}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	128		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,13
Access time from column address	t_{AA}		30		35	ns	3,10,13
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,13
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,13
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	18	ns	6,11,13
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	13
$\overline{CAS}$ hold time	t_{CSH}	36		38		ns	13
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	15	32	18	40	ns	4,13
$\overline{RAS}$ to column address delay time	t_{RAD}	10	20	13	25	ns	10,13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	13
Row address set-up time	t_{ASR}	5		5		ns	13
Row address hold time	t_{RAH}	5		8		ns	13
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	7		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	13
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,13
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	7		10		ns	
Write command pulse width	t_{WP}	7		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	13
Write command to $\overline{CAS}$ lead time	t_{CWL}	7		10		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,13
Data hold time	t_{DH}	13		15		ns	9,13
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	33		38		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	68		82		ns	7,13

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	45		53		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	47		58		ns	
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	13
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	13
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,13
Hyper page cycle time	t_{HPC}	20		25		ns	12
Hyper page read-modify-write cycle time	t_{HPRWC}	70		77		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	7		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	13
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	13
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	13
$\overline{OE}$ access time	t_{OEA}		18		20	ns	13
$\overline{OE}$ to data delay	t_{OED}	15		18		ns	13
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	8	18	8	18	ns	13
$\overline{OE}$ command hold time	t_{OEH}	5		5		ns	
Output data hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{DOH}	10		10		ns	13
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	13	3	13	ns	6,11
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	8	18	8	18	ns	6,13
$\overline{W}$ to data delay	t_{WED}	20		20		ns	13
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes tha $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min).
   The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

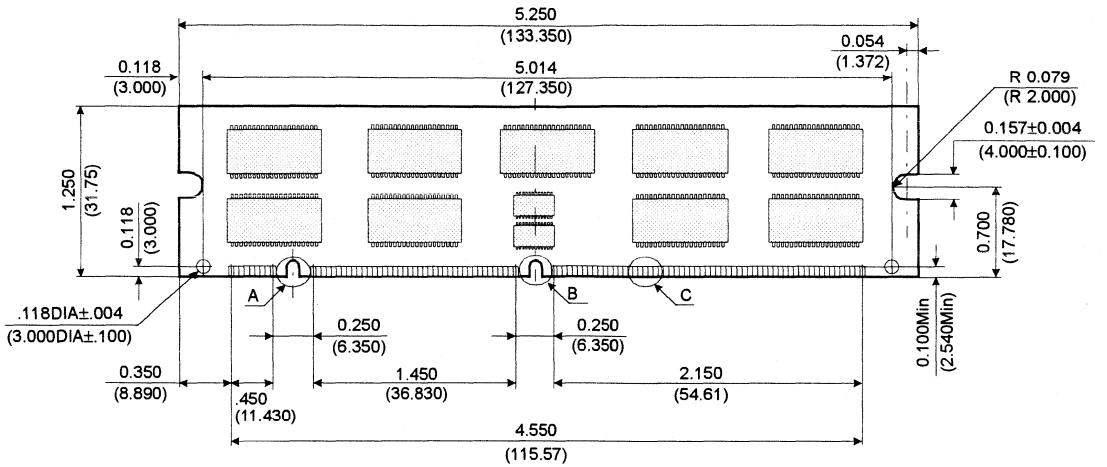
11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

12. $t_{ASC} \geq$ 6ns.

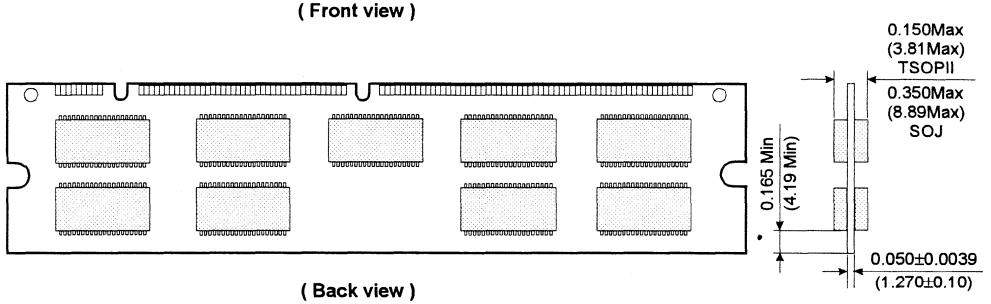
13. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

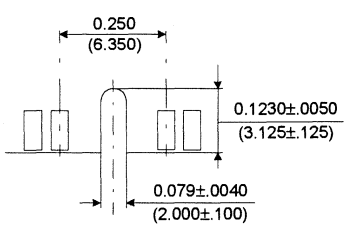
Units : Inches (millimeters)



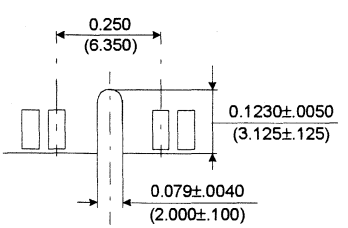
(Front view)



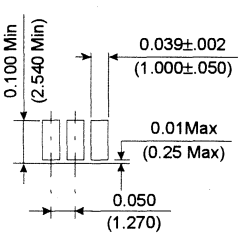
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx4 DRAM with EDO mode, SOJ (400 mil) or TSOPII.
DRAM Part No. : KMM372F1600CK/CS - KM44V16104CK, KM44V16104CS.
KMM372F1680CK/CS - KM44V16004CK, KM44V16004CS.

KMM372V320(8)0CS1 Fast Page Mode

32M x 72 DRAM DIMM with ECC Using 16Mx4, 4K & 8K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM372V320(8)0CS1 is a 32Mx72bits Dynamic RAM high density memory module. The Samsung KMM372V320(8)0CS1 consists of thirty-six CMOS 16Mx4bits DRAMs in TSOP 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372V320(8)0CS1 is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	18ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM372V3200CS1	TSOP	4K	4K/64ms	
KMM372V3280CS1	TSOP	8K	4K/64ms	8K/64ms

- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(2100mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10*	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM372V3280CS1 (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref)
A0, B0, A1 - A12	Address Input(8K ref)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$, 1,4,5	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

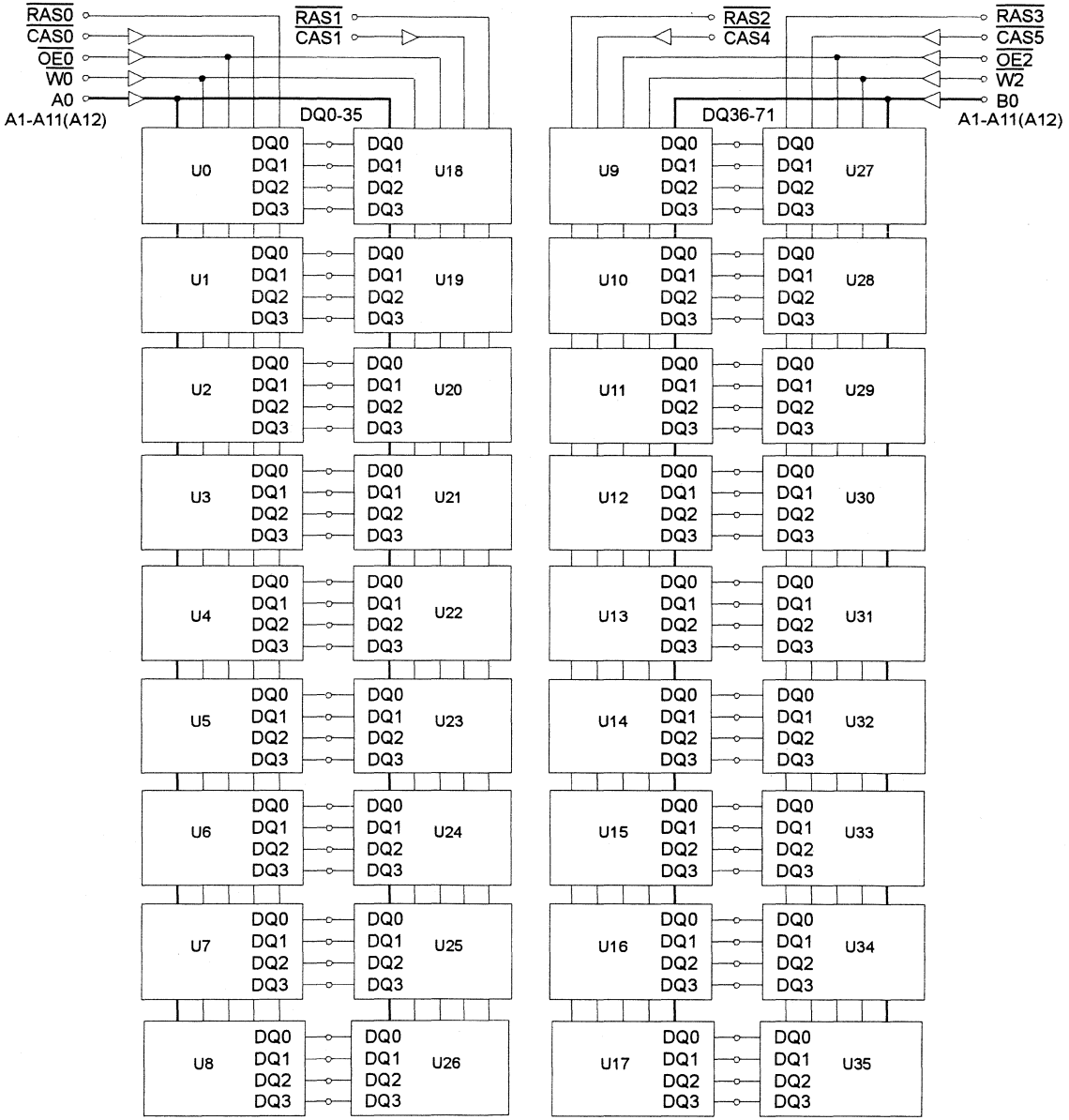
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	0	0
PD4	0	0
PD5	0	0
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

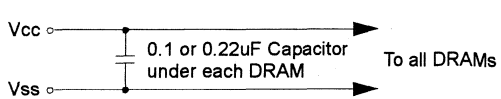
PD : 0 for Vol of Drive IC & 1 for N.C

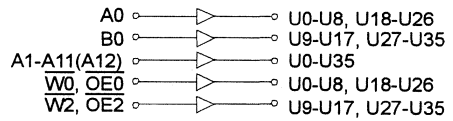
ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM372V3280CS1(8K Ref.)





ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	36	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V at pulse width≤15ns, which is measured at Vcc.
*2 : -1.3V at pulse width≤15ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372V3200CS1		KMM372V3280CS1		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	1998	-	1458	mA
	-6	-	1818	-	1278	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	1998	-	1458	mA
	-6	-	1818	-	1278	mA
I_{CC4}	-5	-	1098	-	1098	mA
	-6	-	918	-	918	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	1998	-	1998	mA
	-6	-	1818	-	1818	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-10	10	-10	10	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)
I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})
I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)
I_{CC4}*: Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)
I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)
I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)
$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)
$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)
V_{OH} : Output High Voltage Level (I_{OH} = -2mA)
V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	73	pF
Input capacitance[$\overline{CAS0}$, 1, 4, 5]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	24	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,11
Access time from column address	t_{AA}		30		35	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,11
Output buffer turn-off delay	t_{OFF}	5	18	5	20	ns	6,11
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	11
$\overline{CAS}$ hold time	t_{CSH}	48		58		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	11
Row address set-up time	t_{ASR}	5		5		ns	11
Row address hold time	t_{RAH}	8		8		ns	11
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	11
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referencde to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,11
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data in set-up time	t_{DS}	-2		-2		ns	9,11
Data in hold time	t_{DH}	15		15		ns	9,11
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ prechange to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7
$\overline{RAS}$ ro $\overline{W}$ delay time	t_{RWD}	71		83		ns	7,11

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	11
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	11
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3,11
Fast page mode cycle time	t_{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	76		85		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	11
$\overline{OE}$ access time	t_{OEA}		18		20	ns	11
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	11
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes tha $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

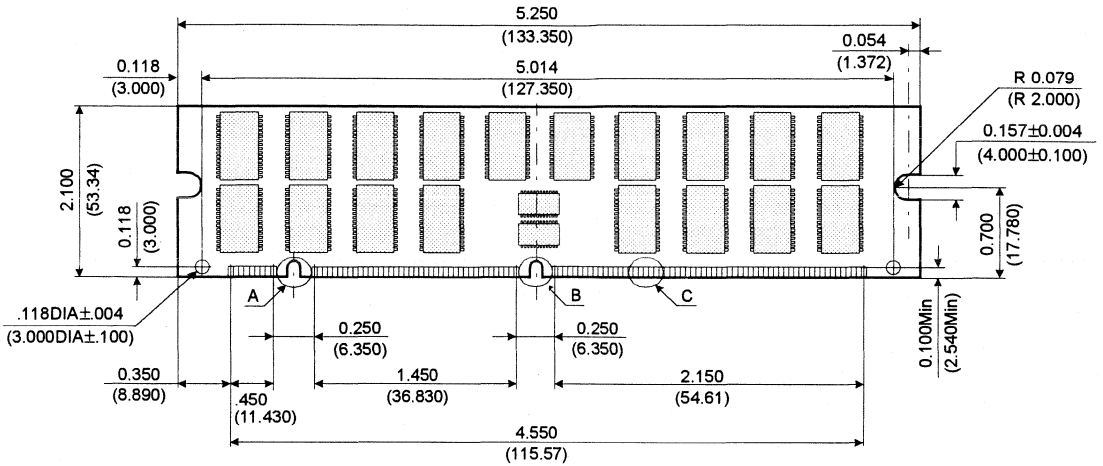
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

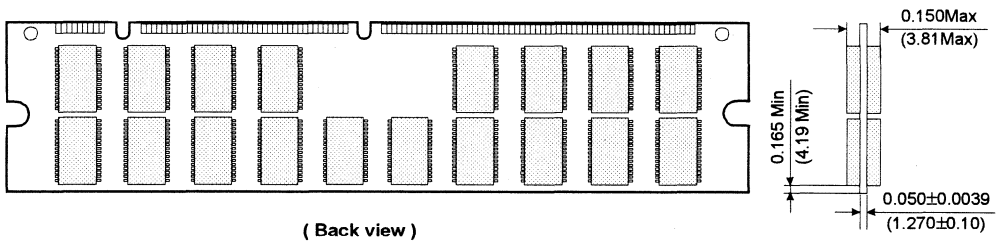
11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

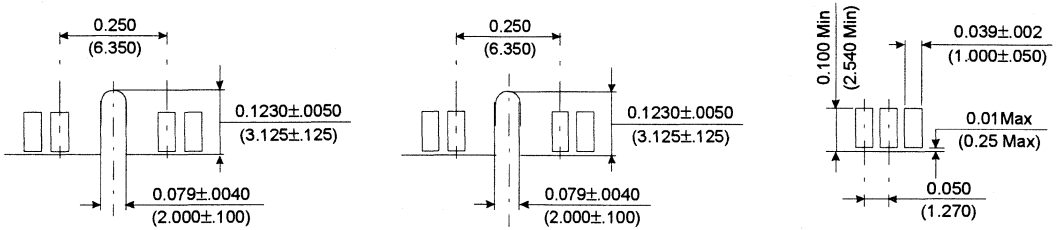
Units : Inches (millimeters)



(Front view)



(Back view)



Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx4 DRAM with Fast Page mode, TSOP II
DRAM Part No. : KMM372V3200CS1 - KM44V16100CS.
KMM372V3280CS1 - KM44V16000CS.

KMM372V320(8)0CK4 Fast Page Mode

32M x 72 DRAM DIMM with ECC Using 16Mx4, 4K & 8K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM372V320(8)0C is a 32Mx72bits Dynamic RAM high density memory module. The Samsung KMM372V320(8)0C consists of thirty-six CMOS 16Mx4bits DRAMs in SOJ 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372V320(8)0C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	18ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM372V3200CK4	SOJ	4K	4K/64ms	
KMM372V3280CK4	SOJ	8K	4K/64ms	8K/64ms

- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(2000mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM372V3280CK4 (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref)
A0, B0, A1 - A12	Address Input(8K ref)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$, 1,4,5	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

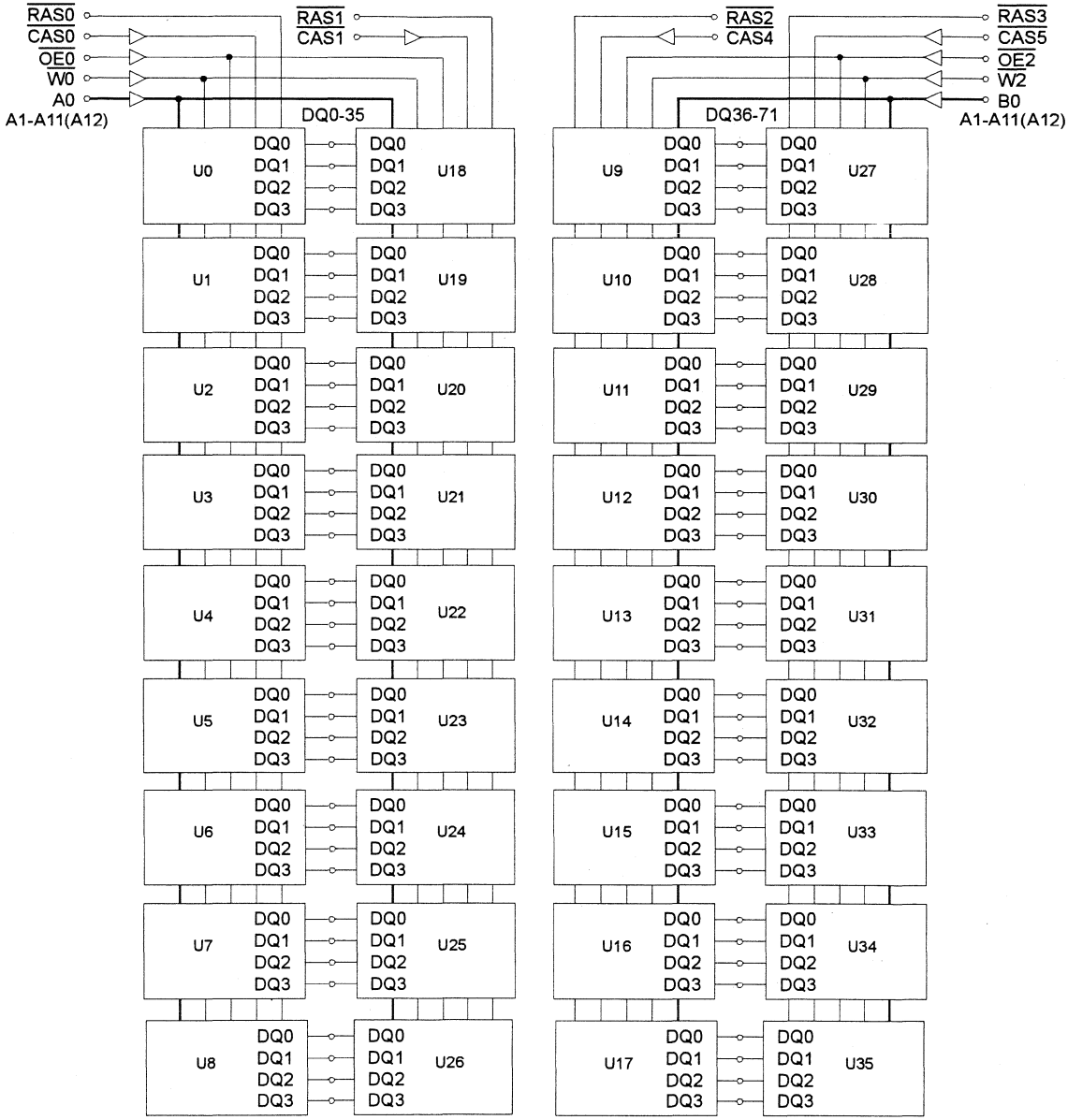
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	0	0
PD4	0	0
PD5	0	0
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

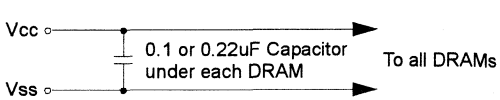
PD : 0 for Vol of Drive IC & 1 for N.C

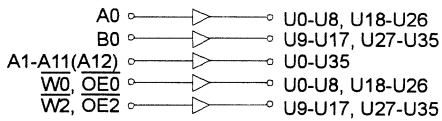
ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM372V3280CK4(8K Ref.)





4

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	36	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width≤15ns, which is measured at Vcc.
*2 : -1.3V at pulse width≤15ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speedl	KMM372V3200CK4		KMM372V3280CK4		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	1998	-	1458	mA
	-6	-	1818	-	1278	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	1998	-	1458	mA
	-6	-	1818	-	1278	mA
I_{CC4}	-5	-	1098	-	1098	mA
	-6	-	918	-	918	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	1998	-	1998	mA
	-6	-	1818	-	1818	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-10	10	-10	10	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0¡ÂVin¡ÂVcc+0.3V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	73	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS1,4,5}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	24	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,11
Access time from column address	t_{AA}		30		35	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,11
Output buffer turn-off delay	t_{OFF}	5	18	5	20	ns	6,11
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	11
$\overline{CAS}$ hold time	t_{CSH}	48		58		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	11
Row address set-up time	t_{ASR}	5		5		ns	11
Row address hold time	t_{RAH}	8		8		ns	11
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	11
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referencde to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,11
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data in set-up time	t_{DS}	-2		-2		ns	9,11
Data in hold time	t_{DH}	15		15		ns	9,11
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ prechange to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{RAS}$ ro $\overline{W}$ delay time	t_{RWD}	71		83		ns	7,11
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	11
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	11
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3,11
Fast page mode cycle time	t_{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	76		85		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	11
$\overline{OE}$ access time	t_{OEA}		18		20	ns	11
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	11
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes tha $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

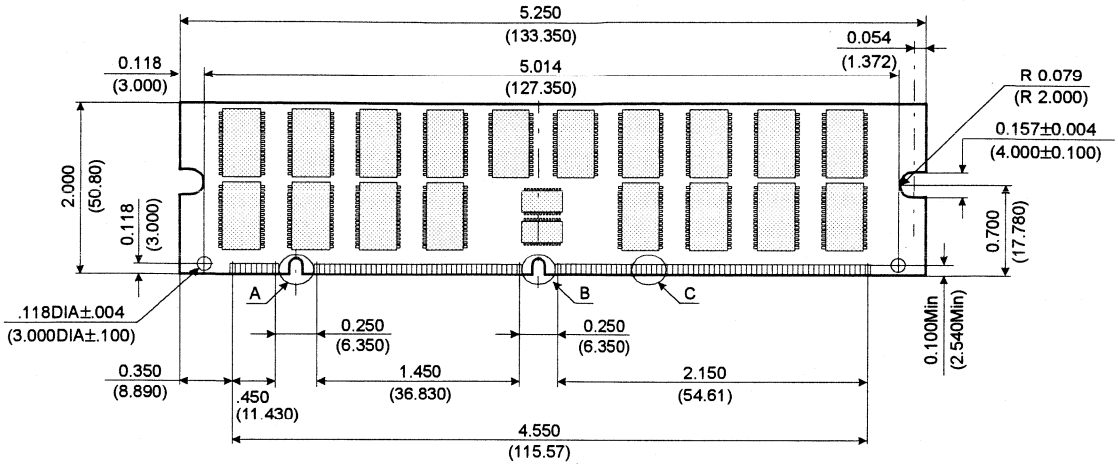
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

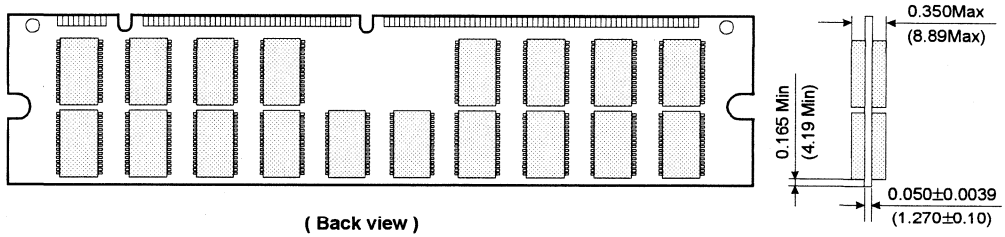
11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

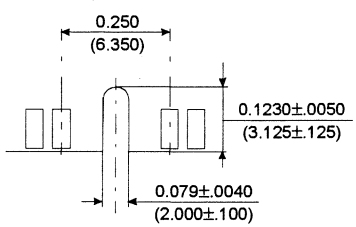
Units : Inches (millimeters)



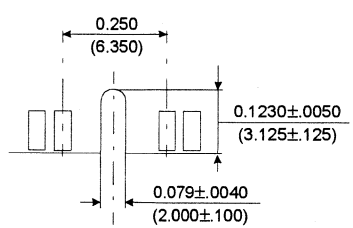
(Front view)



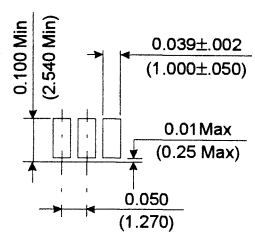
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx4 DRAM with Fast Page mode, SOJ
DRAM Part No. : KMM372V3200CK4 - KM44V16100CK.
KMM372V3280CK4 - KM44V16000CK.

KMM372V320(8)0CK3 Fast Page Mode

32M x 72 DRAM DIMM with ECC Using 16Mx4, 4K & 8K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM372V320(8)0C is a 32Mx72bits Dynamic RAM high density memory module. The Samsung KMM372V320(8)0C consists of thirty-six CMOS 16Mx4bits DRAMs in SOJ 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372V320(8)0C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	18ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM372V3200CK3	SOJ	4K	4K/64ms	
KMM372V3280CK3	SOJ	8K	4K/64ms	8K/64ms

- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1650mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM372V3280CK3 (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref)
A0, B0, A1 - A12	Address Input(8K ref)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$, 1,4,5	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

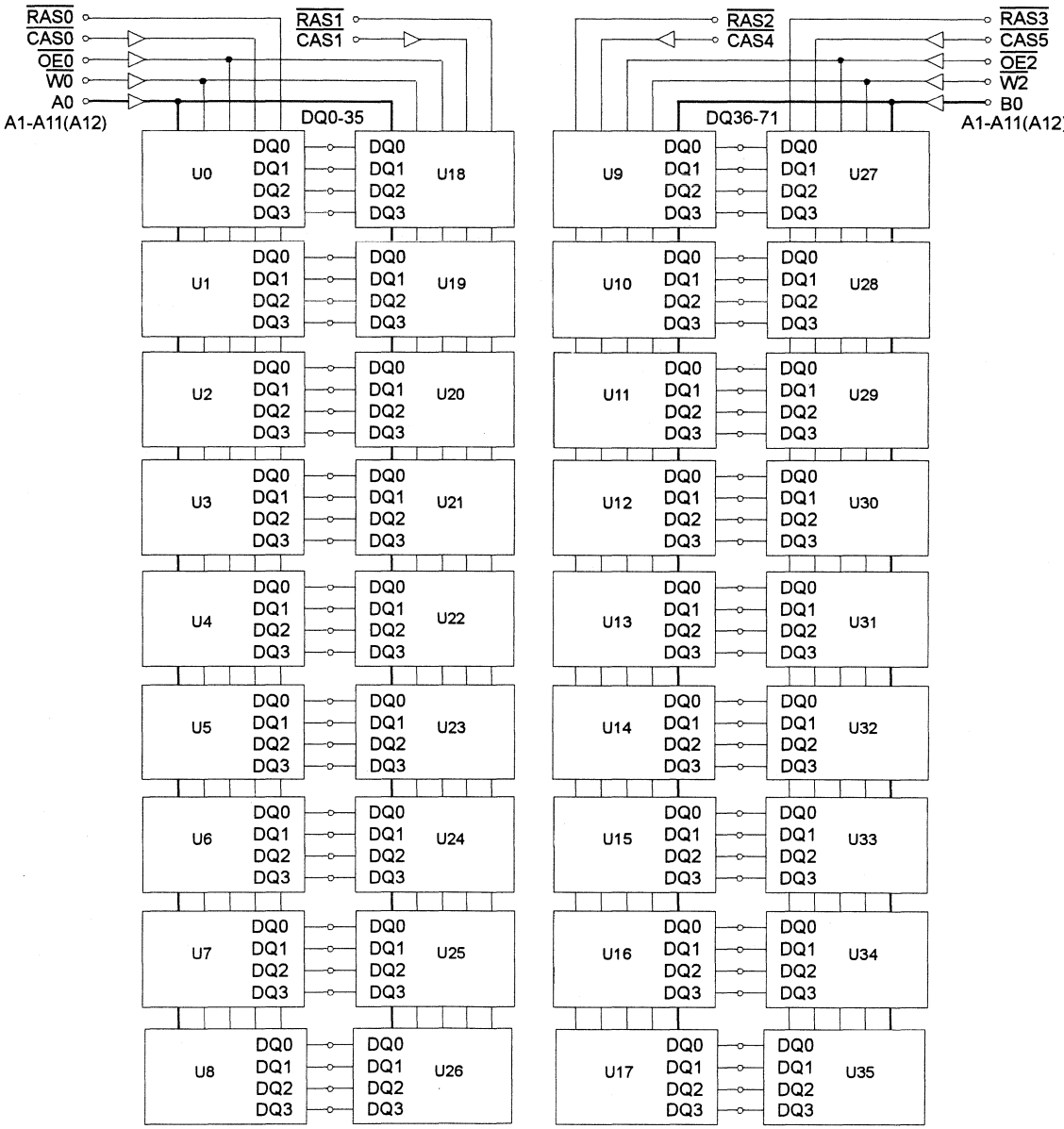
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	0	0
PD4	0	0
PD5	0	0
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

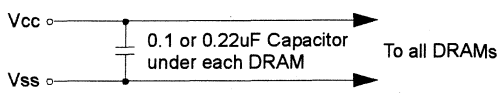
PD : 0 for Vol of Drive IC & 1 for N.C

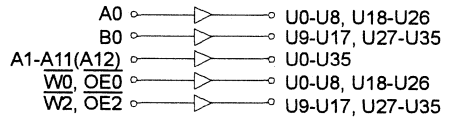
ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM372V3280CK3(8K Ref.)





ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	36	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width≤15ns, which is measured at Vcc.
*2 : -1.3V at pulse width≤15ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372V3200CK3		KMM372V3280CK3		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	1998	-	1458	mA
	-6	-	1818	-	1278	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	1998	-	1458	mA
	-6	-	1818	-	1278	mA
I_{CC4}	-5	-	1098	-	1098	mA
	-6	-	918	-	918	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	1998	-	1998	mA
	-6	-	1818	-	1818	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-10	10	-10	10	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}* : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)
I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})
I_{CC3}* : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)
I_{CC4}* : Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)
I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)
I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)
$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)
$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)
V_{OH} : Output High Voltage Level (I_{OH} = -2mA)
V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	73	pF
Input capacitance[$\overline{CAS0}$, 1, 4, 5]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	24	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,11
Access time from column address	t_{AA}		30		35	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,11
Output buffer turn-off delay	t_{OFF}	5	18	5	20	ns	6,11
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	11
$\overline{CAS}$ hold time	t_{CSH}	48		58		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	11
Row address set-up time	t_{ASR}	5		5		ns	11
Row address hold time	t_{RAH}	8		8		ns	11
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	11
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referencde to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,11
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data in set-up time	t_{DS}	-2		-2		ns	9,11
Data in hold time	t_{DH}	15		15		ns	9,11
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ prechange to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7

4

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{RAS}$ ro $\overline{W}$ delay time	t_{RWD}	71		83		ns	7,11
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	11
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	11
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3,11
Fast page mode cycle time	t_{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	76		85		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	11
$\overline{OE}$ access time	t_{OEA}		18		20	ns	11
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	11
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes tha $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

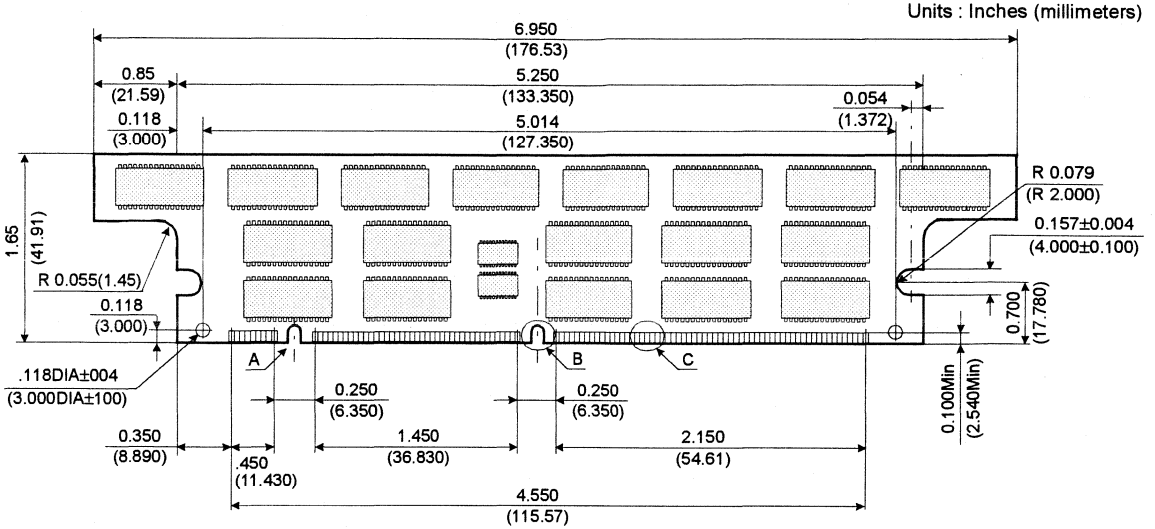
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

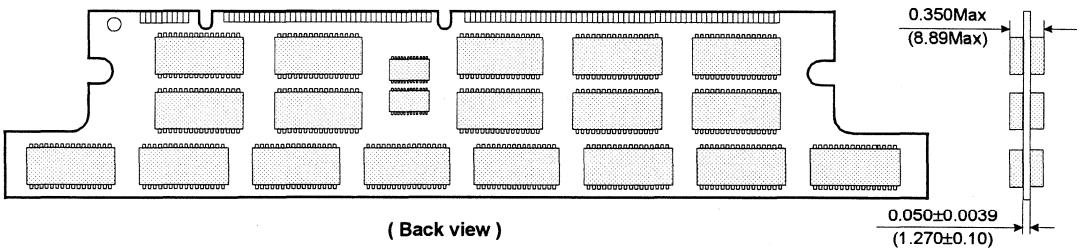
11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

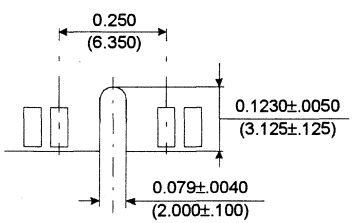
Units : Inches (millimeters)



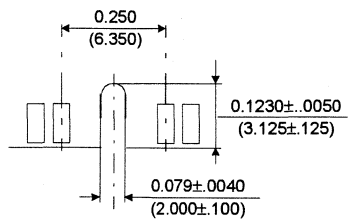
(Front view)



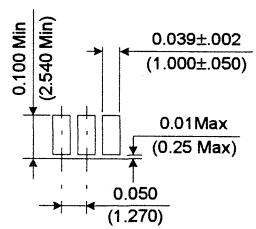
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx4 DRAM with Fast Page mode, SOJ
DRAM Part No. : KMM372V3200CK3 - KM44V16100CK.
KMM372V3280CK3 - KM44V16000CK.

KMM372F320(8)0CS1 EDO Mode

32M x 72 DRAM DIMM with ECC Using 16Mx4, 4K & 8K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM372F320(8)0C1 is a 32Mx72bits Dynamic RAM high density memory module. The Samsung KMM372F320(8)0C1 consists of thirty-six CMOS 16Mx4bits DRAMs in TSOP 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372F320(8)0C1 is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	18ns	84ns	20ns
-6	60ns	20ns	104ns	25ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM372F3200CS1	TSOP	4K	4K/64ms	
KMM372F3280CS1	TSOP	8K	4K/64ms	8K/64ms

- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(2100mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM372F3280CS1 (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref)
A0, B0, A1 - A12	Address Input(8K ref)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$, 1,4,5	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

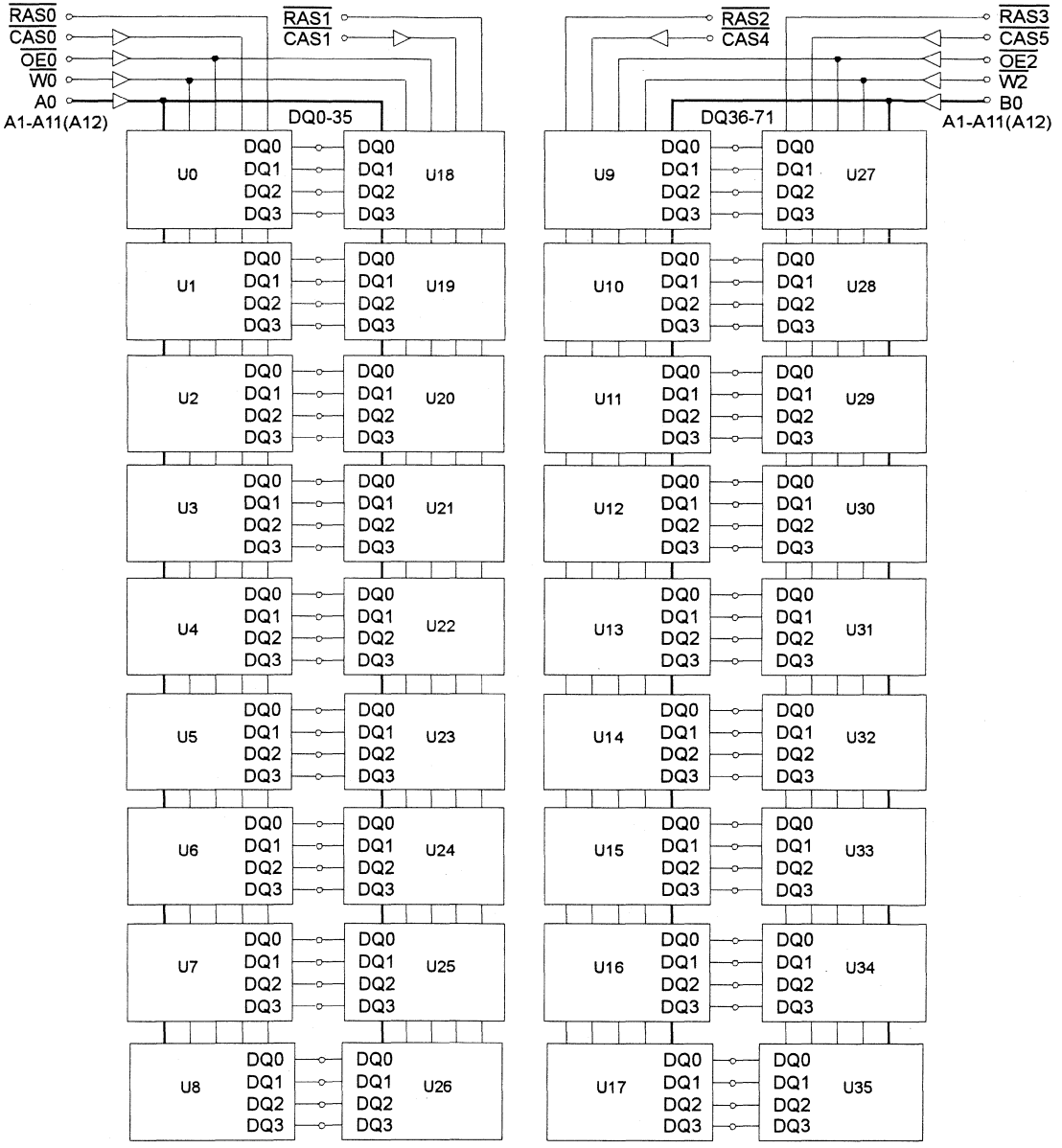
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	0	0
PD4	0	0
PD5	1	1
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

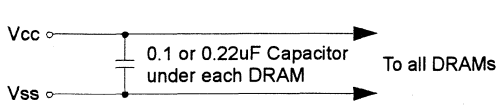
PD : 0 for Vol of Drive IC & 1 for N.C

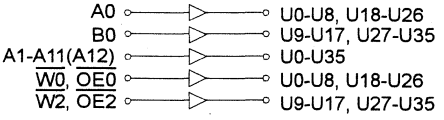
ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM372F3280CS1(8K Ref.)





4

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	36	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width≤15ns, which is measured at Vcc.
*2 : -1.3V at pulse width≤15ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372F3200CS1		KMM372F3280CS1		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	1998	-	1458	mA
	-6	-	1818	-	1278	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	1998	-	1458	mA
	-6	-	1818	-	1278	mA
I_{CC4}	-5	-	1638	-	1638	mA
	-6	-	1458	-	1458	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	1998	-	1998	mA
	-6	-	1818	-	1818	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-10	10	-10	10	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	73	pF
Input capacitance[$\overline{CAS0}$, 1,4,5]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	24	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	128		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,13
Access time from column address	t_{AA}		30		35	ns	3,10,13
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,13
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,13
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	18	ns	6,11,13
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	13
$\overline{CAS}$ hold time	t_{CSH}	36		38		ns	13
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	15	32	18	40	ns	4,13
$\overline{RAS}$ to column address delay time	t_{RAD}	10	20	13	25	ns	10,13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	13
Row address set-up time	t_{ASR}	5		5		ns	13
Row address hold time	t_{RAH}	5		8		ns	13
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	7		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	13
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,13
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	7		10		ns	
Write command pulse width	t_{WP}	7		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	13
Write command to $\overline{CAS}$ lead time	t_{CWL}	7		10		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,13
Data hold time	t_{DH}	13		15		ns	9,13
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	33		38		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	68		82		ns	7,13

4

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	45		53		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	47		58		ns	
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	13
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	13
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,13
Hyper page cycle time	t_{HPC}	20		25		ns	12
Hyper page read-modify-write cycle time	t_{HPRWC}	70		77		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	7		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	13
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	13
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	13
$\overline{OE}$ access time	t_{OEA}		18		20	ns	13
$\overline{OE}$ to data delay	t_{OED}	15		18		ns	13
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	8	18	8	18	ns	13
$\overline{OE}$ command hold time	t_{OEH}	5		5		ns	
Output data hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{DOH}	10		10		ns	13
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	13	3	13	ns	6,11
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	8	18	8	18	ns	6,13
$\overline{W}$ to data delay	t_{WED}	20		20		ns	13
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes tha $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

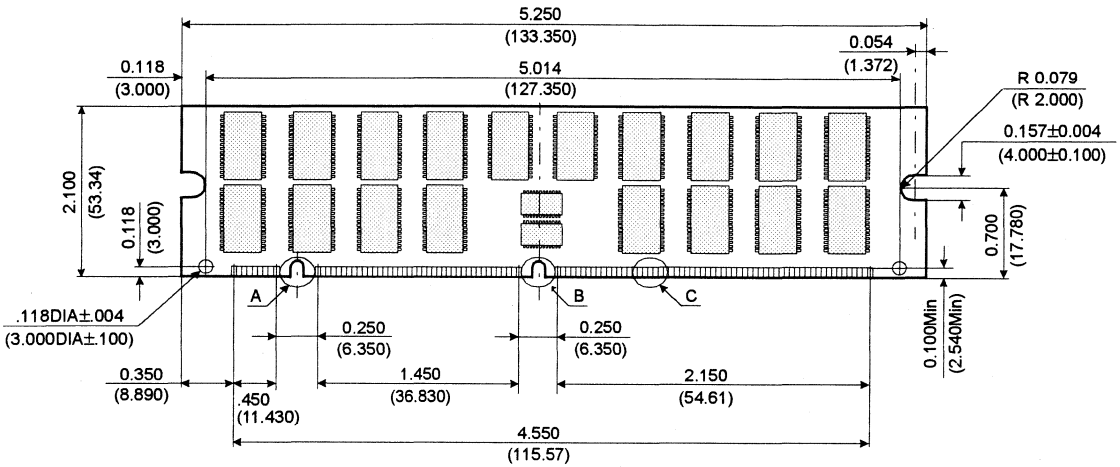
12. $t_{ASC} \geq 6$ns.

13. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

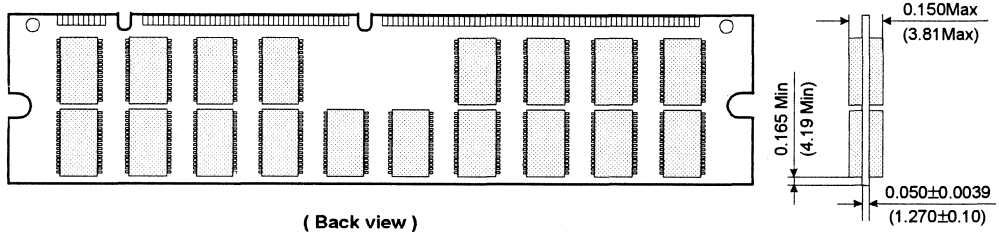
4

PACKAGE DIMENSIONS

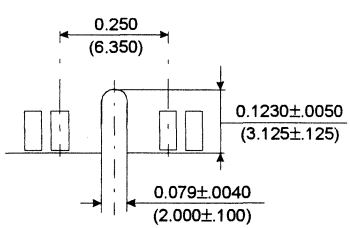
Units : Inches (millimeters)



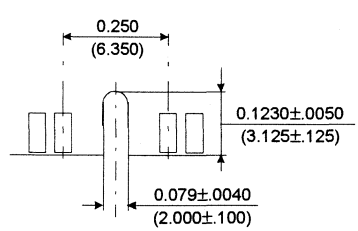
(Front view)



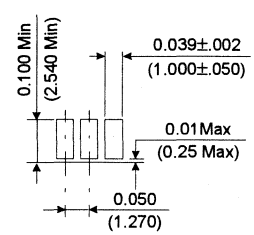
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx4 DRAM with EDO mode, TSOP II.
DRAM Part No. : KMM372F3200CS1 - KM44V16104CS.
KMM372F3280CS1 - KM44V16004CS.

KMM372F320(8)0CK4 EDO Mode

32M x 72 DRAM DIMM with ECC Using 16Mx4, 4K & 8K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM372F320(8)0CK4 is a 32Mx72bits Dynamic RAM high density memory module. The Samsung KMM372F320(8)0CK4 consists of thirty-six CMOS 16Mx4bits DRAMs in SOJ 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372F320(8)0CK4 is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	18ns	84ns	20ns
-6	60ns	20ns	104ns	25ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM372F3200CK4	SOJ	4K	4K/64ms	
KMM372F3280CK4	SOJ	8K	4K/64ms	8K/64ms

- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(2000mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM372F3280CK4 (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref)
A0, B0, A1 - A12	Address Input(8K ref)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$, 1,4,5	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

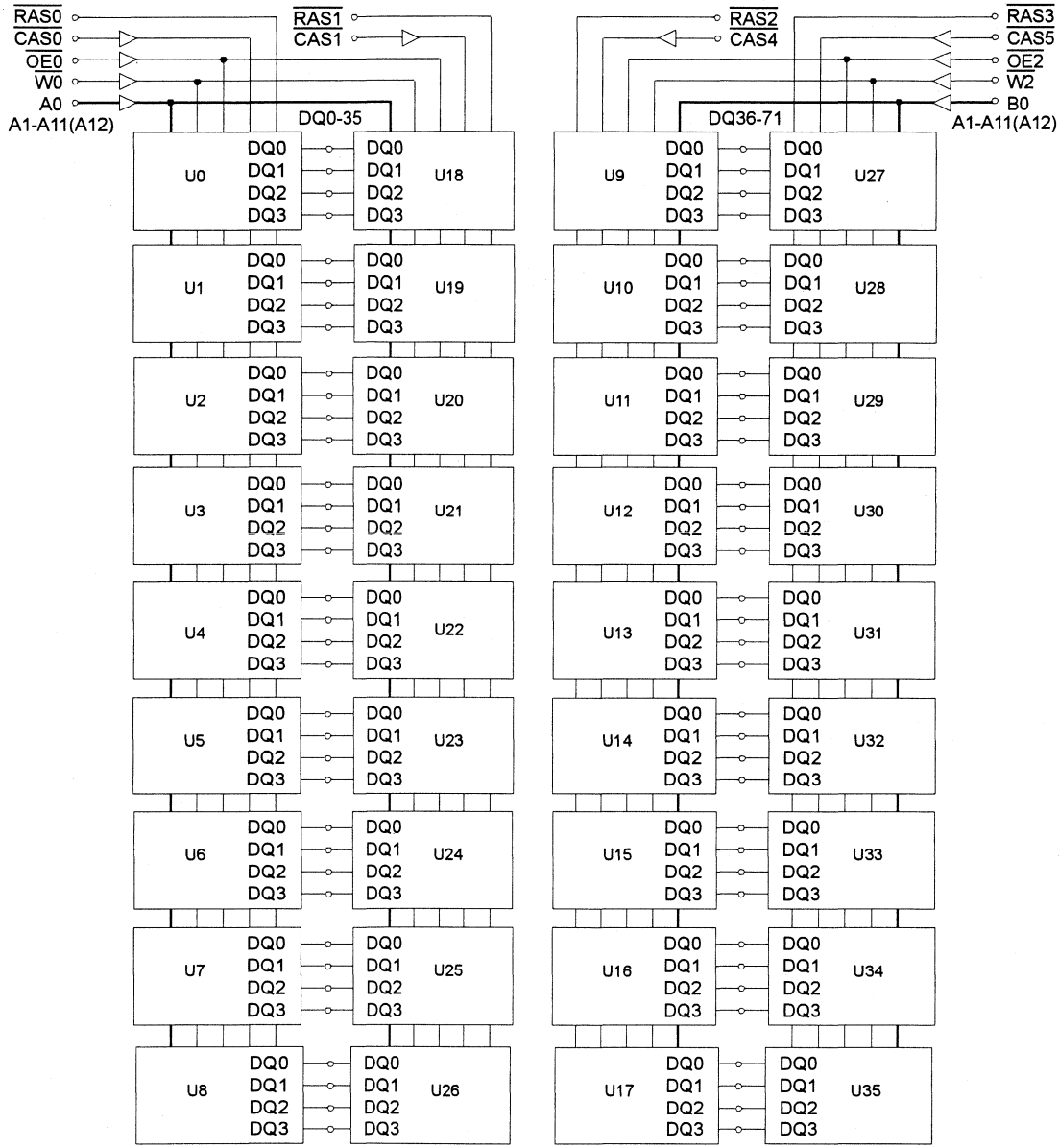
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	0	0
PD4	0	0
PD5	1	1
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

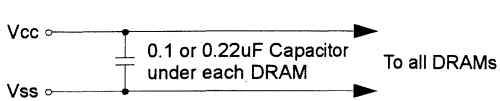
PD : 0 for Vol of Drive IC & 1 for N.C

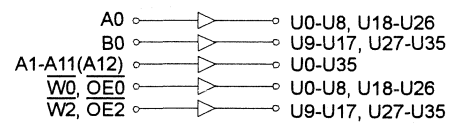
ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM372F3280CK4(8K Ref.)





ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	36	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V at pulse width≤15ns, which is measured at V_{CC}.
*2 : -1.3V at pulse width≤15ns, which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372F3200CK4		KMM372F3280CK4		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	1998	-	1458	mA
	-6	-	1818	-	1278	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	1998	-	1458	mA
	-6	-	1818	-	1278	mA
I_{CC4}	-5	-	1638	-	1638	mA
	-6	-	1458	-	1458	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	1998	-	1998	mA
	-6	-	1818	-	1818	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-10	10	-10	10	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	73	pF
Input capacitance[$\overline{CAS0}$, 1,4,5]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	24	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	128		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,13
Access time from column address	t_{AA}		30		35	ns	3,10,13
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,13
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,13
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	18	ns	6,11,13
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	13
$\overline{CAS}$ hold time	t_{CSH}	36		38		ns	13
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	15	32	18	40	ns	4,13
$\overline{RAS}$ to column address delay time	t_{RAD}	10	20	13	25	ns	10,13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	13
Row address set-up time	t_{ASR}	5		5		ns	13
Row address hold time	t_{RAH}	5		8		ns	13
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	7		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	13
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,13
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	7		10		ns	
Write command pulse width	t_{WP}	7		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	13
Write command to $\overline{CAS}$ lead time	t_{CWL}	7		10		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,13
Data hold time	t_{DH}	13		15		ns	9,13
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
$\overline{CAS}$ to $\overline{W}$ dealy time	t_{CWD}	33		38		ns	7
$\overline{RAS}$ to $\overline{W}$ dealy time	t_{RWD}	68		82		ns	7,13

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	45		53		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	47		58		ns	
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	13
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	13
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,13
Hyper page cycle time	t_{HPC}	20		25		ns	12
Hyper page read-modify-write cycle time	t_{HPRWC}	70		77		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	7		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	13
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	13
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	13
$\overline{OE}$ access time	t_{OEA}		18		20	ns	13
$\overline{OE}$ to data delay	t_{OED}	15		18		ns	13
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	8	18	8	18	ns	13
$\overline{OE}$ command hold time	t_{OEH}	5		5		ns	
Output data hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{DOH}	10		10		ns	13
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	13	3	13	ns	6,11
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	8	18	8	18	ns	6,13
$\overline{W}$ to data delay	t_{WED}	20		20		ns	13
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes tha $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

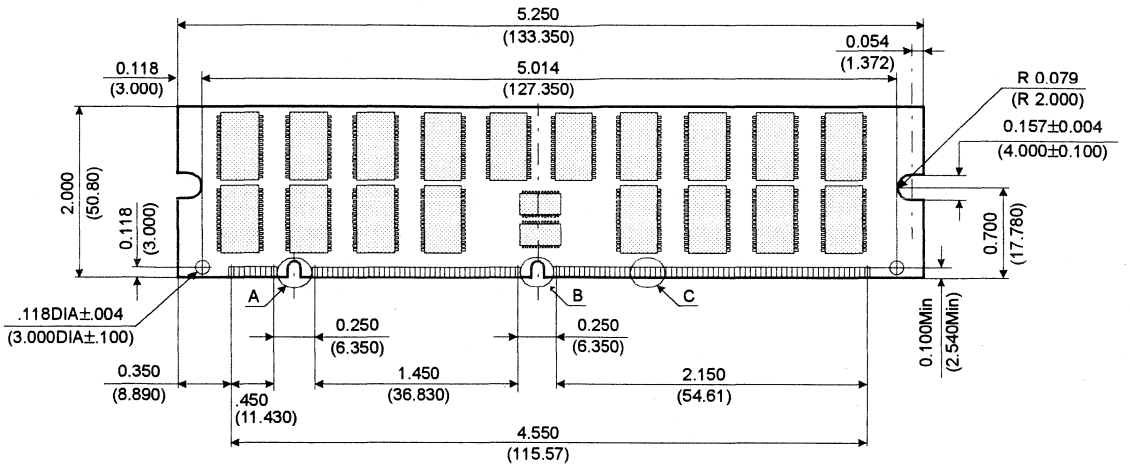
11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

12. $t_{ASC} \geq 6$ns.

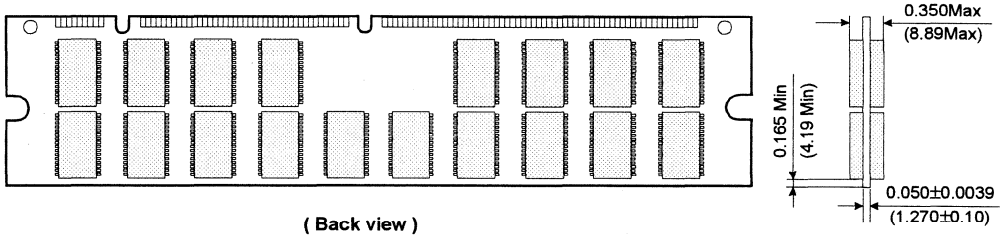
13. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

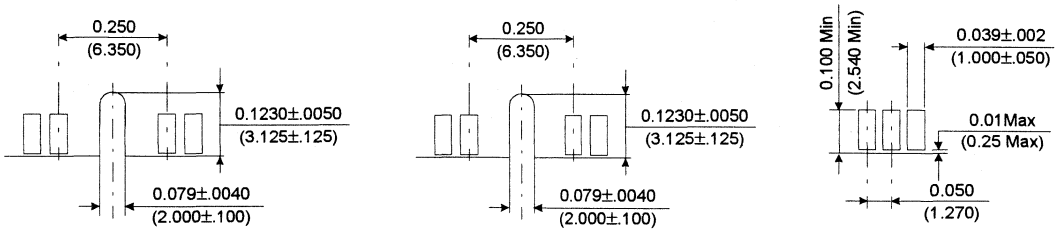
Units : Inches (millimeters)



(Front view)



(Back view)



Detail A Detail B Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx4 DRAM with EDO mode, SOJ.
DRAM Part No. : KMM372F3200CK4 - KM44V16104CK.
KMM372F3280CK4 - KM44V16004CK.

KMM372F320(8)0CK3 EDO Mode

32M x 72 DRAM DIMM with ECC Using 16Mx4, 4K & 8K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM372F320(8)0C is a 32Mx72bits Dynamic RAM high density memory module. The Samsung KMM372F320(8)0C consists of thirty-six CMOS 16Mx4bits DRAMs in SOJ 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372F320(8)0C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	18ns	84ns	20ns
-6	60ns	20ns	104ns	25ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM372F3200CK3	SOJ	4K	4K/64ms	
KMM372F3280CK3	SOJ	8K	4K/64ms	8K/64ms

- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1650mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM372F3280CK3 (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
A0, B0, A1 - A12	Address Input(8K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$, 1,4,5	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

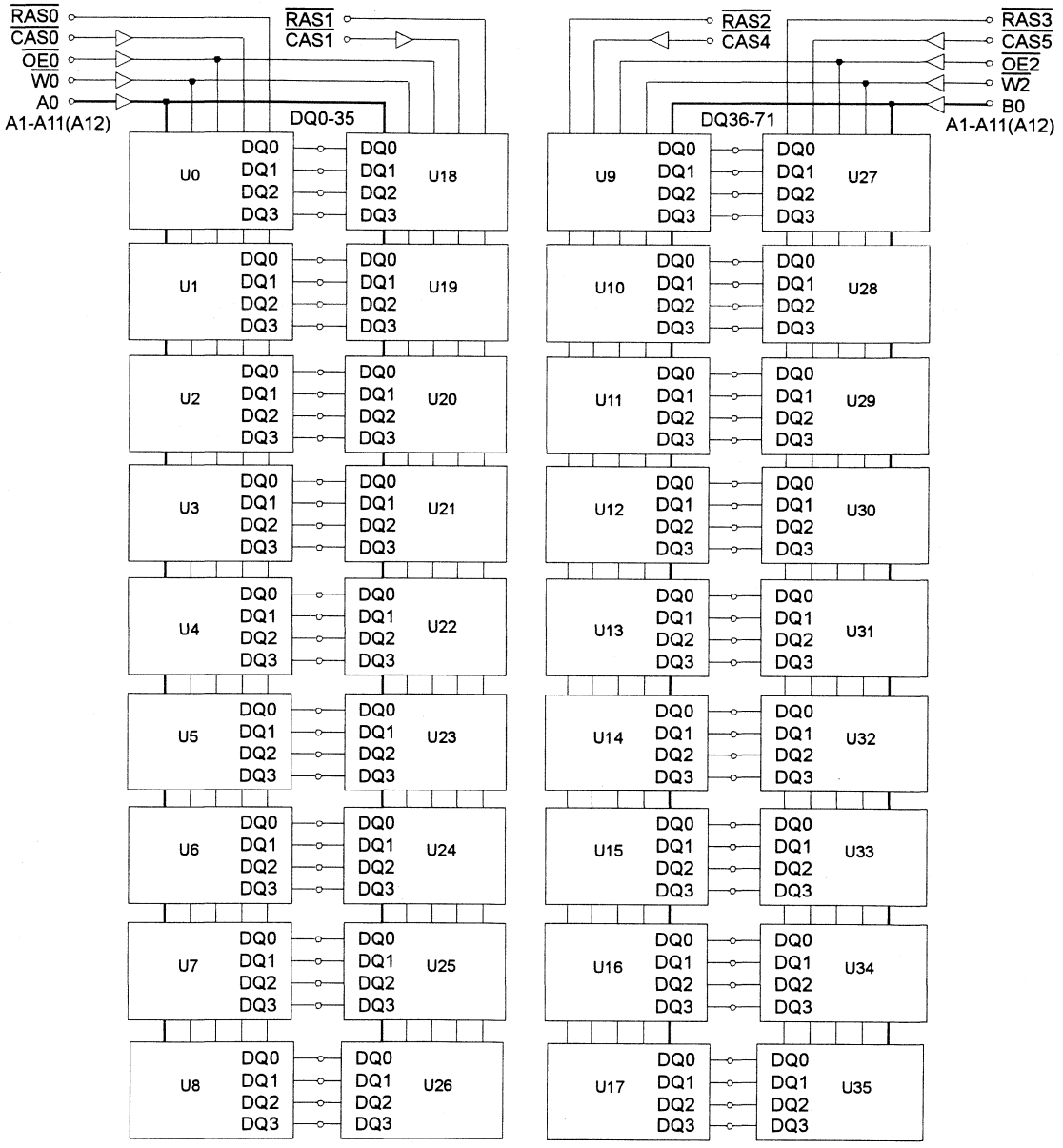
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	0	0
PD4	0	0
PD5	1	1
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

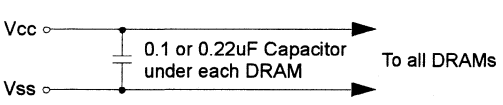
PD : 0 for Vol of Drive IC & 1 for N.C

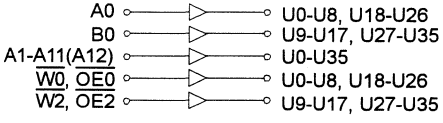
ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM372F3280CK3(8K Ref.)





4

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	36	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width≤15ns, which is measured at Vcc.
*2 : -1.3V at pulse width≤15ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372F3200CK3		KMM372F3280CK3		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	1998	-	1458	mA
	-6	-	1818	-	1278	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	1998	-	1458	mA
	-6	-	1818	-	1278	mA
I_{CC4}	-5	-	1638	-	1638	mA
	-6	-	1458	-	1458	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	1998	-	1998	mA
	-6	-	1818	-	1818	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-10	10	-10	10	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	73	pF
Input capacitance[$\overline{CAS0}$, 1,4,5]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	24	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	128		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,13
Access time from column address	t_{AA}		30		35	ns	3,10,13
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,13
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,13
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	18	ns	6,11,13
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	13
$\overline{CAS}$ hold time	t_{CSH}	36		38		ns	13
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	15	32	18	40	ns	4,13
$\overline{RAS}$ to column address delay time	t_{RAD}	10	20	13	25	ns	10,13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	13
Row address set-up time	t_{ASR}	5		5		ns	13
Row address hold time	t_{RAH}	5		8		ns	13
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	7		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	13
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,13
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	7		10		ns	
Write command pulse width	t_{WP}	7		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	13
Write command to $\overline{CAS}$ lead time	t_{CWL}	7		10		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,13
Data hold time	t_{DH}	13		15		ns	9,13
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	33		38		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	68		82		ns	7,13

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	45		53		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	47		58		ns	
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	13
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	13
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,13
Hyper page cycle time	t_{HPC}	20		25		ns	12
Hyper page read-modify-write cycle time	t_{HPRWC}	70		77		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	13
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	13
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	13
$\overline{OE}$ access time	t_{OEA}		18		20	ns	13
$\overline{OE}$ to data delay	t_{OED}	15		18		ns	13
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	8	18	8	18	ns	13
$\overline{OE}$ command hold time	t_{OEH}	5		5		ns	
Output data hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{DOH}	10		10		ns	13
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	13	3	13	ns	6,11
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	8	18	8	18	ns	6,13
$\overline{W}$ to data delay	t_{WED}	20		20		ns	13
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes tha $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

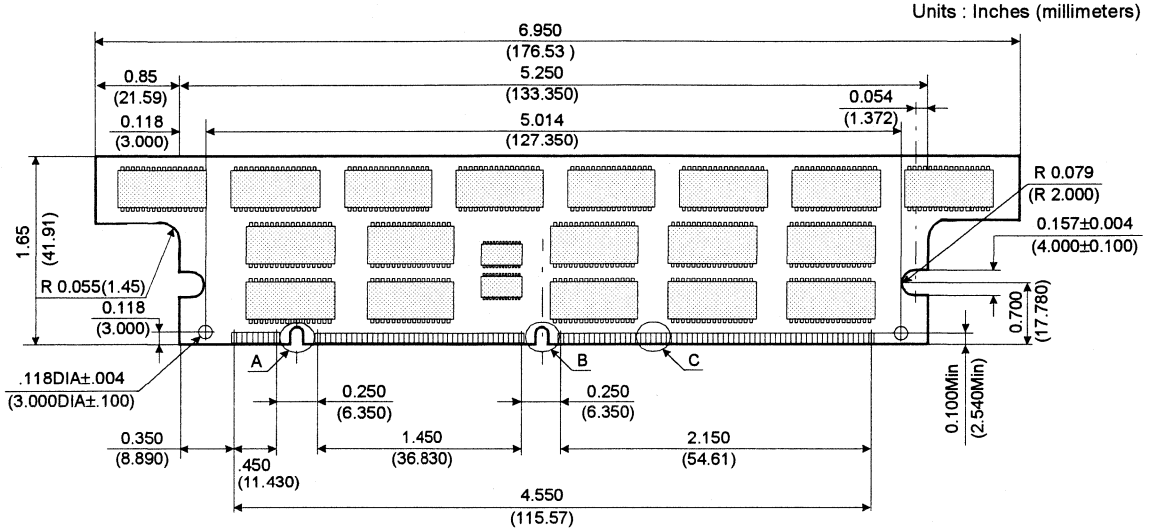
12. $t_{ASC} \geq 6$ns.

13. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

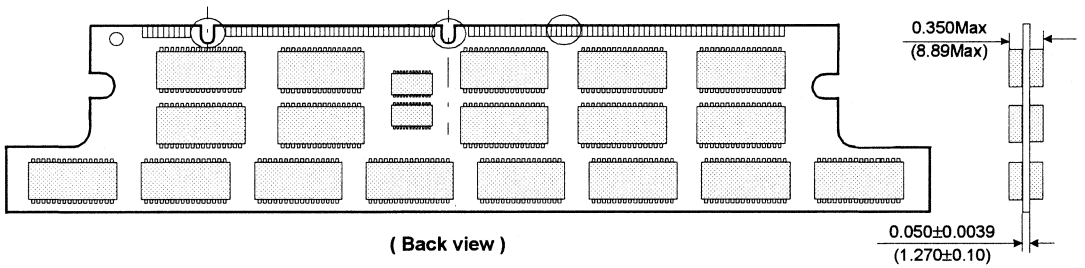
4

PACKAGE DIMENSIONS

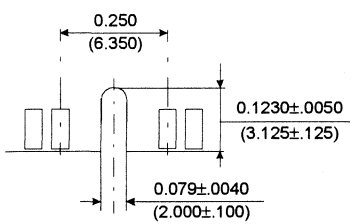
Units : Inches (millimeters)



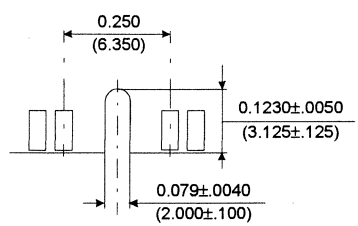
(Front view)



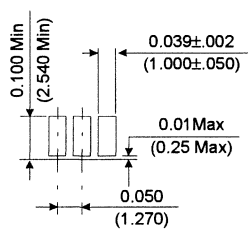
(Back view)



Detail A



Detail B

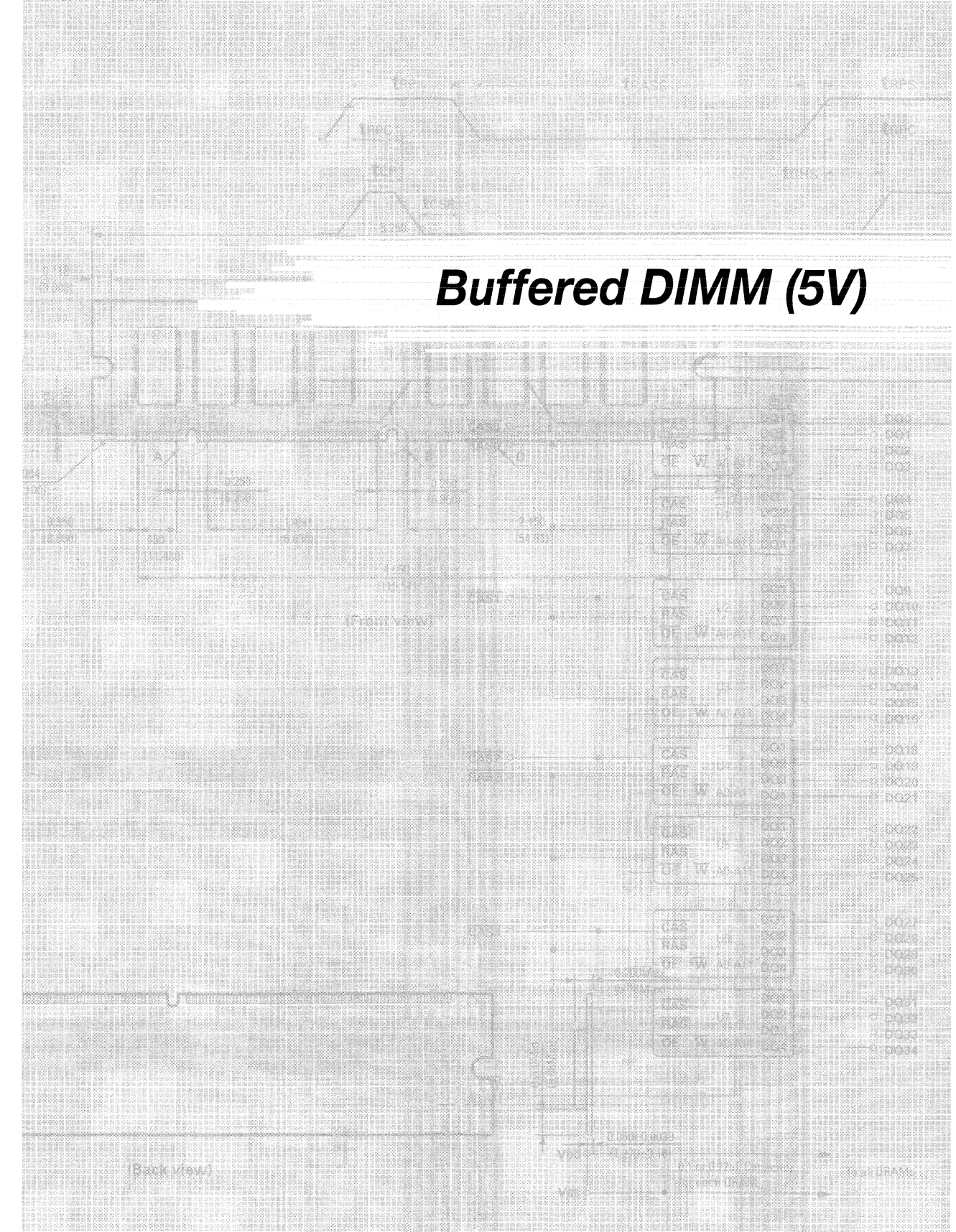


Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx4 DRAM with EDO mode, SOJ.
DRAM Part No. : KMM372F3200CK3 - KM44V16104CK.
KMM372F3280CK3 - KM44V16004CK.

Buffered DIMM (5V)



KMM364C124CJ Fast Page Mode

1M x 64 DRAM DIMM using 1Mx16, 1K Refresh , 5V

GENERAL DESCRIPTION

The Samsung KMM364C124C is a 1Mx64bits Dynamic RAM high density memory module. The Samsung KMM364C124C consists of four CMOS 1Mx16bits DRAMs in 42-pin SOJ 400mil package, and two 16bits driver IC in 48pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM364C124C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	tRAC	tCAC	tRC	tPC
-5	50ns	20ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

FEATURES

- Part Identification
  - KMM364C124CJ (1024 cycles/16ms Ref. SOJ)
- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS2}$	57	DQ22	85	Vss	113	$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	*A10	66	*DQ26	94	DQ43	122	*A11	150	*DQ62
11	*DQ8	39	*A12	67	DQ27	95	*DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	$\overline{RFU}$	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	$\overline{CAS6}$	75	DQ33	103	DQ50	131	$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	*DQ35	105	DQ52	133	Vcc	161	*DQ71
22	*DQ17	50	RSVD	78	Vss	106	*DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	$\overline{RFU}$	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

PD Note : PD & ID Terminals must each be pulled up through a resister to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A9	Address Input
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ ~ $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

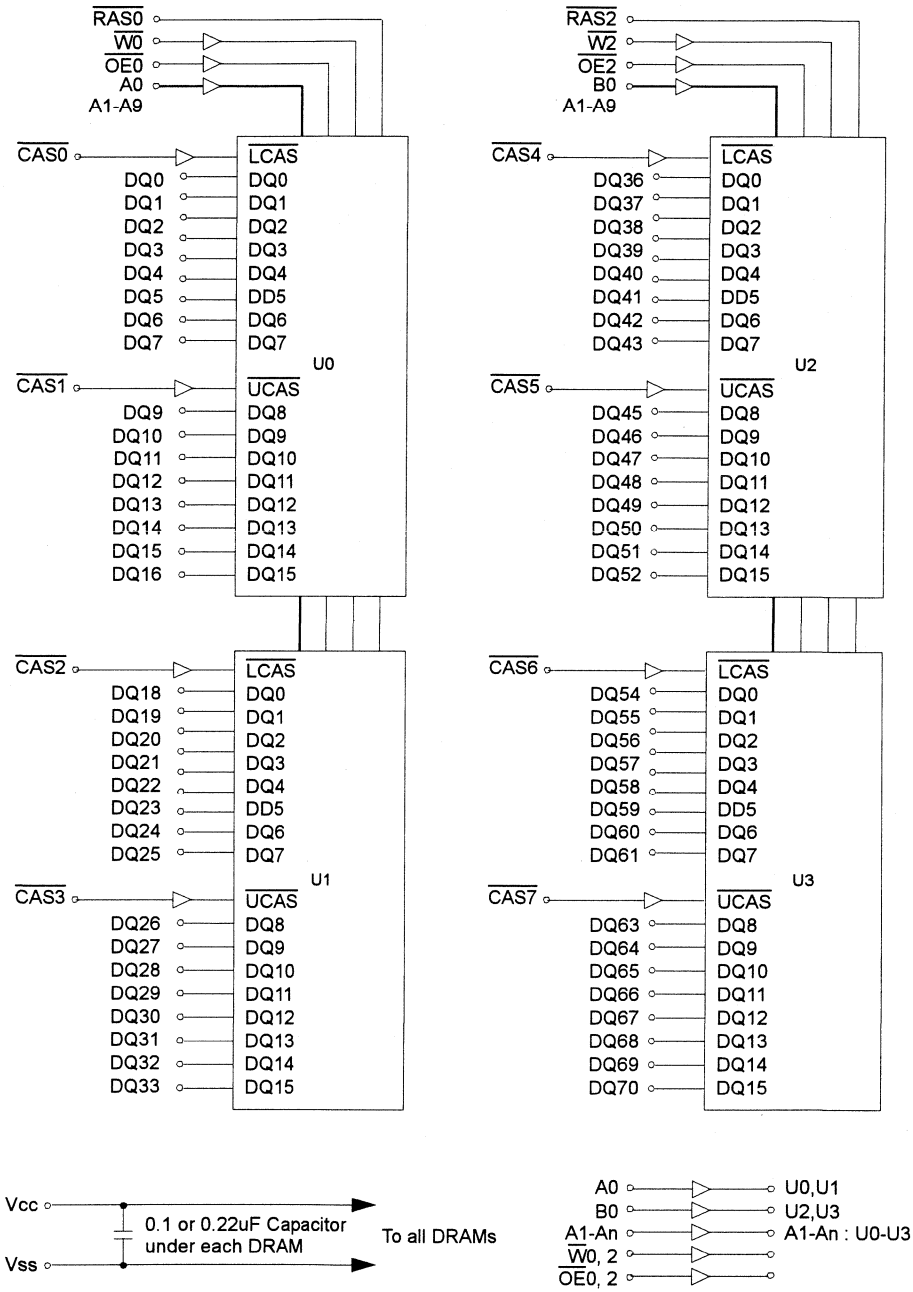
PD & ID Table

Pin	50NS	60NS
PD1	0	0
PD2	0	0
PD3	1	1
PD4	0	0
PD5	0	0
PD6	0	1
PD7	0	1
PD8	1	1
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	4	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V/20ns, Pulse width is measured at Vcc.
*2 : -2.0V/20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM364C124CJ		Unit
		Min	Max	
I_{CC1}	-5 -6	- -	560 520	mA mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-5 -6	- -	560 520	mA mA
I_{CC4}	-5 -6	- -	360 320	mA mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-5 -6	- -	560 520	mA mA
$I_{I(L)}$ $I_{O(L)}$	Don't care	-10 -5	10 5	uA uA
V_{OH} V_{OL}	Don't care	2.4 -	- 0.4	V V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)
I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})
I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)
I_{CC4}*: Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)
I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)
I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)
$I_{I(L)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)
$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)
V_{OH} : Output High Voltage Level (I_{OH} = -5mA)
V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one page mode cycle, t_{PC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A9, B0]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	25	pF
Input capacitance[$\overline{CAS0}$ ~ $\overline{CAS7}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ1}	-	25	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		20		20	ns	3,4,5,11
Access time from column address	t_{AA}		30		35	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,11
Output buffer turn-off delay	t_{OFF}	5	18	5	20	ns	6,11
Transition time(rise and fall)	t_T	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	11
$\overline{CAS}$ hold time	t_{CSH}	48		58		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	11
Row address set-up time	t_{ASR}	5		5		ns	11
Row address hold time	t_{RAH}	8		8		ns	11
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	11
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,11
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,11
Data hold time	t_{DH}	20		20		ns	9,11
Refresh period	t_{REF}		16		16	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	71		83		ns	7,11
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	11
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	11
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	3		3		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3,11
Fast page mode cycle time	t_{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	76		80		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	t_{RASP}	50	100K	60	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	8		8		ns	11
$\overline{OE}$ access time	t_{OEA}		18		20	ns	
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	11
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	11
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS} is not restrictive operating parameter. It included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

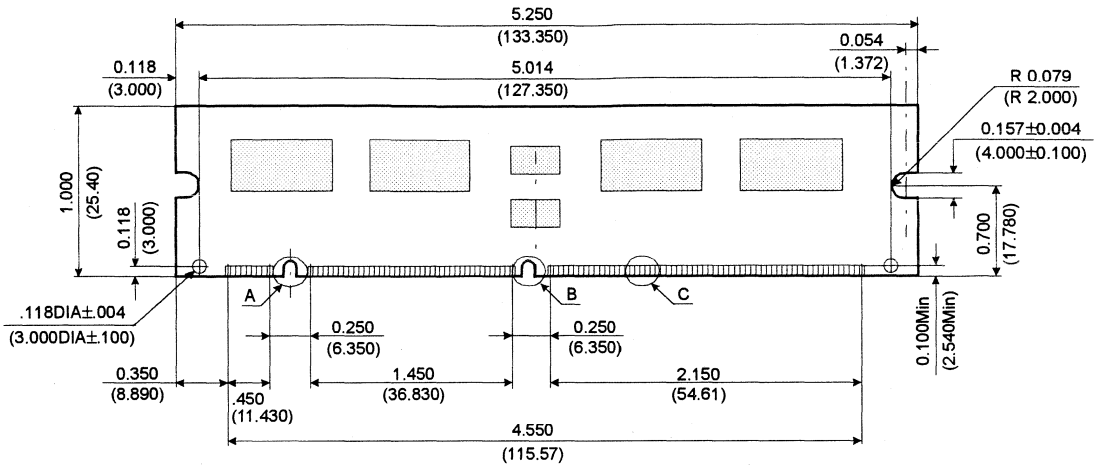
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

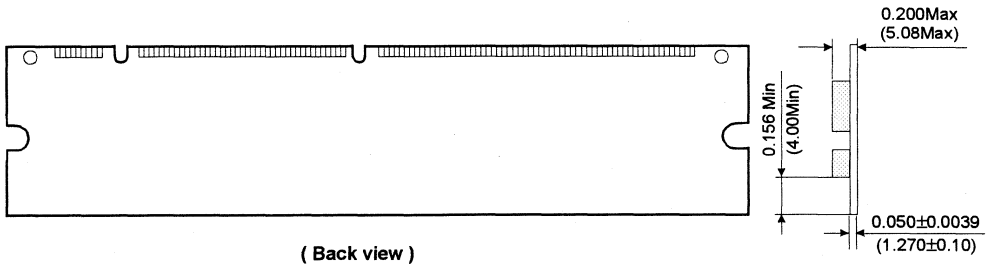
11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

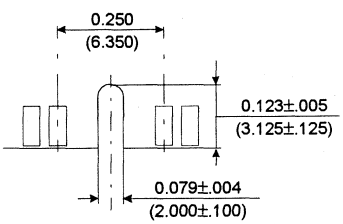
Units : Inches (millimeters)



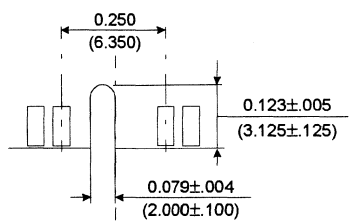
(Front view)



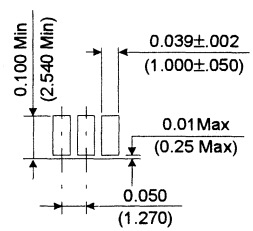
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 1Mx16 DRAM with Fast Page mode, SOJ.
DRAM Part No. : KMM364C124CJ - KM416C1200CJ.

KMM364E124CJ EDO Mode

1M x 64 DRAM DIMM using 1Mx16, 1K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM364E124CJ is a 1Mx64bits Dynamic RAM high density memory module. The Samsung KMM364E124CJ consists of four CMOS 1Mx16bits DRAMs in 42-pin SOJ 400mil package, and two 16bits driver IC in 48pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM364E124CJ is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	20ns	84ns	20ns
-6	60ns	22ns	104ns	25ns

FEATURES

- Part Identification
  - KMM364E124CJ (1024 cycles/16ms Ref., SOJ)
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS2}$	57	DQ22	85	Vss	113	$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	*A10	66	*DQ26	94	DQ43	122	*A11	150	*DQ62
11	*DQ8	39	*A12	67	DQ27	95	*DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	$\overline{CAS6}$	75	DQ33	103	DQ50	131	$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	*DQ35	105	DQ52	133	Vcc	161	*DQ71
22	*DQ17	50	RSVD	78	Vss	106	*DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

PD Note : PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A9	Address Input
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ ~ $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

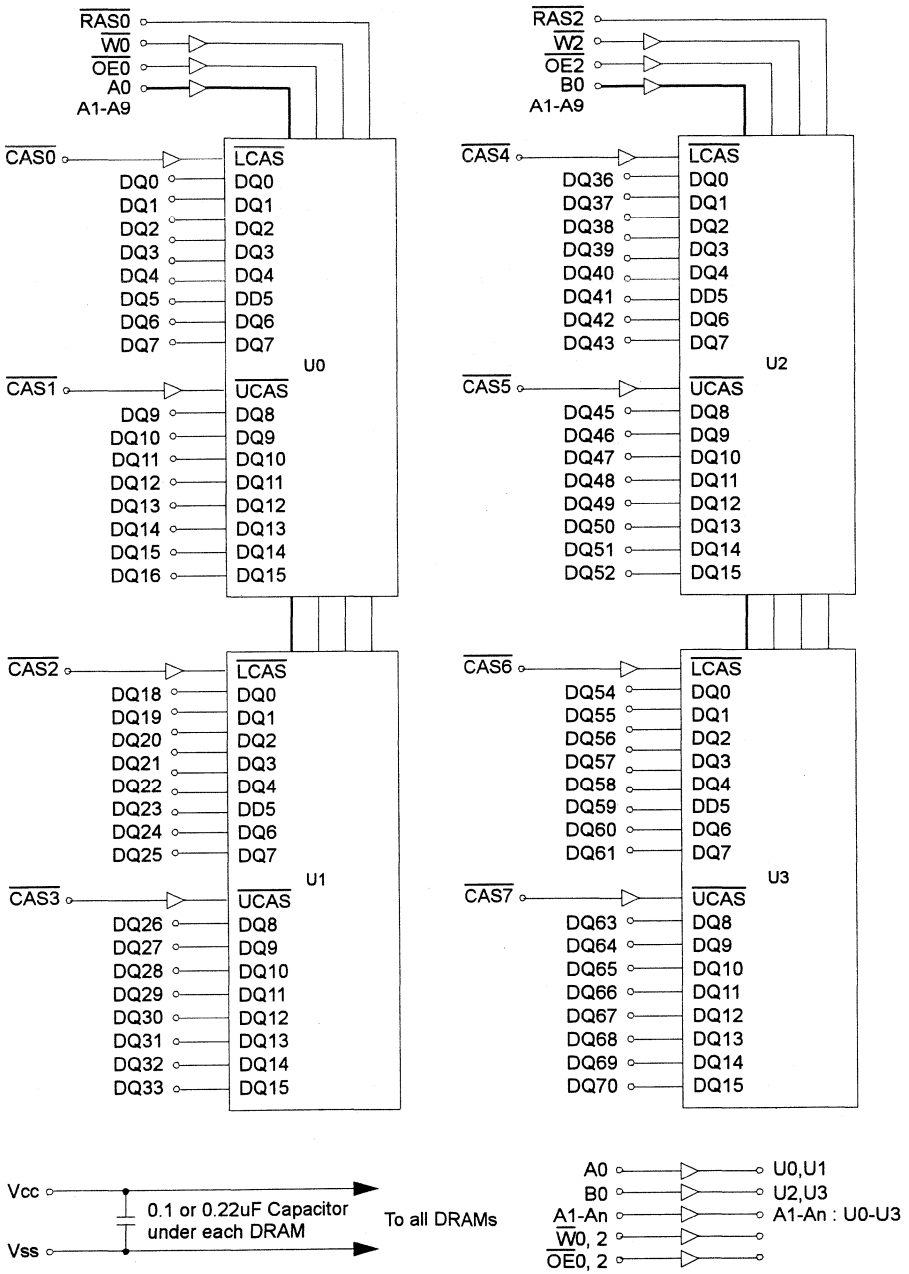
PD & ID Table

Pin	50NS	60NS
PD1	0	0
PD2	0	0
PD3	1	1
PD4	0	0
PD5	1	1
PD6	0	1
PD7	0	1
PD8	1	1
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	4	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V/20ns, Pulse width is measured at Vcc.
*2 : -2.0V/20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM364E124CJ		Unit
		Min	Max	
I_{CC1}	-5	-	560	mA
	-6	-	520	mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-5	-	560	mA
	-6	-	520	mA
I_{CC4}	-5	-	400	mA
	-6	-	360	mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-5	-	560	mA
	-6	-	520	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: EDO Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{I(L)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page mode cycle, t_{HPC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A9, B0]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	25	pF
Input capacitance[$\overline{CAS0}$ ~ $\overline{CAS7}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ1}	-	20	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	130		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		20		22	ns	3,4,5,14
Access time from column address	t_{AA}		30		35	ns	3,10,14
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,14
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,14
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	20	ns	6,11,12,14
Transition time(rise and fall)	t_T	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		22		ns	14
$\overline{CAS}$ hold time	t_{CSH}	38		48		ns	14
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	13
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	30	18	38	ns	4,14
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,14
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	14
Row address set-up time	t_{ASR}	5		5		ns	14
Row address hold time	t_{RAH}	8		8		ns	14
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	14
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,14
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	18		20		ns	14
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,14
Data hold time	t_{DH}	13		15		ns	9,14
Refresh period(1K Ref.)	t_{REF}		16		16	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	38		42		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	71		83		ns	7,14

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	
$\overline{CAS}$ set-up time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	14
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	14
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	14
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,14
Hyper page cycle time	t_{HPC}	20		25		ns	13
Hyper page read-modify-write cycle time	t_{HPRWC}	68		77		ns	13
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	14
$\overline{OE}$ access time	t_{OEA}		18		20	ns	14
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	14
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	6,11,14
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	14
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	14
Output data hold time	t_{DOH}	10		10		ns	14
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	6,11,12
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	3	18	3	20	ns	6,11,14
$\overline{W}$ to data delay	t_{WED}	20		20		ns	14
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width(Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2TTL loads and 100pF. Voh=2.0V and Vol=0.8V.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

   If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data output will contain data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out(at access time) is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. t_{CEZ}(max), t_{REZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ high going.

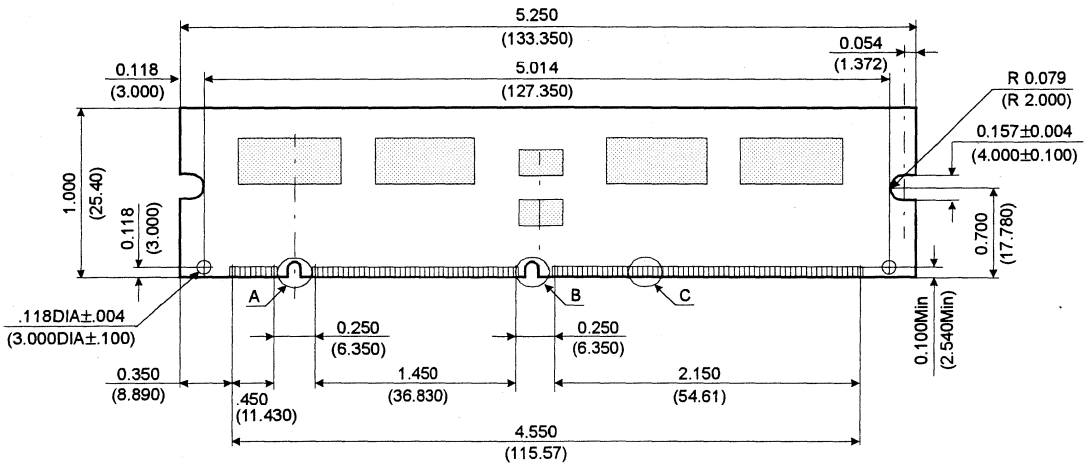
13. $t_{ASC} \geq t_{CP}$ min

14. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

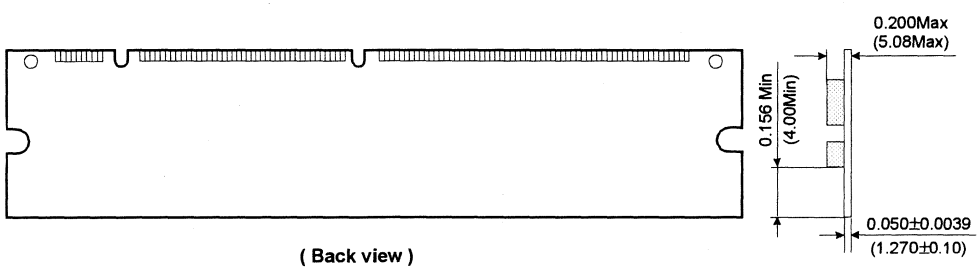
4

PACKAGE DIMENSIONS

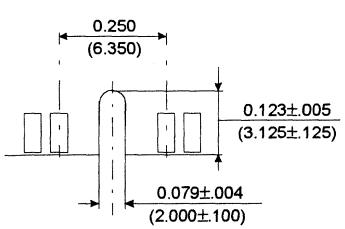
Units : Inches (millimeters)



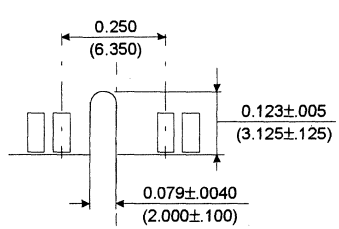
(Front view)



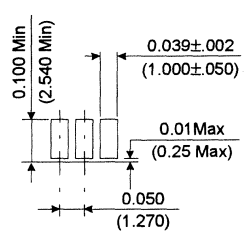
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 1Mx16 DRAM with EDO mode, SOJ.
DRAM Part No. : KMM364E124CJ - KM416C1204CJ.

KMM372C124BT Fast Page Mode

1M x 72 DRAM DIMM with ECC using 1Mx16 & 1Mx4, 1K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM372C124CT is a 1Mx72bits Dynamic RAM high density memory module. The Samsung KMM372C124CT consists of four CMOS 1Mx16bits DRAMs in TSOP-II 400mil package, two CMOS 1Mx4bit DRAMs in TSOP-II 300mil package and two 16bits driver IC in 48pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372C124CT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	20ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

FEATURES

- Part Identification
  - KMM372C124CT (1024 cycles/16ms Ref., TSOP-II)
- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{RSVD}$	57	DQ22	85	Vss	113	$\overline{RSVD}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	*A10	66	DQ26	94	DQ43	122	*A11	150	DQ62
11	DQ8	39	*A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	*$\overline{CAS5}$	158	DQ68
19	DQ14	47	$\overline{RSVD}$	75	DQ33	103	DQ50	131	$\overline{RSVD}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	*$\overline{CAS1}$	140	DQ57	168	Vcc

PD Note : PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A9	Address Input
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

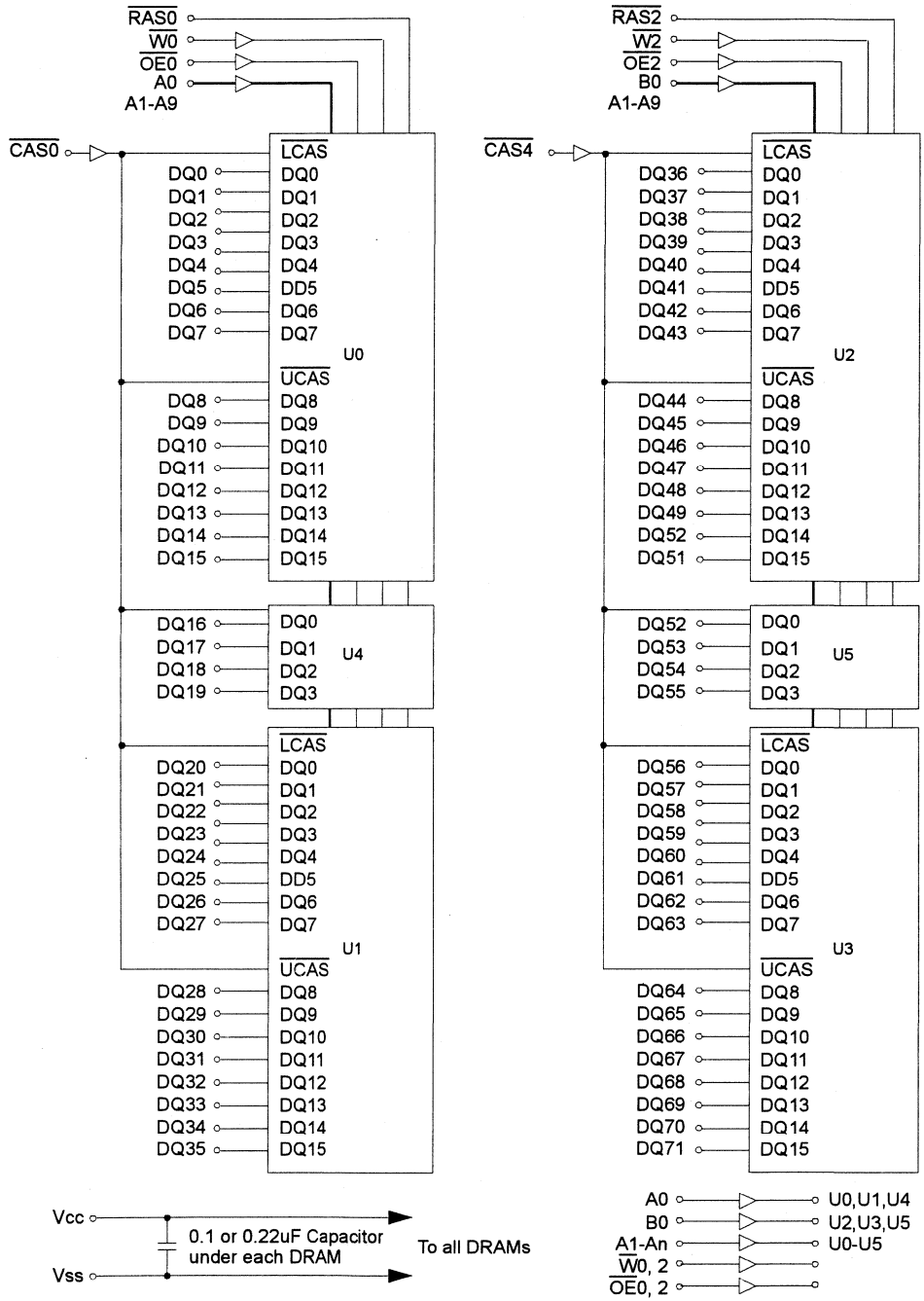
PD & ID Table

Pin	50NS	60NS
PD1	0	0
PD2	0	0
PD3	1	1
PD4	0	0
PD5	0	0
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	¡É
Power Dissipation	P_D	5.2	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V/20ns, Pulse width is measured at Vcc.
*2 : -2.0V/20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372C124CT		Unit
		Min	Max	
I_{CC1}	-5	-	730	mA
	-6	-	670	mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-5	-	730	mA
	-6	-	670	mA
I_{CC4}	-5	-	490	mA
	-6	-	430	mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-5	-	730	mA
	-6	-	670	mA
$I_{I(L)}$	Don't care	-15	15	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)
I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})
I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)
I_{CC4}*: Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)
I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)
I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)
$I_{I(L)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)
$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)
V_{OH} : Output High Voltage Level (I_{OH} = -5mA)
V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one page mode cycle,t_{PC}.

CAPACITANCE (T_A = 25°C, Vcc=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A9, B0]	C_{IN1}	-	15	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	17	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	31	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS4}$]	C_{IN4}	-	17	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ1}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, Vcc=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		20		20	ns	3,4,5,11
Access time from column address	t_{AA}		30		35	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,11
Output buffer turn-off delay	t_{OFF}	5	18	5	20	ns	6,11
Transition time(rise and fall)	t_T	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	11
$\overline{CAS}$ hold time	t_{CSH}	48		58		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	11
Row address set-up time	t_{ASR}	5		5		ns	11
Row address hold time	t_{RAH}	8		8		ns	11
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	11
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,11
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,11
Data hold time	t_{DH}	20		20		ns	9,11
Refresh period	t_{REF}		16		16	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	71		83		ns	7,11
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	11
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	11
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	3		3		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3,11
Fast page mode cycle time	t_{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	76		80		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	t_{RASP}	50	100K	60	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	8		8		ns	11
$\overline{OE}$ access time	t_{OEA}		18		20	ns	
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	11
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	11
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS} is not restrictive operating parameter. It included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

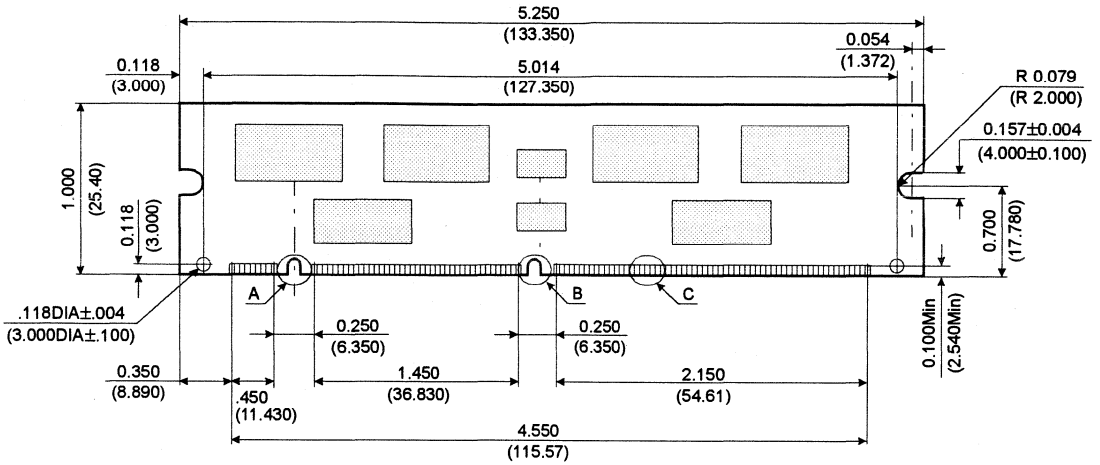
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

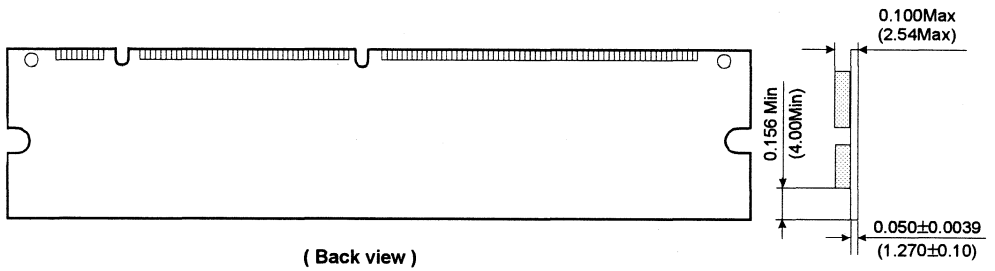
11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

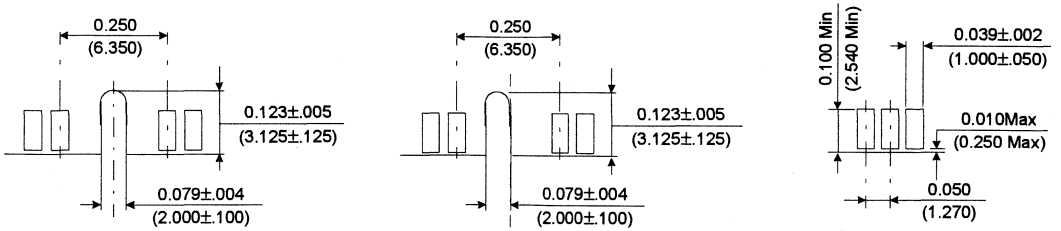
Units : Inches (millimeters)



(Front view)



(Back view)



Tolerances : ±.005(.13) unless otherwise specified

The used device is 1Mx16 DRAM with FP mode, TSOP and 1Mx4 DRAM with FP mode,TSOP.
DRAM Part No. : KMM372C124CT - KM416C1200CT and KM44C1000DT

KMM372E124CT EDO Mode

1M x 72 DRAM DIMM with ECC using 1Mx16 & 1Mx4, 1K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM372E124CT is a 1Mx72bits Dynamic RAM high density memory module. The Samsung KMM372E124CT consists of four CMOS 1Mx16bits DRAMs in TSOP-II 400mil package, two CMOS 1Mx4bit DRAMs in TSOP-II 300mil package and two 16bits driver IC in 48pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372E124CT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	20ns	84ns	20ns
-6	60ns	22ns	104ns	25ns

FEATURES

- Part Identification
  - KMM372E124CT (1024 cycles/16ms Ref., TSOP-II)
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{RSVD}$	57	DQ22	85	Vss	113	$\overline{RSVD}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	*A10	66	DQ26	94	DQ43	122	*A11	150	DQ62
11	DQ8	39	*A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	$\overline{RFU}$	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	*$\overline{CAS5}$	158	DQ68
19	DQ14	47	$\overline{RSVD}$	75	DQ33	103	DQ50	131	$\overline{RSVD}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	$\overline{RFU}$	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	*$\overline{CAS1}$	140	DQ57	168	Vcc

PD Note : PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A9	Address Input
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

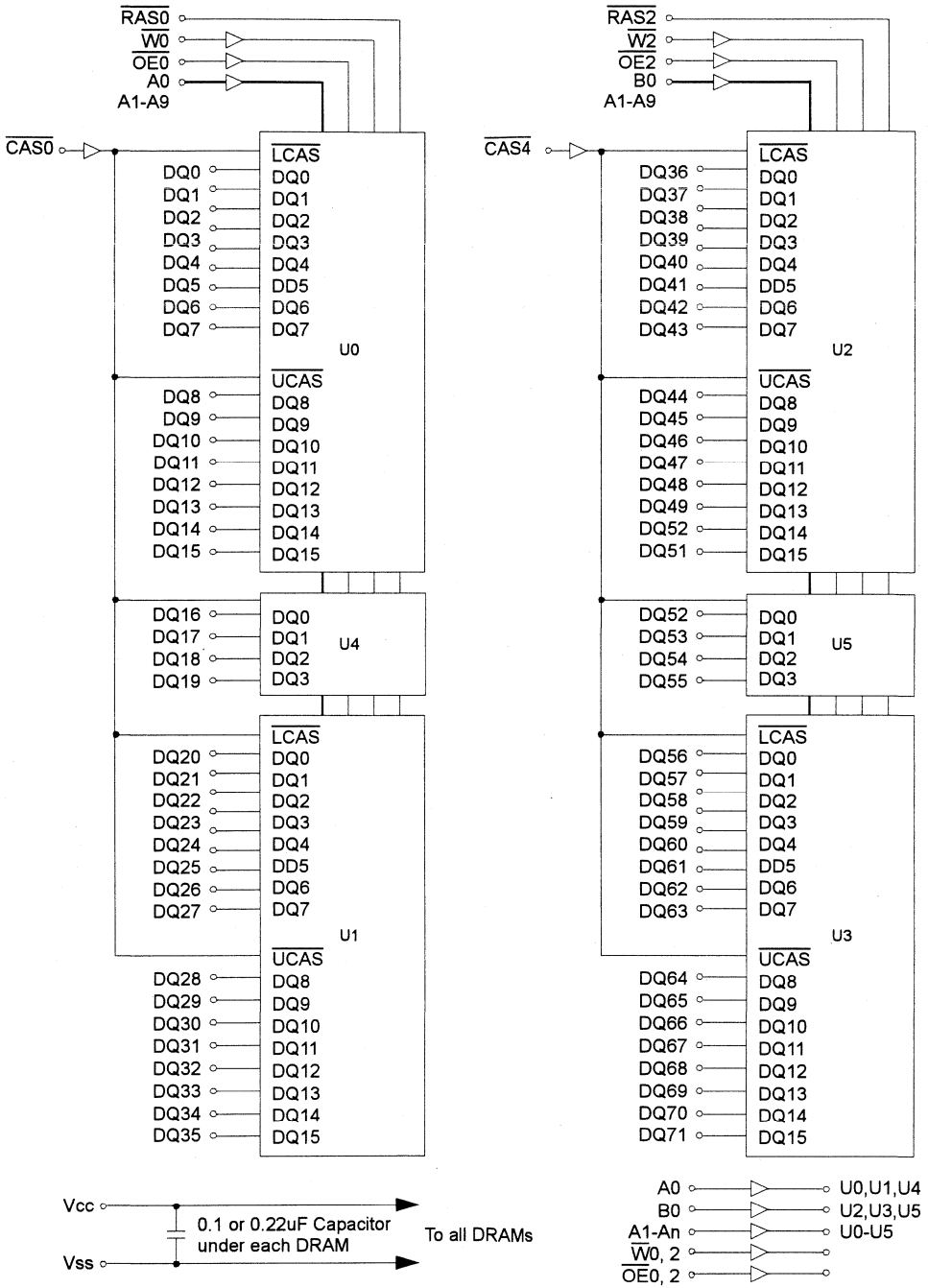
PD & ID Table

Pin	50NS	60NS
PD1	0	0
PD2	0	0
PD3	1	1
PD4	0	0
PD5	1	1
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	5.2	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V/20ns, Pulse width is measured at Vcc.
*2 : -2.0V/20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372E124CT		Unit
		Min	Max	
I_{CC1}	-5	-	730	mA
	-6	-	670	mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-5	-	730	mA
	-6	-	670	mA
I_{CC4}	-5	-	570	mA
	-6	-	510	mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-5	-	730	mA
	-6	-	670	mA
$I_{I(L)}$	Don't care	-15	15	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)
I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})
I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)
I_{CC4}*: EDO Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)
I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)
I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)
$I_{I(L)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)
$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)
V_{OH} : Output High Voltage Level (I_{OH} = -5mA)
V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page mode cycle,t_{HPC}

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A9, B0]	C_{IN1}	-	15	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	17	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	31	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS4}$]	C_{IN4}	-	17	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ1}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	130		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		20		22	ns	3,4,5,14
Access time from column address	t_{AA}		30		35	ns	3,10,14
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,14
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,14
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	20	ns	6,11,12,14
Transition time(rise and fall)	t_T	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		22		ns	14
$\overline{CAS}$ hold time	t_{CSH}	38		48		ns	14
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	13
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	30	18	38	ns	4,14
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,14
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	14
Row address set-up time	t_{ASR}	5		5		ns	14
Row address hold time	t_{RAH}	8		8		ns	14
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	14
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,14
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	18		20		ns	14
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,14
Data hold time	t_{DH}	13		15		ns	9,14
Refresh period(1K Ref.)	t_{REF}		16		16	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	38		42		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	71		83		ns	7,14

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	
$\overline{CAS}$ set-up time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	14
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	14
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	14
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,14
Hyper page cycle time	t_{HPC}	20		25		ns	13
Hyper page read-modify-write cycle time	t_{HPRWC}	68		77		ns	13
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	14
$\overline{OE}$ access time	t_{OEA}		18		20	ns	14
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	14
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	6,11,14
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	14
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	14
Output data hold time	t_{DOH}	10		10		ns	14
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	6,11,12
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	3	18	3	20	ns	6,11,14
$\overline{W}$ to data delay	t_{WED}	20		20		ns	14
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width(Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF. Voh=2.0V and Vol=0.8V.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

   If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data output will contain data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out(at access time) is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. t_{CEZ}(max), t_{REZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

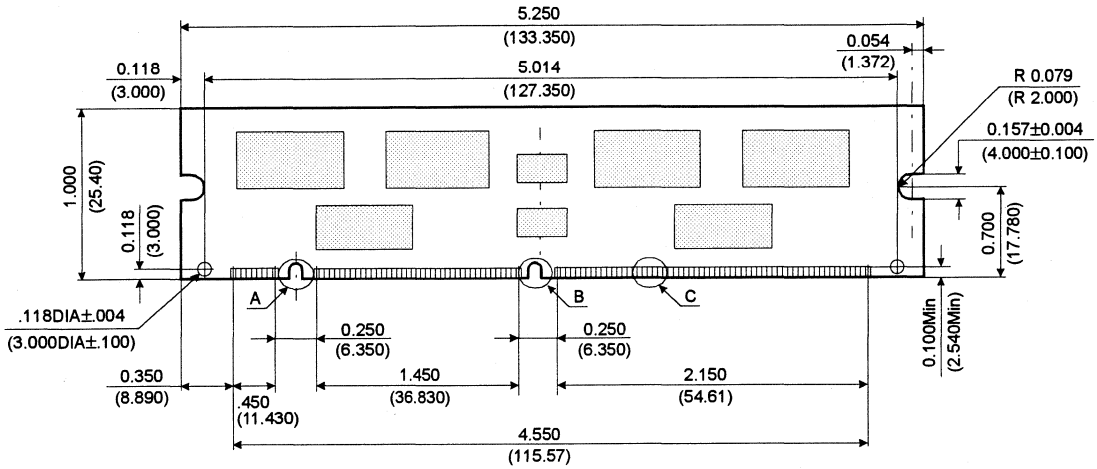
12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ high going.

13. $t_{ASC} \geq t_{CP}$ min

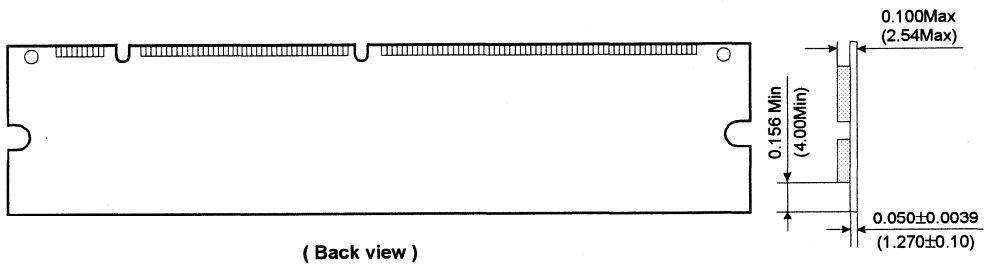
14. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

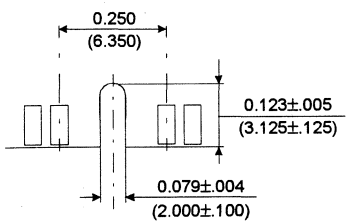
Units : Inches (millimeters)



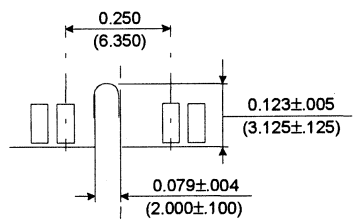
(Front view)



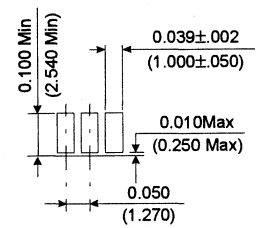
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 1Mx16 DRAM with EDO mode, TSOP and 1Mx4 DRAM with EDO mode,TSOP.
DRAM Part No. : KMM372E124CT - KM416C1204CT and KM44C1004DT

KMM364C224CJ Fast Page Mode
2M x 64 DRAM DIMM using 1Mx16, 1K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM364C224CJ is a 2Mx64bits Dynamic RAM high density memory module. The Samsung KMM364C224CJ consists of eight CMOS 1Mx16bits DRAMs in 42-pin SOJ 400mil package, and two 16bits driver IC in 48pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM364C224CJ is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	20ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

FEATURES

- Part Identification
  - KMM364C224CJ (1024 cycles/16ms Ref., SOJ)
- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS2}$	57	DQ22	85	Vss	113	$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	*A10	66	*DQ26	94	DQ43	122	*A11	150	*DQ62
11	*DQ8	39	*A12	67	DQ27	95	*DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	$\overline{CAS6}$	75	DQ33	103	DQ50	131	$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	*DQ35	105	DQ52	133	Vcc	161	*DQ71
22	*DQ17	50	RSVD	78	Vss	106	*DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

PD Note : PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A9	Address Input
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$ ~ $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ ~ $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

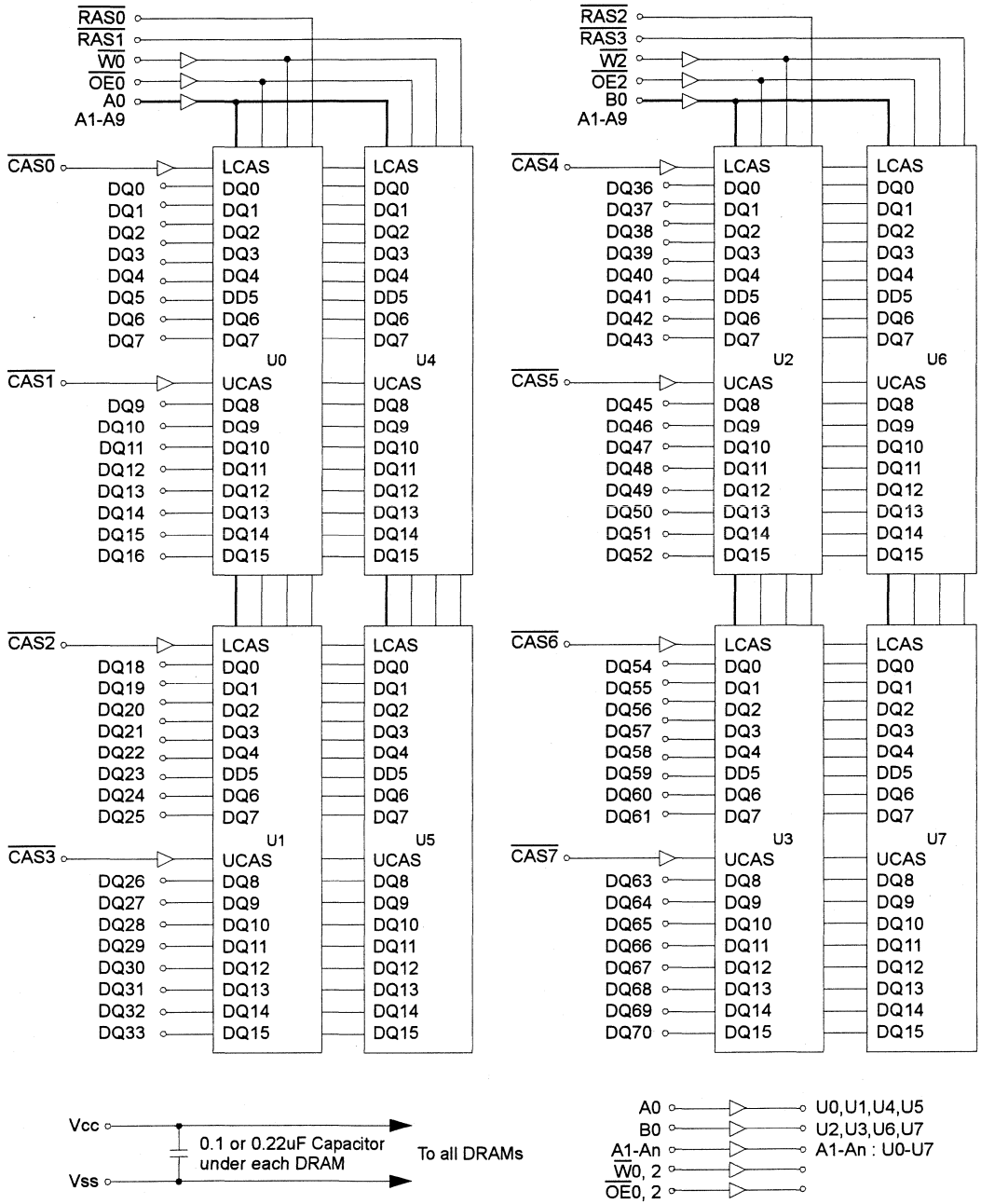
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	1	1
PD4	0	0
PD5	0	0
PD6	0	1
PD7	0	1
PD8	1	1
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V/20ns, Pulse width is measured at Vcc.
*2 : -2.0V/20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM364C224CJ		Unit
		Min	Max	
I_{CC1}	-5 -6	- -	660 620	mA mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-5 -6	- -	660 620	mA mA
I_{CC4}	-5 -6	- -	460 420	mA mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-5 -6	- -	660 620	mA mA
$I_{I(L)}$ $I_{O(L)}$	Don't care	-10 -10	10 10	uA uA
V_{OH} V_{OL}	Don't care	2.4 -	- 0.4	V V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)
I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})
I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)
I_{CC4}*: Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)
I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)
I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)
$I_{I(L)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)
$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)
V_{OH} : Output High Voltage Level (I_{OH} = -5mA)
V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one page mode cycle, t_{PC}.

CAPACITANCE (T_A = 25°C, Vcc=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A9, B0]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$ ~ $\overline{RAS3}$]	C_{IN3}	-	25	pF
Input capacitance[$\overline{CAS0}$ ~ $\overline{CAS7}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ1}	-	25	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		20		20	ns	3,4,5,11
Access time from column address	t_{AA}		30		35	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,11
Output buffer turn-off delay	t_{OFF}	5	18	5	20	ns	6,11
Transition time(rise and fall)	t_T	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	11
$\overline{CAS}$ hold time	t_{CSH}	48		58		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	11
Row address set-up time	t_{ASR}	5		5		ns	11
Row address hold time	t_{RAH}	8		8		ns	11
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	11
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,11
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,11
Data hold time	t_{DH}	20		20		ns	9,11
Refresh period	t_{REF}		16		16	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	71		83		ns	7,11
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	11
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	11
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	3		3		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3,11
Fast page mode cycle time	t_{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	76		80		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	t_{RASP}	50	100K	60	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	8		8		ns	11
$\overline{OE}$ access time	t_{OEA}		18		20	ns	
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	11
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	11
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. twcs is not restrictive operating parameter. It included in the data sheet as electrical characteristic only. If twcs≥twcs(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

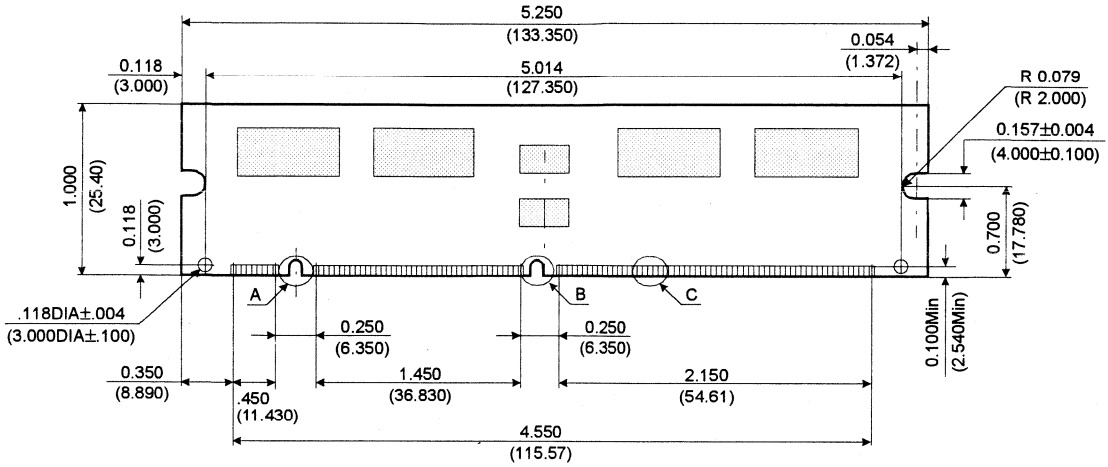
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

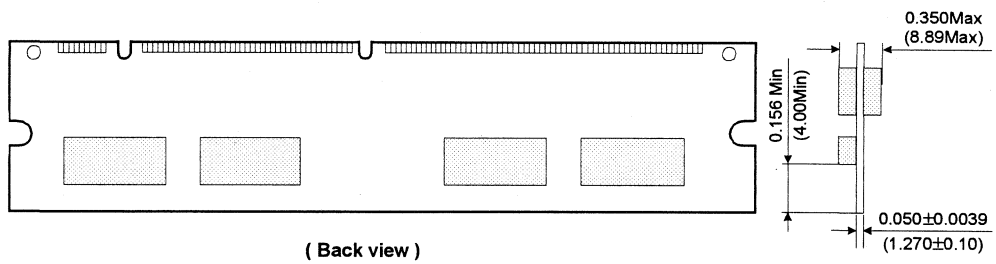
11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

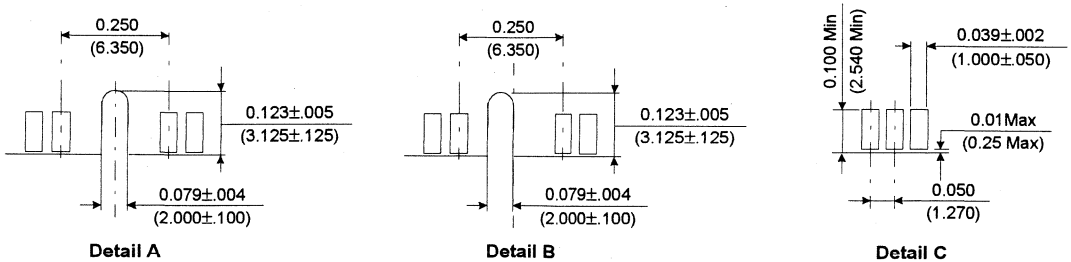
Units : Inches (millimeters)



(Front view)



(Back view)



Tolerances : ±.005(.13) unless otherwise specified

The used device is 1Mx16 DRAM with FP mode, SOJ.
DRAM Part No. : KMM364C224CJ - KM416C1200CJ.

KMM364E224CJ EDO Mode

2M x 64 DRAM DIMM using 1Mx16, 1K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM364E224CJ is a 2Mx64bits Dynamic RAM high density memory module. The Samsung KMM364E224CJ consists of eight CMOS 1Mx16bits DRAMs in 42-pin SOJ 400mil package, and two 16bits driver IC in 48pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM364E224CJ is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	20ns	84ns	20ns
-6	60ns	22ns	104ns	25ns

FEATURES

- Part Identification
  - KMM364E224CJ (1024 cycles/16ms Ref., SOJ)
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS2}$	57	DQ22	85	Vss	113	$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	*A10	66	*DQ26	94	DQ43	122	*A11	150	*DQ62
11	*DQ8	39	*A12	67	DQ27	95	*DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	$\overline{CAS6}$	75	DQ33	103	DQ50	131	$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	*DQ35	105	DQ52	133	Vcc	161	*DQ71
22	*DQ17	50	RSVD	78	Vss	106	*DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

PD Note : PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A9	Address Input
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$ ~ $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ ~ $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

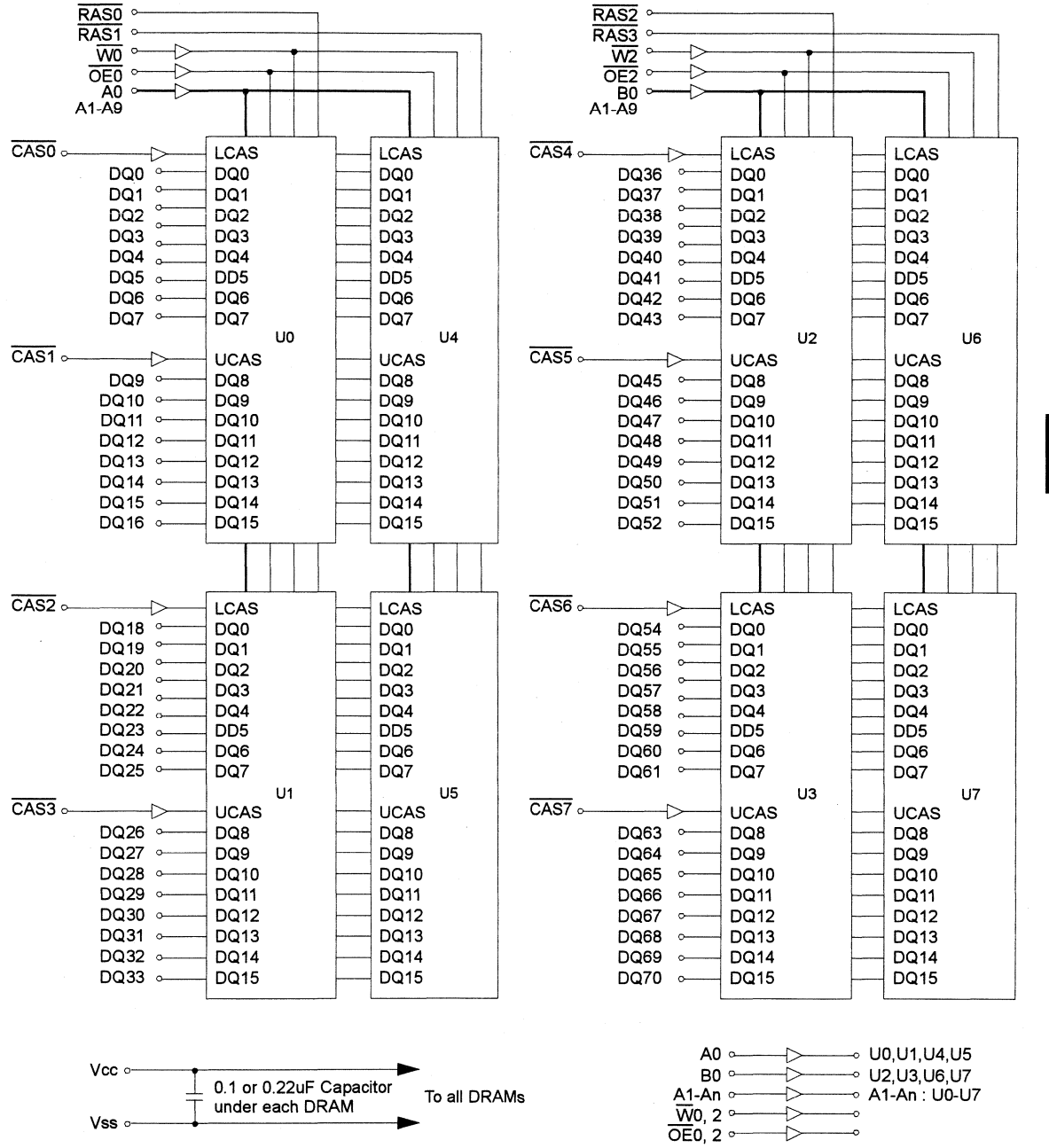
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	1	1
PD4	0	0
PD5	1	1
PD6	0	1
PD7	0	1
PD8	1	1
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



4

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V/20ns, Pulse width is measured at Vcc.
*2 : -2.0V/20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM364E224CJ		Unit
		Min	Max	
I_{CC1}	-5	-	660	mA
	-6	-	620	mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-5	-	660	mA
	-6	-	620	mA
I_{CC4}	-5	-	500	mA
	-6	-	460	mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-5	-	660	mA
	-6	-	600	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-10	10	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1}* : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}* : EDO Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{I(L)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page mode cycle,t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A9, B0]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$ ~ $\overline{RAS3}$]	C_{IN3}	-	25	pF
Input capacitance[$\overline{CAS0}$ ~ $\overline{CAS7}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ1}	-	25	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	130		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		20		22	ns	3,4,5,14
Access time from column address	t_{AA}		30		35	ns	3,10,14
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,14
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,14
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	20	ns	6,11,12,14
Transition time(rise and fall)	t_T	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		22		ns	14
$\overline{CAS}$ hold time	t_{CSH}	38		48		ns	14
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	13
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	30	18	38	ns	4,14
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,14
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	14
Row address set-up time	t_{ASR}	5		5		ns	14
Row address hold time	t_{RAH}	8		8		ns	14
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	14
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,14
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	18		20		ns	14
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,14
Data hold time	t_{DH}	13		15		ns	9,14
Refresh period(1K Ref.)	t_{REF}		16		16	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	38		42		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	71		83		ns	7,14

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	
$\overline{CAS}$ set-up time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	14
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	14
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	14
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,14
Hyper page cycle time	t_{HPC}	20		25		ns	13
Hyper page read-modify-write cycle time	t_{HPRWC}	68		77		ns	13
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	14
$\overline{OE}$ access time	t_{OEA}		18		20	ns	14
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	14
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	6,11,14
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	14
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	14
Output data hold time	t_{DOH}	10		10		ns	14
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	6,11,12
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	3	18	3	20	ns	6,11,14
$\overline{W}$ to data delay	t_{WED}	20		20		ns	14
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width(Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF. Voh=2.0V and Vol=0.8V.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

   If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data output will contain data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out(at access time) is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. t_{CEZ}(max), t_{REZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ high going.

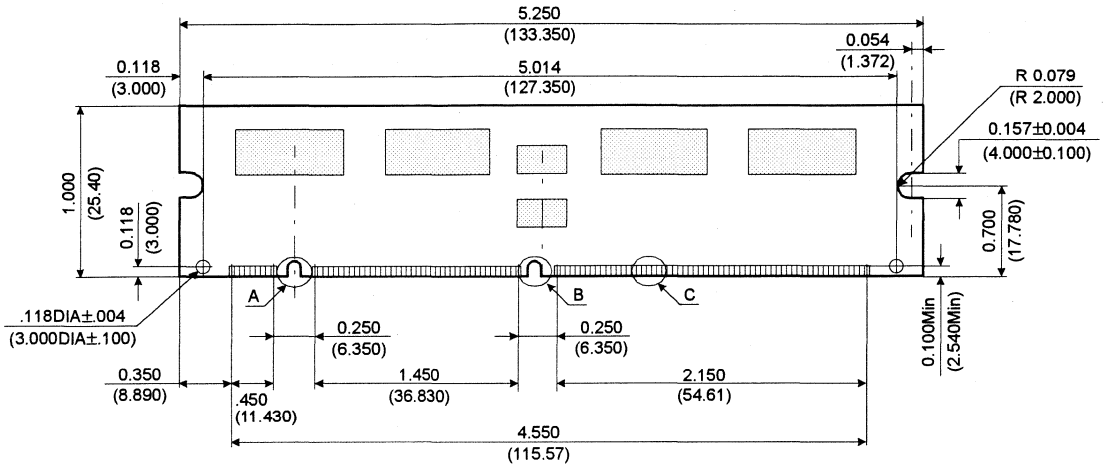
13. $t_{ASC} \geq t_{CP}$ min

14. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

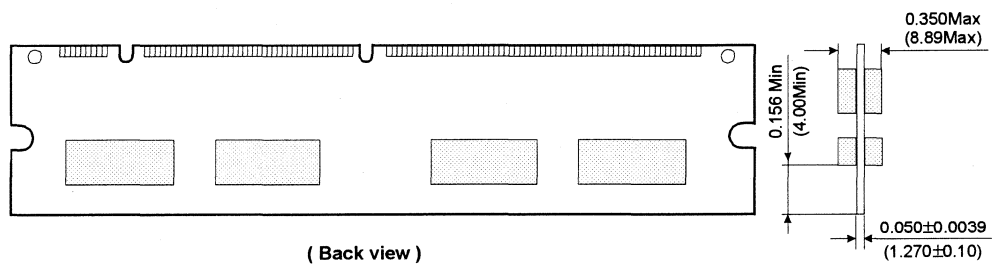
4

PACKAGE DIMENSIONS

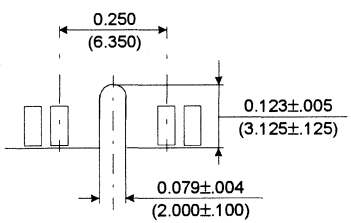
Units : Inches (millimeters)



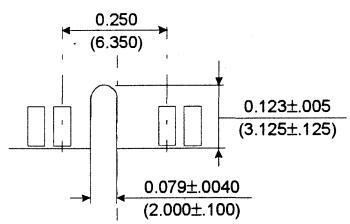
(Front view)



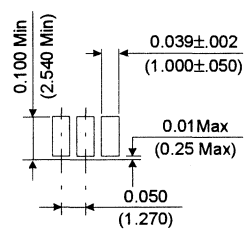
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 1Mx16 DRAM with EDO mode, SOJ.
DRAM Part No. : KMM364E224CJ - KM416C1204CJ.

KMM364C213CK/CS Fast Page Mode

2M x 64 DRAM DIMM using 2Mx8, 2K Refresh , 5V

GENERAL DESCRIPTION

The Samsung KMM364C213C is a 2Mx64bits Dynamic RAM high density memory module. The Samsung KMM364C213C consists of eight CMOS 2Mx8bits DRAMs in SOJ/TSOP-II 300mil package, and two 16bits driver IC in 48pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM364C213C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	18ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

FEATURES

- Part Identification
  - KMM364C213CK (2048 cycles/32ms Ref. 300mil SOJ)
  - KMM364C213CS (2048 cycles/32ms Ref. 300mil TSOP)
- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS2}$	57	DQ22	85	Vss	113	$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	*DQ26	94	DQ43	122	*A11	150	*DQ62
11	*DQ8	39	*A12	67	DQ27	95	*DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	$\overline{CAS6}$	75	DQ33	103	DQ50	131	$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	*DQ35	105	DQ52	133	Vcc	161	*DQ71
22	*DQ17	50	RSVD	78	Vss	106	*DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	$\overline{RFU}$	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

PD Note : PD & ID Terminals must each be pulled up through a resister to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A10	Address Input (2K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ ~ $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

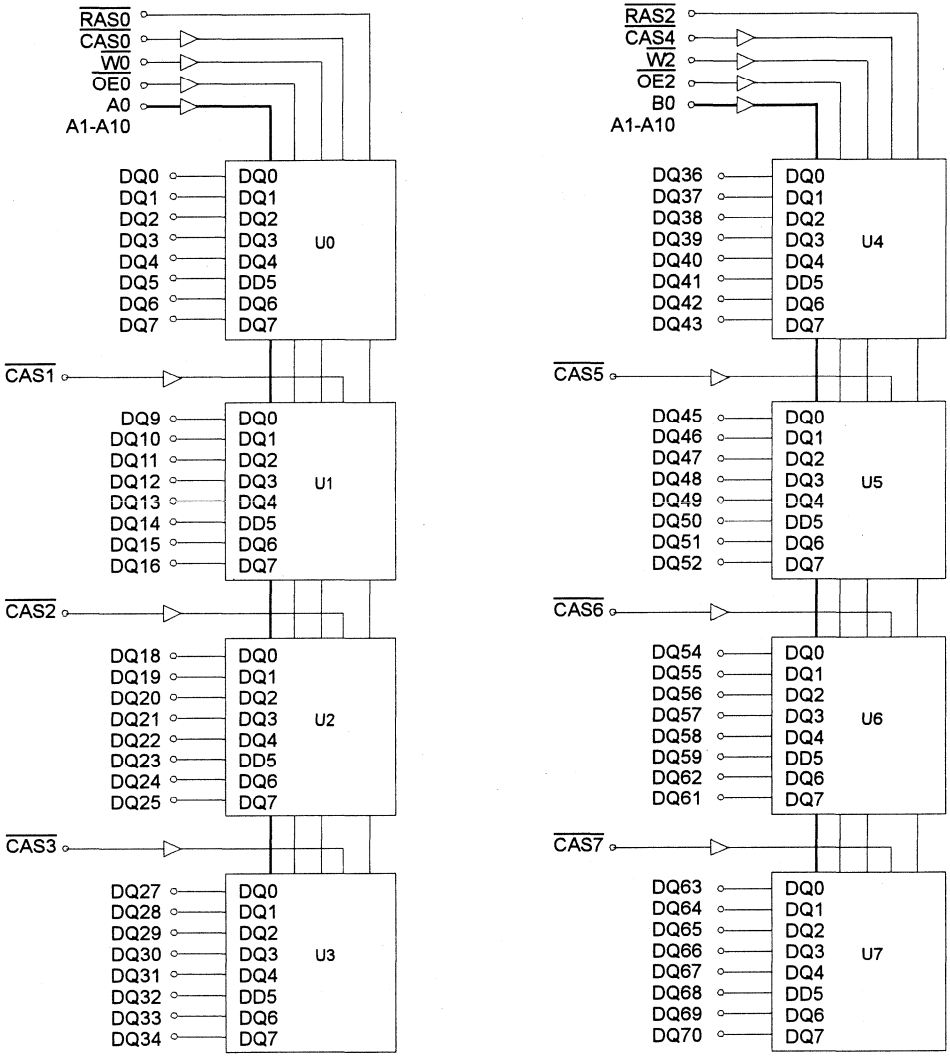
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	0	0
PD4	1	1
PD5	0	0
PD6	0	1
PD7	0	1
PD8	1	1
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V/20ns, Pulse width is measured at Vcc.
*2 : -2.0V/20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM364C213CK/CS		Unit
		Min	Max	
I_{CC1}	-5 -6	- -	880 800	mA mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-5 -6	- -	880 800	mA mA
I_{CC4}	-5 -6	- -	720 640	mA mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-5 -6	- -	880 800	mA mA
$I_{I(L)}$ $I_{O(L)}$	Don't care	-40 -5	40 5	uA uA
V_{OH} V_{OL}	Don't care	2.4 -	- 0.4	V V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)
I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})
I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)
I_{CC4}*: Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)
I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)
I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)
$I_{I(L)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)
$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)
V_{OH} : Output High Voltage Level (I_{OH} = -5mA)
V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one page mode cycle, t_{PC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A10, B0]	C_{IN1}	-	15	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	17	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	38	pF
Input capacitance[$\overline{CAS0}$ ~ $\overline{CAS7}$]	C_{IN4}	-	17	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ1}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,11
Access time from column address	t_{AA}		30		35	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,11
Output buffer turn-off delay	t_{OFF}	5	18	5	20	ns	6,11
Transition time(rise and fall)	t_T	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	11
$\overline{CAS}$ hold time	t_{CSH}	48		58		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	11
Row address set-up time	t_{ASR}	5		5		ns	11
Row address hold time	t_{RAH}	8		8		ns	11
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	11
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,11
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	18		20		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,11
Data hold time	t_{DH}	15		20		ns	9,11
Refresh period (2K refresh)	t_{REF}		32		32	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7

AC CHARACTERISTICS (0°C≤TA≤70°C, Vcc=5.0V±10%. See notes 1,2.)

Test condition : Vih/Vil=2.4/0.8V, Voh/Vol=2.4/0.4V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	71		83		ns	7,11
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	11
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	11
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	3		3		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3,11
Fast page mode cycle time	t_{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	75		80		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	8		8		ns	11
$\overline{OE}$ access time	t_{OEA}		18		20	ns	11
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5		5	20	ns	11
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS} is not restrictive operating parameter. It included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

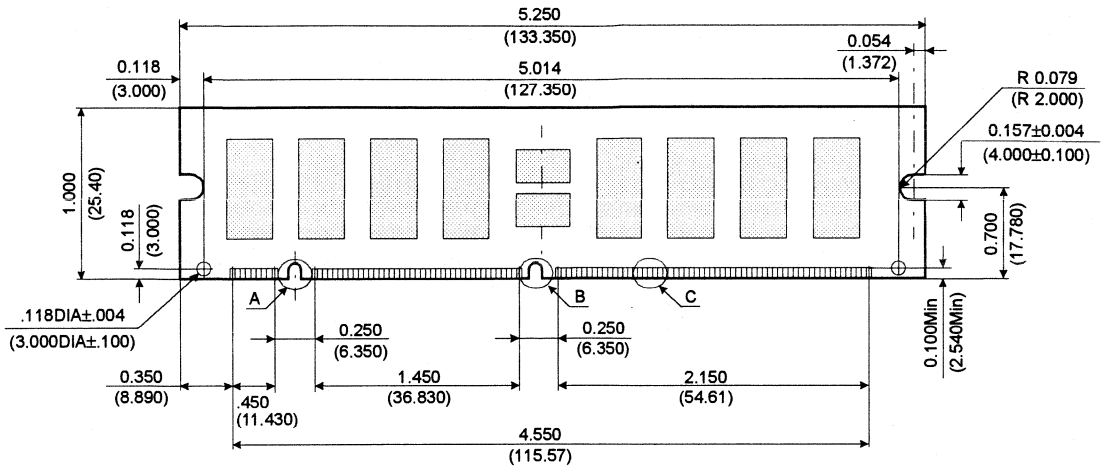
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

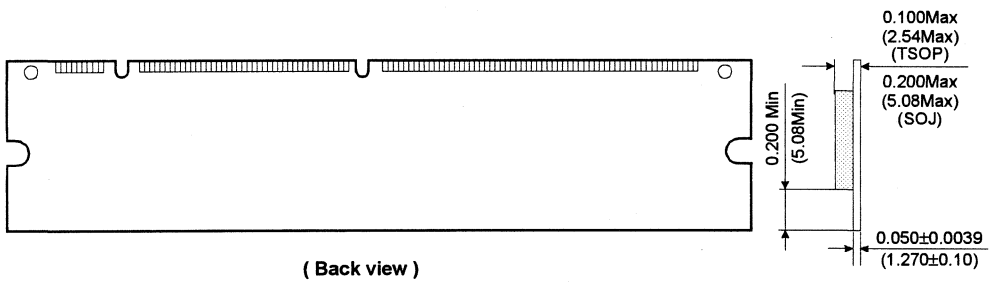
11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

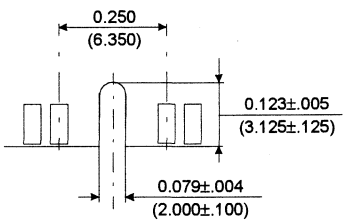
Units : Inches (millimeters)



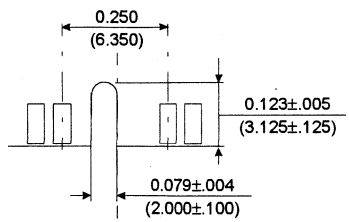
(Front view)



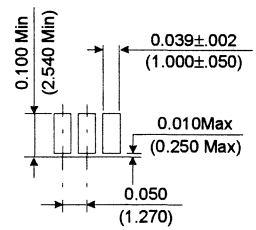
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 2Mx8 DRAM with Fast Page mode, SOJ or TSOP II (Forward).

DRAM Part No. : KMM364C213CK - KM48C2100CK
KMM364C213CS - KM48C2100CS

KMM364E213CK/CS EDO Mode

2M x 64 DRAM DIMM using 2Mx8, 2K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM364E213C is a 2Mx64bits Dynamic RAM high density memory module. The Samsung KMM364E213C consists of eight CMOS 2Mx8bits DRAMs in SOJ/TSOP-II 300mil package, and two 16bits driver IC in 48pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM364E213C is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	18ns	84ns	20ns
-6	60ns	20ns	104ns	25ns

FEATURES

- Part Identification
  - KMM364E213CK (2048 cycles/32ms Ref., SOJ)
  - KMM364E213CS (2048 cycles/32ms Ref., TSOP)
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS2}$	57	DQ22	85	Vss	113	$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	*DQ26	94	DQ43	122	*A11	150	*DQ62
11	*DQ8	39	*A12	67	DQ27	95	*DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	$\overline{CAS6}$	75	DQ33	103	DQ50	131	$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	*DQ35	105	DQ52	133	Vcc	161	*DQ71
22	*DQ17	50	RSVD	78	Vss	106	*DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

PIN NAMES

Pin Names	Function
A0, B0, A1 - A10	Address Input (2K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ ~ $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	0	0
PD4	1	1
PD5	1	1
PD6	0	1
PD7	0	1
PD8	1	1
ID0	0	0
ID1	0	0

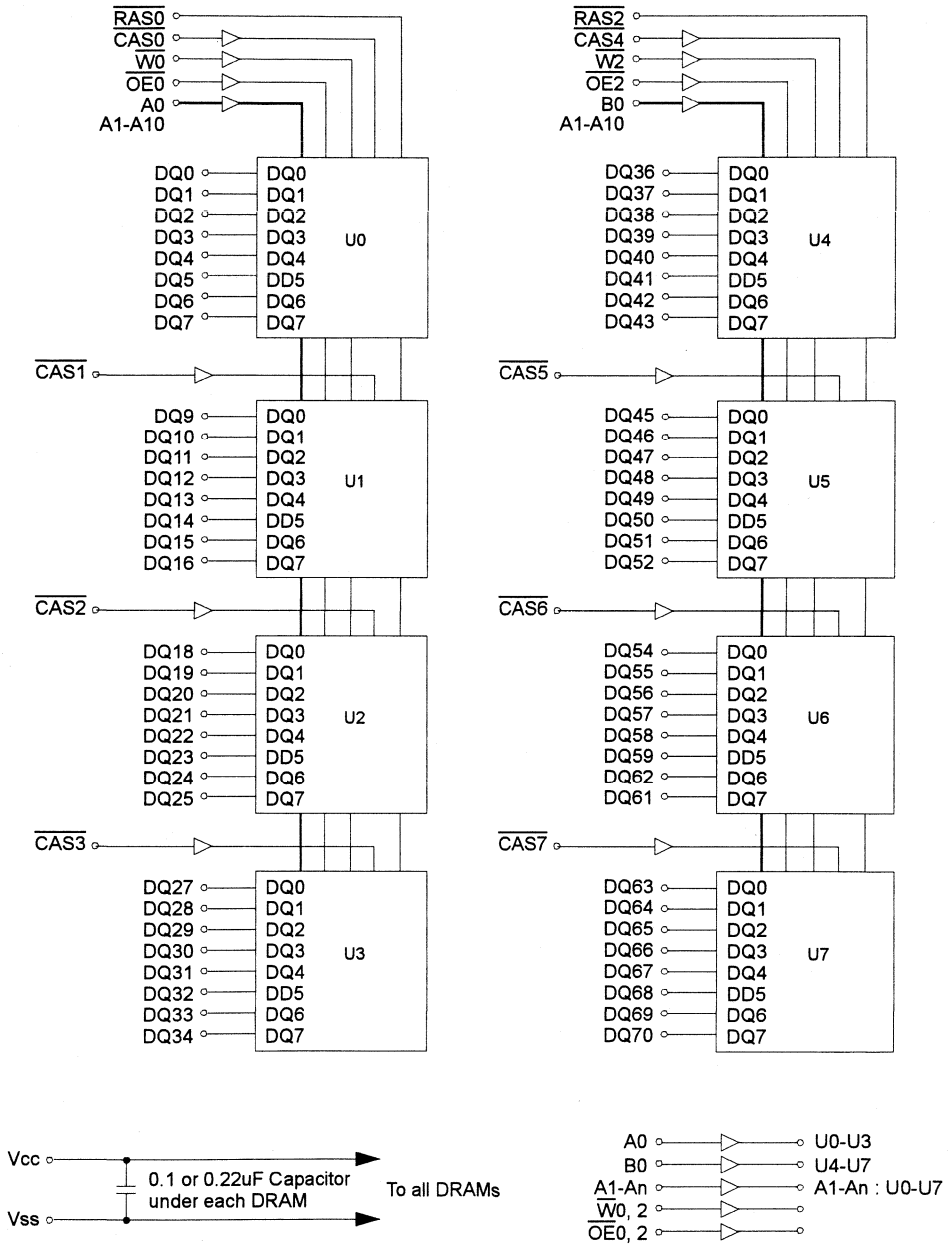
PD Note : PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V/20ns, Pulse width is measured at Vcc.
*2 : -2.0V/20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM364E213CK/CS		Unit
		Min	Max	
I_{CC1}	-5	-	880	mA
	-6	-	800	mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-5	-	880	mA
	-6	-	800	mA
I_{CC4}	-5	-	720	mA
	-6	-	640	mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-5	-	880	mA
	-6	-	800	mA
$I_{I(L)}$	Don't care	-40	40	uA
$I_{O(L)}$		-10	10	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)
I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})
I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)
I_{CC4}*: EDO Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)
I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)
I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)
$I_{I(L)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)
$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)
V_{OH} : Output High Voltage Level (I_{OH} = -5mA)
V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page mode cycle, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5.0V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A10, B0]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	40	pF
Input capacitance[$\overline{CAS0}$ ~ $\overline{CAS7}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ1}	-	20	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	131		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,14
Access time from column address	t_{AA}		30		35	ns	3,10,14
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,14
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,14
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	20	ns	6,11,12,14
Transition time(rise and fall)	t_T	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	14
$\overline{CAS}$ hold time	t_{CSH}	36		43		ns	14
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	13
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,14
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,14
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	14
Row address set-up time	t_{ASR}	5		5		ns	14
Row address hold time	t_{RAH}	8		8		ns	14
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	14
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,14
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	18		20		ns	14
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,14
Data hold time	t_{DH}	13		15		ns	9,14
Refresh period(2K Ref.)	t_{REF}		32		32	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	71		83		ns	7,14

4

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.4/0.8V$, $V_{oh}/V_{ol}=2.0/0.8V$, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	
$\overline{CAS}$ set-up time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	14
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	14
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	14
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,14
Hyper page cycle time	t_{HPC}	20		25		ns	13
Hyper page read-modify-write cycle time	t_{HPRWC}	68		77		ns	13
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	14
$\overline{OE}$ access time	t_{OEA}		18		20	ns	14
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	14
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	7,11,14
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	14
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	14
Output data hold time	t_{DOH}	10		10		ns	14
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	6,11,12
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	3	18	3	20	ns	6,11,14
$\overline{W}$ to data delay	t_{WED}	20		20		ns	14
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width(Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF. Voh=2.0V and Vol=0.8V.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

   If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data output will contain data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out(at access time) is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. t_{CEZ}(max), t_{REZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ high going.

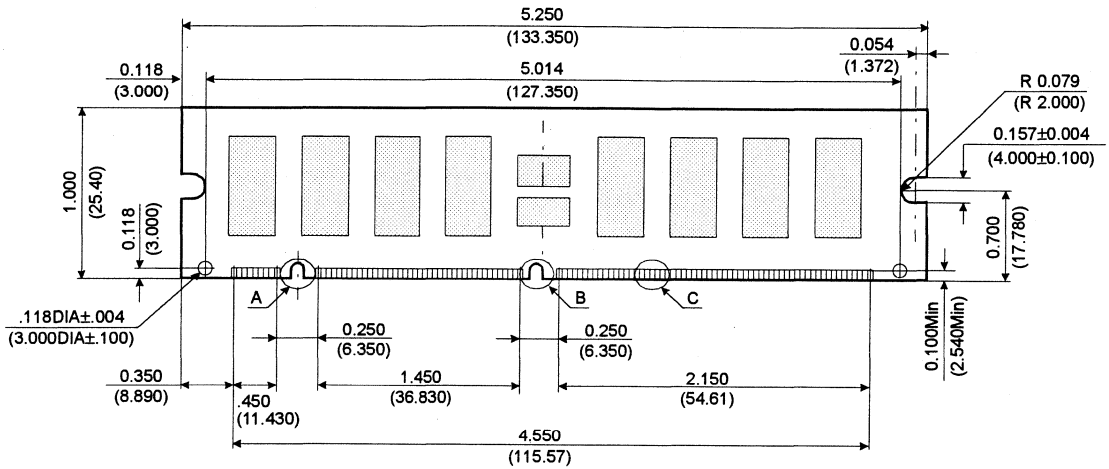
13. $t_{ASC} \geq t_{CP}$ min

14. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

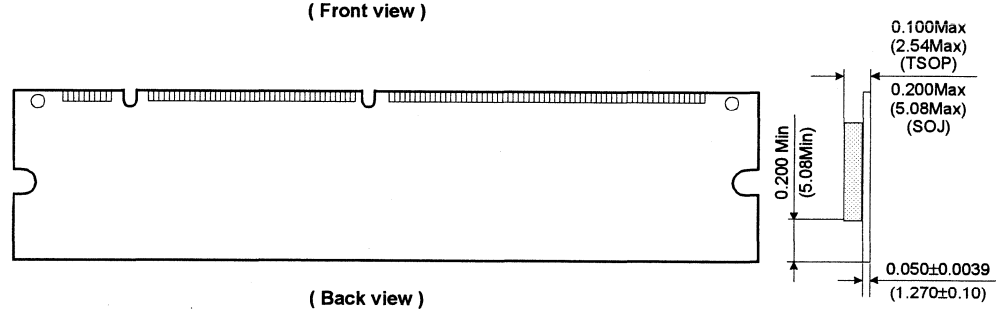
4

PACKAGE DIMENSIONS

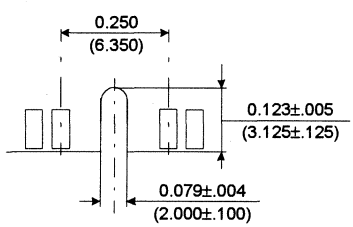
Units : Inches (millimeters)



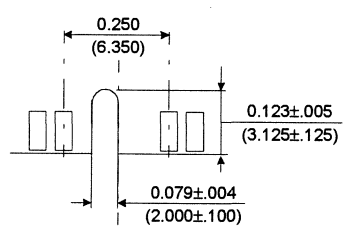
(Front view)



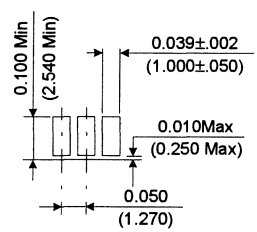
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 2Mx8 DRAM with EDO mode, SOJ or TSOP II (Forward).
DRAM Part No. : KMM364E213CK - KM48C2104CK
KMM364E213CS - KM48C2104CS

KMM372C213CK/CS Fast Page Mode

2M x 72 DRAM DIMM with ECC using 2Mx8, 2K Refresh , 5V

GENERAL DESCRIPTION

The Samsung KMM372C213C is a 2Mx72bits Dynamic RAM high density memory module. The Samsung KMM372C213C consists of nine CMOS 2Mx8bits DRAMs in SOJ/TSOP-II 300mil package, and two 16bits driver IC in 48pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372C213C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	18ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

FEATURES

- Part Identification
  - KMM372C213CK (2048 cycles/32ms Ref. 300mil SOJ)
  - KMM372C213CS (2048 cycles/32ms Ref. 300mil TSOP)
- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{RSVD}$	57	DQ22	85	Vss	113	$\overline{RSVD}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	*A11	150	DQ62
11	DQ8	39	*A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	$\overline{RFU}$	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	*$\overline{CAS5}$	158	DQ68
19	DQ14	47	$\overline{RSVD}$	75	DQ33	103	DQ50	131	$\overline{RSVD}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	$\overline{RFU}$	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	*$\overline{CAS1}$	140	DQ57	168	Vcc

PD Note : PD & ID Terminals must each be pulled up through a resister to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A10	Address Input
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

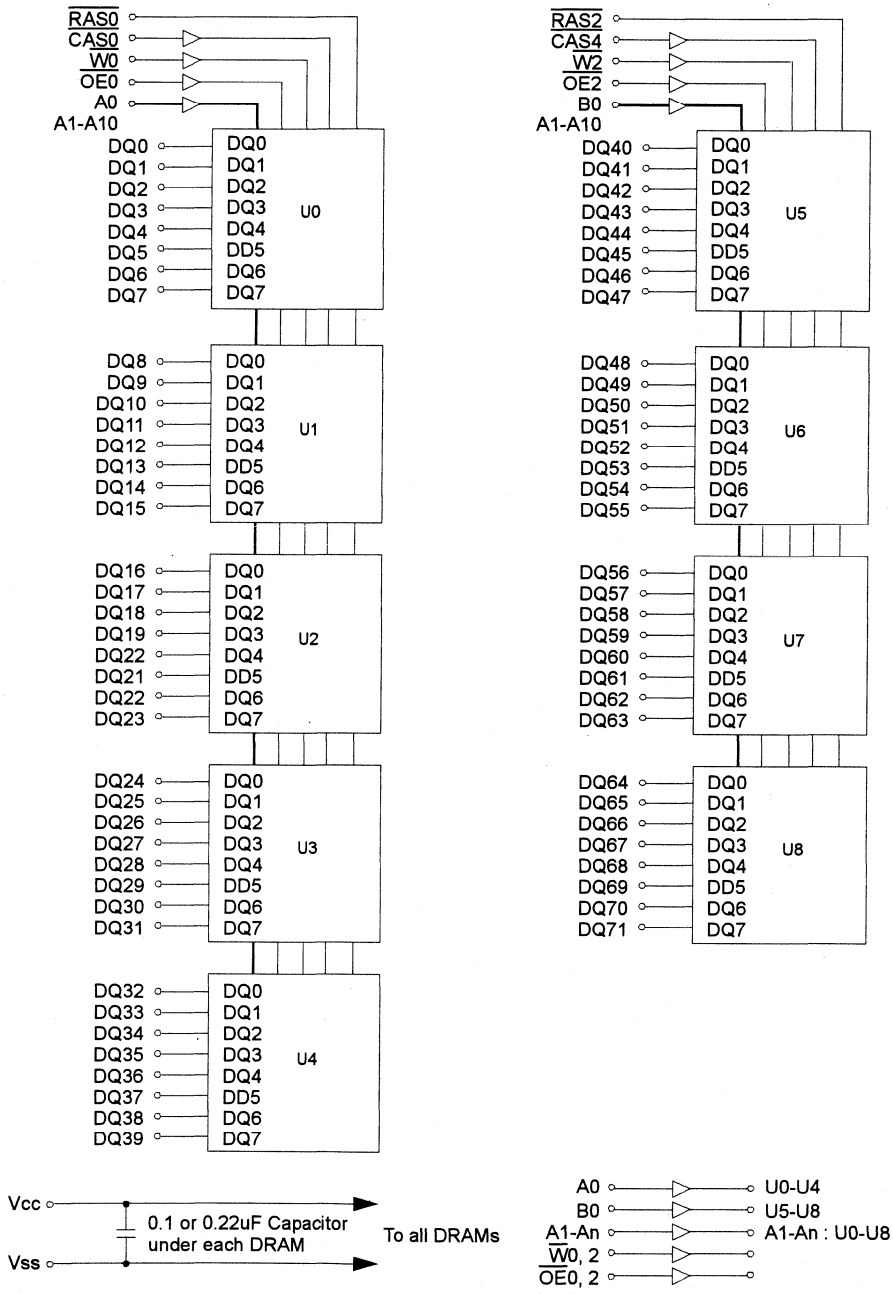
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	0	0
PD4	1	1
PD5	0	0
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	9	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : V_{CC}+2.0V/20ns, Pulse width is measured at V_{CC}.
*2 : -2.0V/20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372C213CK/CS		Unit
		Min	Max	
I_{CC1}	-5	-	990	mA
	-6	-	900	mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-5	-	990	mA
	-6	-	900	mA
I_{CC4}	-5	-	810	mA
	-6	-	720	mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-5	-	990	mA
	-6	-	900	mA
$I_{I(L)}$	Don't care	-25	25	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)
I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})
I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)
I_{CC4}*: Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)
I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)
I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)
$I_{I(L)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)
$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)
V_{OH} : Output High Voltage Level (I_{OH} = -5mA)
V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one page mode cycle, t_{PC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A10, B0]	C_{IN1}	-	15	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	17	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	38	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS4}$]	C_{IN4}	-	17	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ1}		17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,11
Access time from column address	t_{AA}		30		35	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,11
Output buffer turn-off delay	t_{OFF}	5	18	5	20	ns	6,11
Transition time(rise and fall)	t_T	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	11
$\overline{CAS}$ hold time	t_{CSH}	48		58		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	11
Row address set-up time	t_{ASR}	5		5		ns	11
Row address hold time	t_{RAH}	8		8		ns	11
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	11
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,11
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	18		20		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,11
Data hold time	t_{DH}	15		20		ns	9,11
Refresh period (2K refresh)	t_{REF}		32		32	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.4/0.8V$, $V_{oh}/V_{ol}=2.4/0.4V$, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	71		83		ns	7,11
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	11
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	11
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	3		3		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3,11
Fast page mode cycle time	t_{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	75		80		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	8		8		ns	11
$\overline{OE}$ access time	t_{OEA}		18		20	ns	11
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	11
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS} is not restrictive operating parameter. It included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

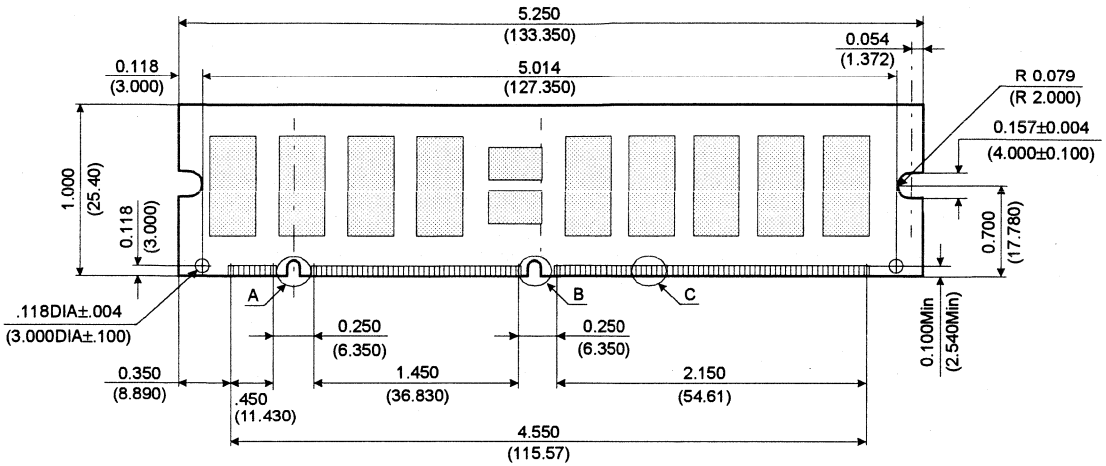
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

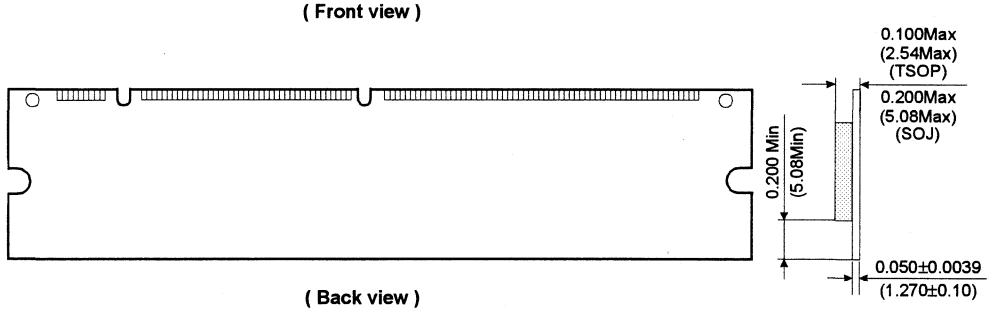
11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

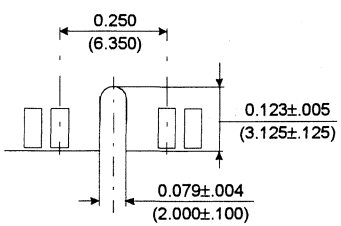
Units : Inches (millimeters)



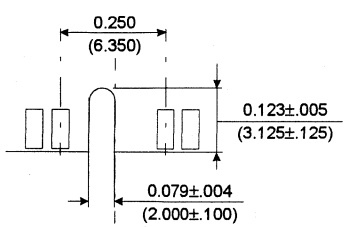
(Front view)



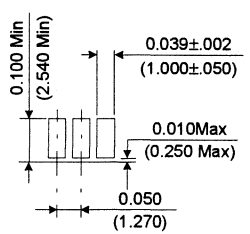
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 2Mx8 DRAM with Fast Page mode, SOJ or TSOP II (Forward).
DRAM Part No. : KMM372C213CK - KM48C2100CK
KMM372C213CS - KM48C2100CS

KMM372E213CK/CS EDO Mode

2Mx72 DRAM DIMM with ECC using 2Mx8, 2K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM372E213C is a 2Mx72bits Dynamic RAM high density memory module. The Samsung KMM372E213C consists of nine CMOS 2Mx8bits DRAMs in SOJ/TSOP-II 300mil package, and two 16bits driver IC in 48pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372E213C is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	18ns	84ns	20ns
-6	60ns	20ns	104ns	25ns

FEATURES

- Part Identification
  - KMM372E213CK (2048 cycles/32ms Ref., SOJ)
  - KMM372E213CS (2048 cycles/32ms Ref., TSOP)
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{RSVD}$	57	DQ22	85	Vss	113	$\overline{RSVD}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	*A11	150	DQ62
11	DQ8	39	*A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	$\overline{RFU}$	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	*$\overline{CAS5}$	158	DQ68
19	DQ14	47	$\overline{RSVD}$	75	DQ33	103	DQ50	131	$\overline{RSVD}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	$\overline{RFU}$	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	*$\overline{CAS1}$	140	DQ57	168	Vcc

PD Note : PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A10	Address Input
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

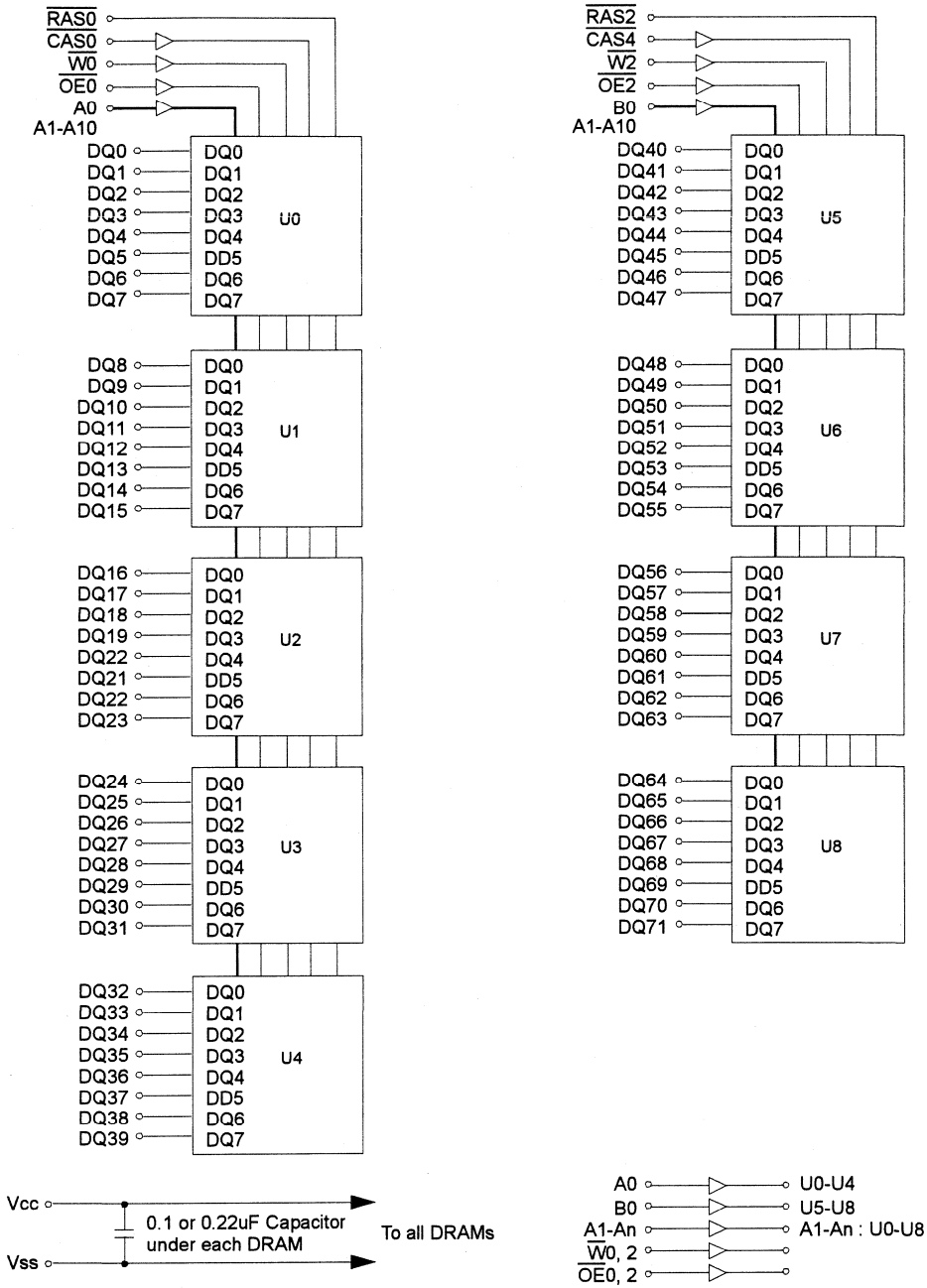
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	0	0
PD4	1	1
PD5	1	1
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



4

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	9	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V/20ns, Pulse width is measured at Vcc.
*2 : -2.0V/20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372E213CK/CS		Unit
		Min	Max	
I_{CC1}	-5	-	990	mA
	-6	-	900	mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-5	-	990	mA
	-6	-	900	mA
I_{CC4}	-5	-	810	mA
	-6	-	720	mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-5	-	990	mA
	-6	-	900	mA
$I_{I(L)}$	Don't care	-45	45	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)
I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})
I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)
I_{CC4}*: EDO Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)
I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)
I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)
$I_{I(L)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)
$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)
V_{OH} : Output High Voltage Level (I_{OH} = -5mA)
V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page mode cycle, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A10, B0]	C_{IN1}	-	15	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	17	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	45	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS4}$]	C_{IN4}	-	17	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ1}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	131		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,14
Access time from column address	t_{AA}		30		35	ns	3,10,14
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,14
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,14
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	20	ns	6,11,12,14
Transition time(rise and fall)	t_T	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	14
$\overline{CAS}$ hold time	t_{CSH}	36		43		ns	14
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	13
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,14
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,14
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	14
Row address set-up time	t_{ASR}	5		5		ns	14
Row address hold time	t_{RAH}	8		8		ns	14
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	14
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,14
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	18		20		ns	14
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,14
Data hold time	t_{DH}	13		15		ns	9,14
Refresh period(2K Ref.)	t_{REF}		32		32	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	71		83		ns	7,14

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.4/0.8V$, $V_{oh}/V_{ol}=2.0/0.8V$, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	
$\overline{CAS}$ set-up time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	14
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	14
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	14
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,14
Hyper page cycle time	t_{HPC}	20		25		ns	13
Hyper page read-modify-write cycle time	t_{HPRWC}	68		77		ns	13
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	14
$\overline{OE}$ access time	t_{OEA}		18		20	ns	14
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	14
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	7,11,14
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	14
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	14
Output data hold time	t_{DOH}	10		10		ns	14
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	6,11,12
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	3	18	3	20	ns	6,11,14
$\overline{W}$ to data delay	t_{WED}	20		20		ns	14
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width(Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2TTL loads and 100pF. Voh=2.0V and Vol=0.8V.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

   If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data output will contain data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out(at access time) is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. t_{CEZ}(max), t_{REZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.

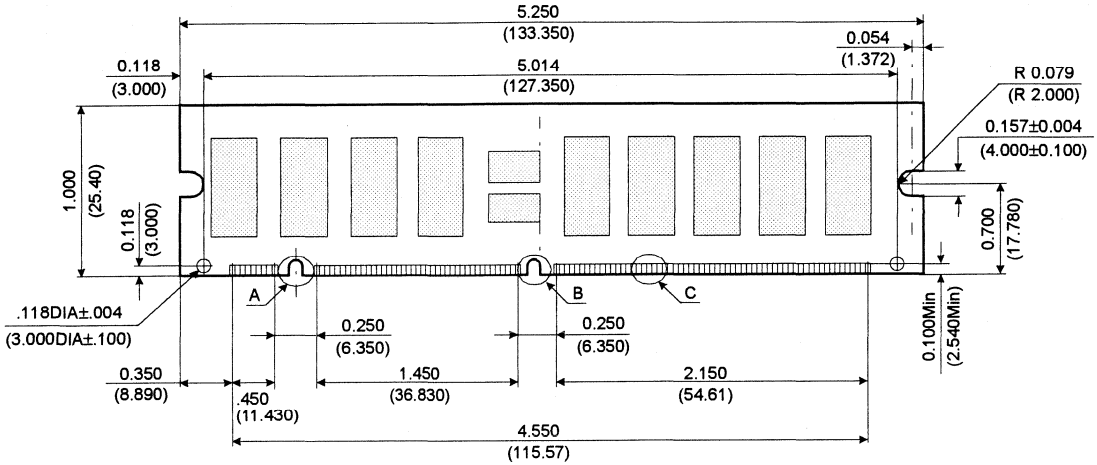
13. $t_{ASC} \geq t_{CP}$ min

14. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

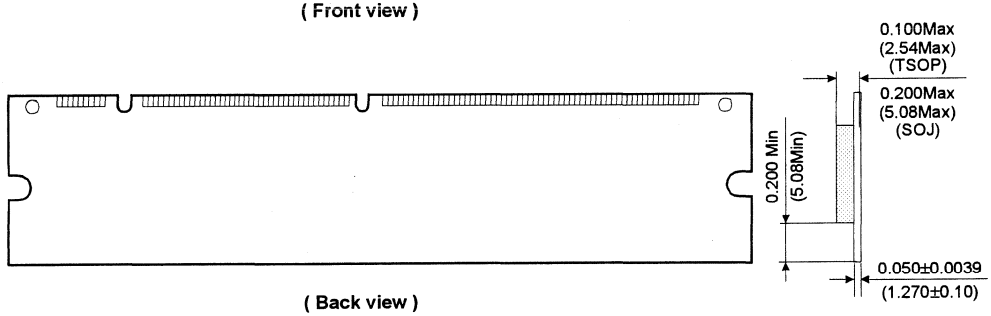
4

PACKAGE DIMENSIONS

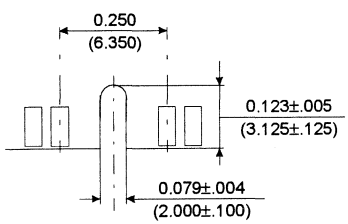
Units : Inches (millimeters)



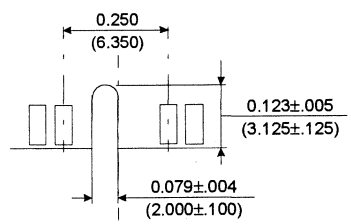
(Front view)



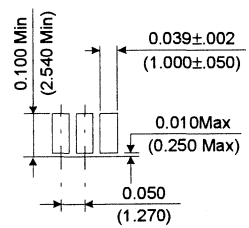
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 2Mx8 DRAM with EDO mode, SOJ or TSOP II (Forward).

DRAM Part No. : KMM372E213CK - KM48C2104CK

KMM372E213CS - KM48C2104CS

KMM364C40(8)4BS Fast Page Mode

4M x 64 DRAM DIMM Using 4Mx16, 4K & 8K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM364C40(8)4B is a 4Mx64bits Dynamic RAM high density memory module. The Samsung KMM364C40(8)4B consists of four CMOS 4Mx16bits DRAMs in TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM364C40(8)4B is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	18ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM364C404BS	TSOPII	4K	4K/64ms	
KMM364C484BS	TSOPII	8K	4K/64ms	8K/64ms

- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS2}$	57	DQ22	85	Vss	113	$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	*DQ26	94	DQ43	122	A11	150	*DQ62
11	*DQ8	39	A12	67	DQ27	95	*DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	$\overline{CAS6}$	75	DQ33	103	DQ50	131	$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	*DQ35	105	DQ52	133	Vcc	161	*DQ71
22	*DQ17	50	RSVD	78	Vss	106	*DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	$\overline{RFU}$	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM364C884BS (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a resistor to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
A0, B0, A1 - A12	Address Input(8K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

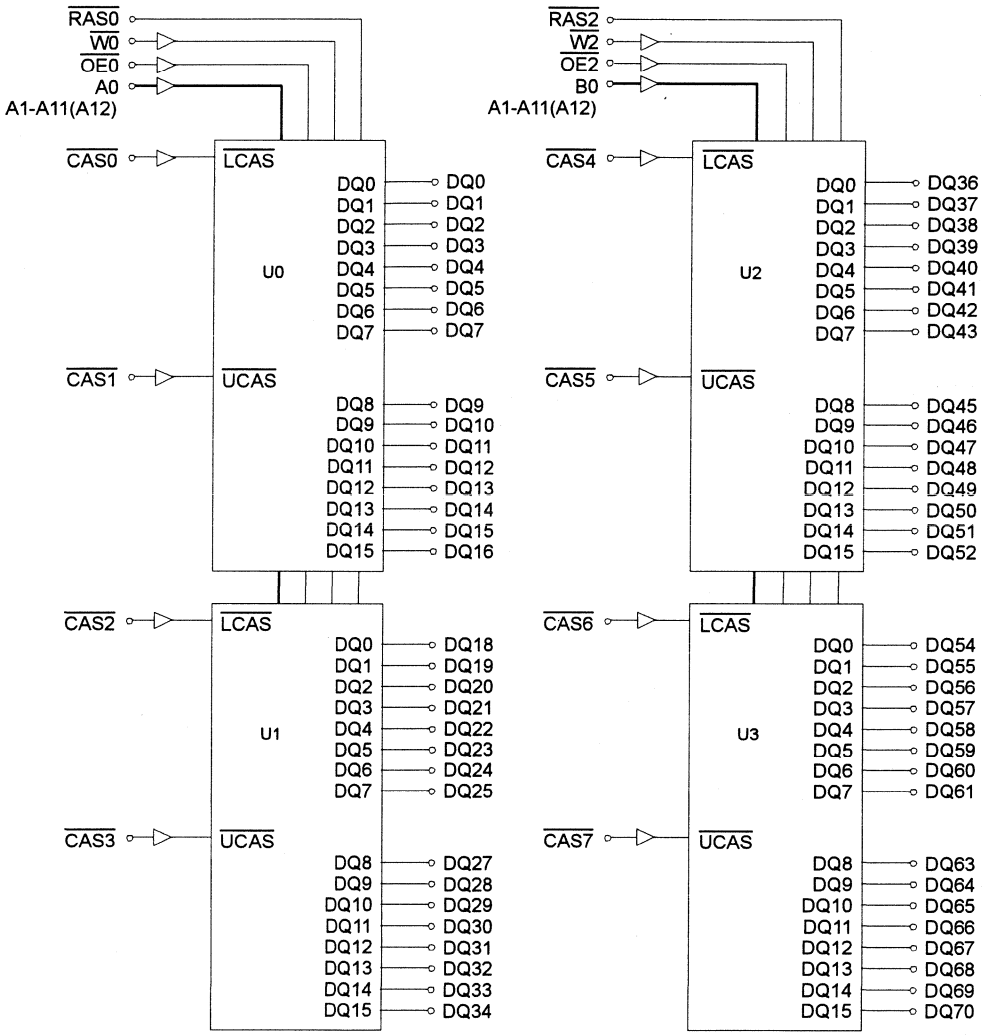
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	1	1
PD3	0	0
PD4	1	1
PD5	0	0
PD6	0	1
PD7	0	1
PD8	1	1
ID0	0	0
ID1	0	0

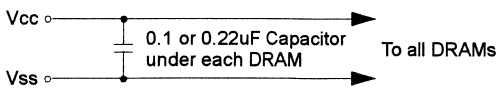
PD : 0 for Vol of Drive IC & 1 for N.C

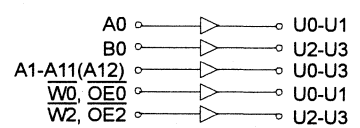
ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



Note : A12 is used for only KMM364C484BS (8K ref.)





ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	4	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM364C404BS		KMM364C484BS		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	480	-	360	mA
	-6	-	440	-	320	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	480	-	360	mA
	-6	-	440	-	320	mA
I_{CC4}	-5	-	280	-	240	mA
	-6	-	240	-	200	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	480	-	360	mA
	-6	-	440	-	320	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	24	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.6/0.8V, V_{oh}/V_{ol}=2.4/0.4V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,11
Access time from column address	t_{AA}		30		35	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,11
Output buffer turn-off delay	t_{OFF}	5	18	5	20	ns	6,11
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	11
$\overline{CAS}$ hold time	t_{CSH}	45		55		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	11
Row address set-up time	t_{ASR}	5		5		ns	11
Row address hold time	t_{RAH}	8		8		ns	11
Column address set-up time	t_{ASC}	0		0		ns	12
Column address hold time	t_{CAH}	10		10		ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	11
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referencde to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,11
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	15
Data in set-up time	t_{DS}	-2		-2		ns	9,11
Data in hold time	t_{DH}	15		15		ns	9,11
Refresh period	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7,15
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ prechange to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{RAS}$ ro $\overline{W}$ delay time	t_{RWD}	73		85		ns	7,11
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	11,16
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	11
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3,11
Fast page mode cycle time	t_{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	76		85		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	13
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}		18		20	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}		30		35	ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	50	200K	60	200K	ns	11
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	35		40		ns	11
$\overline{OE}$ access time	t_{OEA}	15		15		ns	11
$\overline{OE}$ to data delay	t_{OED}	8		8		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}		18		20	ns	11
$\overline{OE}$ command hold time	t_{OEH}	18		20		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

12. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.

13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

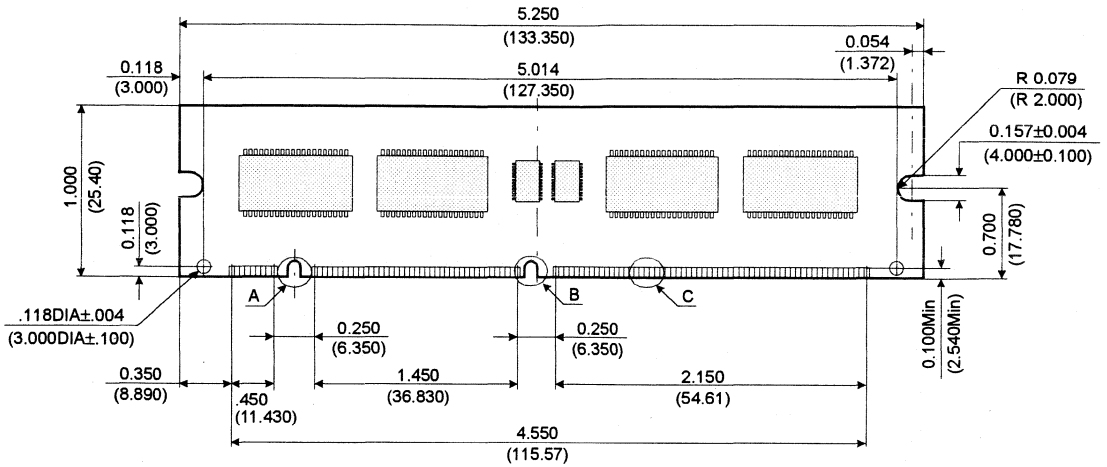
14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

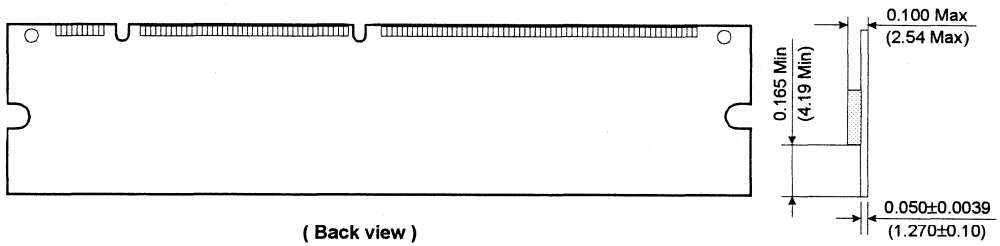
16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.

PACKAGE DIMENSIONS

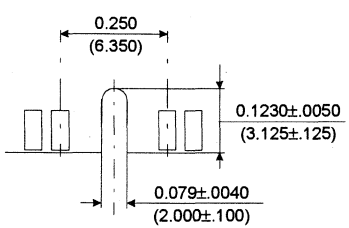
Units : Inches (millimeters)



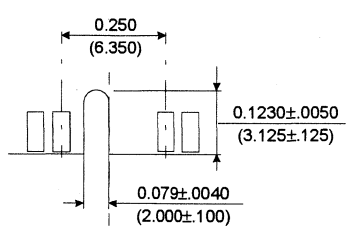
(Front view)



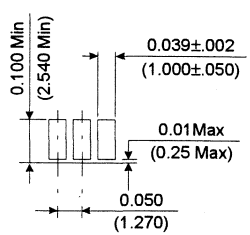
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 DRAM with Fast page mode, TSOP II.
DRAM Part No. : KMM364C404BS - KM416C4100BS.
KMM364C484BS - KM416C4000BS.

KMM364E40(8)4BS EDO Mode

4M x 64 DRAM DIMM Using 4Mx16, 4K & 8K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM364E40(8)4B is a 4Mx64bits Dynamic RAM high density memory module. The Samsung KMM364E40(8)4B consists of four CMOS 4Mx16bits DRAMs in TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM364E40(8)4B is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	18ns	84ns	20ns
-6	60ns	20ns	104ns	25ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM364E404BS	TSOPII	4K	4K/64ms	
KMM364E484BS	TSOPII	8K	4K/64ms	8K/64ms

- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS2}$	57	DQ22	85	Vss	113	$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	*DQ26	94	DQ43	122	A11	150	*DQ62
11	*DQ8	39	A12	67	DQ27	95	*DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	$\overline{CAS6}$	75	DQ33	103	DQ50	131	$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	*DQ35	105	DQ52	133	Vcc	161	*DQ71
22	*DQ17	50	RSVD	78	Vss	106	*DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM364E884BS (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a resistor to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
A0, B0, A1 - A12	Address Input(8K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

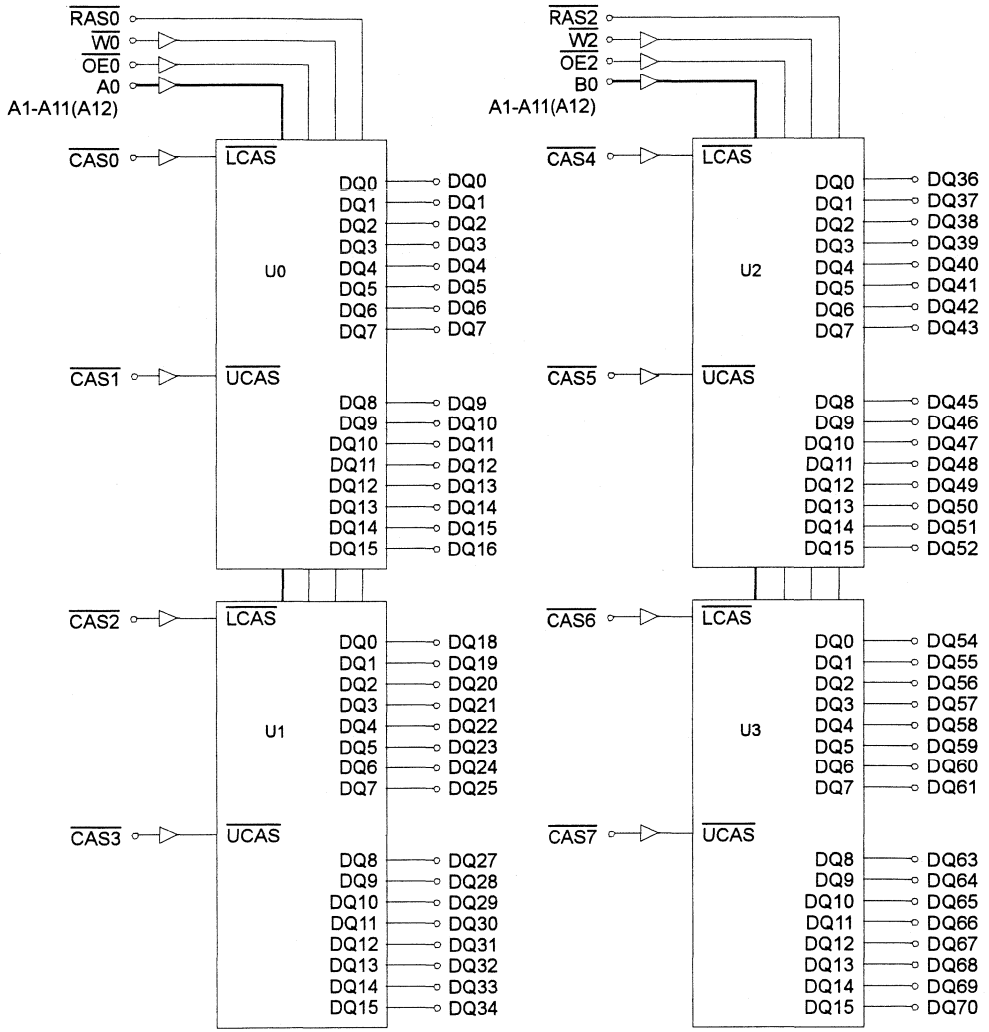
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	1	1
PD3	0	0
PD4	1	1
PD5	1	1
PD6	0	1
PD7	0	1
PD8	1	1
ID0	0	0
ID1	0	0

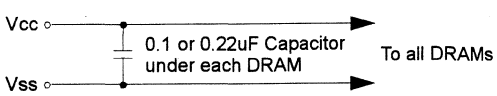
PD : 0 for Vol of Drive IC & 1 for N.C

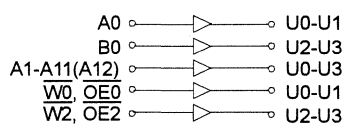
ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



Note : A12 is used for only KMM364E484BS (8K ref.)





ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	4	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : V_{CC}+2.0V at pulse width≤20ns, which is measured at V_{CC}.

*2 : -2.0V at pulse width≤20ns, which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM364E404BS		KMM364E484BS		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	480	-	360	mA
	-6	-	440	-	320	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	480	-	360	mA
	-6	-	440	-	320	mA
I_{CC4}	-5	-	440	-	400	mA
	-6	-	400	-	360	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	480	-	360	mA
	-6	-	440	-	320	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	24	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.6/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,13
Access time from column address	t_{AA}		30		35	ns	3,10,13
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,13
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,13
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	18	ns	6,11,13
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	13
$\overline{CAS}$ hold time	t_{CSH}	36		43		ns	13
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,13
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	13
Row address set-up time	t_{ASR}	5		5		ns	13
Row address hold time	t_{RAH}	8		8		ns	13
Column address set-up time	t_{ASC}	0		0		ns	14
Column address hold time	t_{CAH}	8		10		ns	14
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	13
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,13
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	18		20		ns	13
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	17
Data set-up time	t_{DS}	-2		-2		ns	9,13
Data hold time	t_{DH}	13		15		ns	9,13
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		38		ns	7,16
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		83		ns	7,13

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	48		53		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	13,18
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	13
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,13
Hyper page cycle time	t_{HPC}	20		25		ns	12
Hyper page read-modify-write cycle time	t_{HPRWC}	70		77		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	8		10		ns	15
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	13
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	13
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	13
$\overline{OE}$ access time	t_{OEA}		18		20	ns	13
$\overline{OE}$ to data delay	t_{OED}	18		18		ns	13
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	8	18	8	18	ns	13
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Output data hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{DOH}	10		10		ns	13
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	15	3	15	ns	6,11
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	8	18	8	20	ns	6,13
$\overline{W}$ to data delay	t_{WED}	20		20		ns	13
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

12. $t_{ASC} \geq 6$ns.

13. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

14. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.

15. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

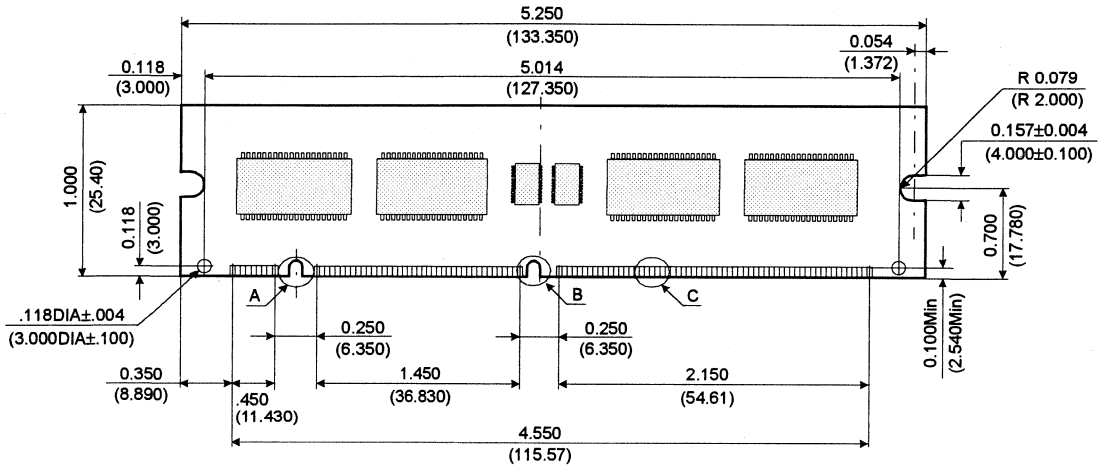
16. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

17. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

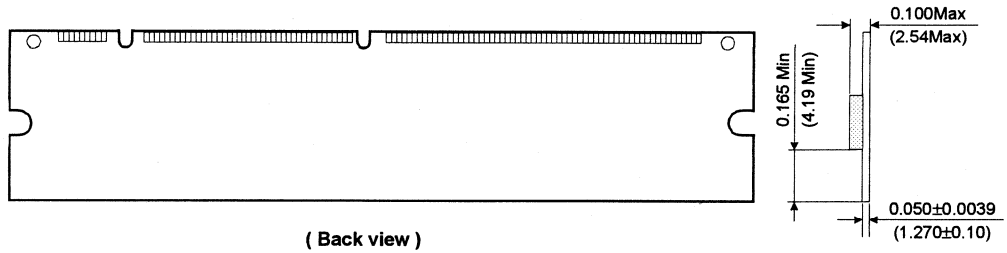
18. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.

PACKAGE DIMENSIONS

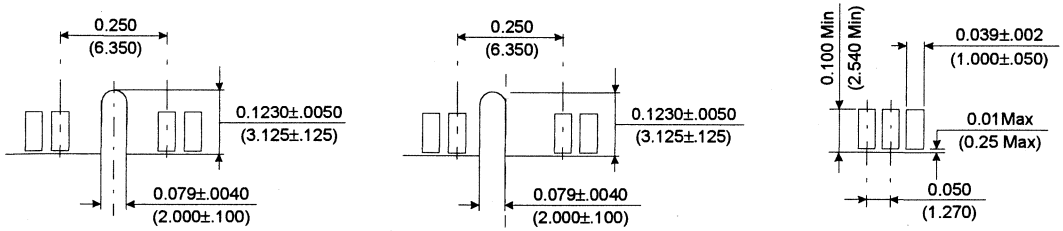
Units : Inches (millimeters)



(Front view)



(Back view)



Detail A Detail B Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 DRAM with EDO mode, TSOP II.
DRAM Part No. : KMM364E404BS - KM416C4104BS.
KMM364E484BS - KM416C4004BS.

KMM372C404BS Fast Page Mode

4M x 72 DRAM DIMM with ECC Using 4Mx16 & 4Mx4 , 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM372C404B is a 4Mx72bits Dynamic RAM high density memory module. The Samsung KMM372C404B consists of four 4Mx16bits & two 4Mx4bits CMOS DRAMs in TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372C404B is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	tRAC	tCAC	tRC	tPC
-5	50ns	18ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

FEATURES

- Part Identification
  - KMM372C404BS(4096cycles/64ms Ref. TSOP II)
- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	*$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	*$\overline{CAS1}$	140	DQ57	168	Vcc

PD Note :PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

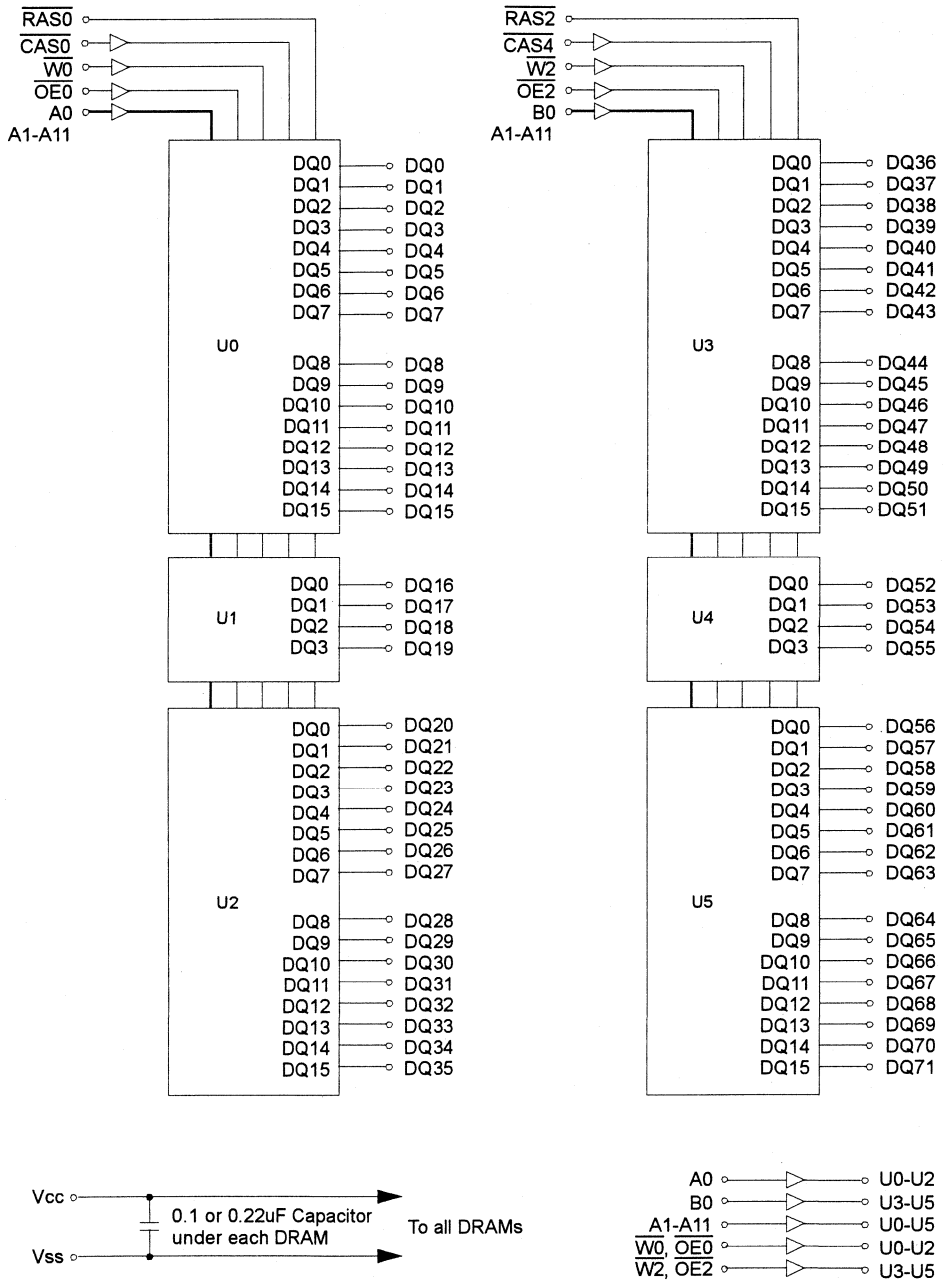
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	1	1
PD3	0	0
PD4	1	1
PD5	0	0
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	6	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372C404BS		Unit
		Min	Max	
I_{CC1}	-5 -6	- -	720 660	mA mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-5 -6	- -	720 660	mA mA
I_{CC4}	-5 -6	- -	420 360	mA mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-5 -6	- -	720 660	mA mA
$I_{I(L)}$ $I_{O(L)}$	Don't care	-10 -5	10 5	uA uA
V_{OH} V_{OL}	Don't care	2.4 -	- 0.4	V V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast Page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A11]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	31	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS4}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.6/0.8V, V_{oh}/V_{ol}=2.4/0.4V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,11
Access time from column address	t_{AA}		30		35	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,11
Output buffer turn-off delay	t_{OFF}	5	18	5	20	ns	6,11
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	11
$\overline{CAS}$ hold time	t_{CSH}	45		55		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	11
Row address set-up time	t_{ASR}	5		5		ns	11
Row address hold time	t_{RAH}	8		8		ns	11
Column address set-up time	t_{ASC}	0		0		ns	12
Column address hold time	t_{CAH}	10		10		ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	11
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referencde to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,11
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	15
Data in set-up time	t_{DS}	-2		-2		ns	9,11
Data in hold time	t_{DH}	15		15		ns	9,11
Refresh period	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7,15
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ prechange to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{RAS}$ ro $\overline{W}$ delay time	t_{RWD}	73		85		ns	7,11
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	11,16
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	11
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3,11
Fast page mode cycle time	t_{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	76		85		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	13
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	11
$\overline{OE}$ access time	t_{OEA}		18		20	ns	11
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	11
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

12. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.

13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

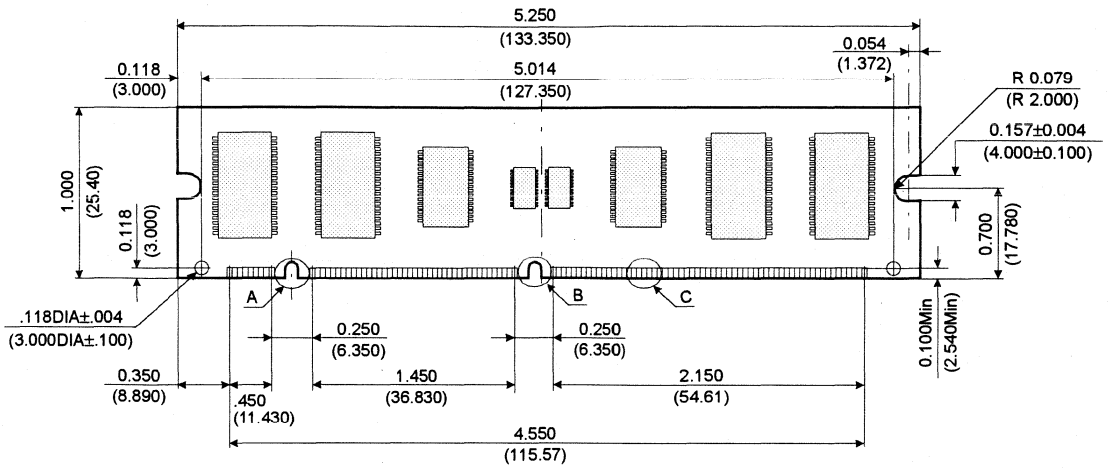
14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

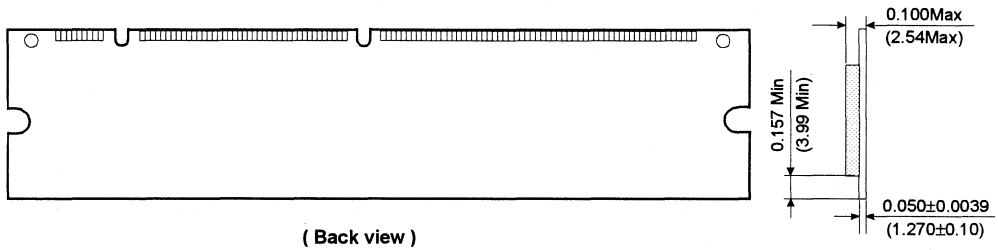
16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.

PACKAGE DIMENSIONS

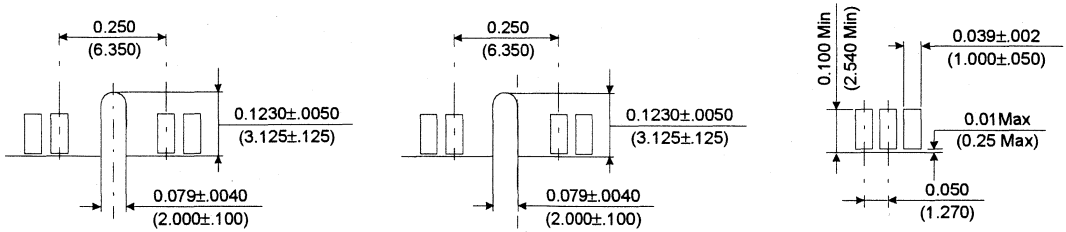
Units : Inches (millimeters)



(Front view)



(Back view)



Detail A Detail B Detail C

Tolerances :±.005(.13) unless otherwise specified

The used device is 4Mx16 & 4Mx4 DRAM with Fast Page mode, TSOP II.
DRAM Part No. : KMM372C404BS -KM416C4100BS & KM44C4000CS

KMM372E404BK/BS EDO Mode

4M x 72 DRAM DIMM Using 4Mx16 & 4Mx4, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM372E404B is a 4Mx72bits Dynamic RAM high density memory module. The Samsung KMM372E404B consists of four 4Mx16bits & two 4Mx4bits CMOS DRAM in SOJ/TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372E404B is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	18ns	84ns	20ns
-6	60ns	20ns	104ns	25ns

FEATURES

- Part Identification
  - KMM372E404BS(4096cycles/64ms Ref. TSOP II)
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	*$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	*$\overline{CAS1}$	140	DQ57	168	Vcc

PD Note :PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

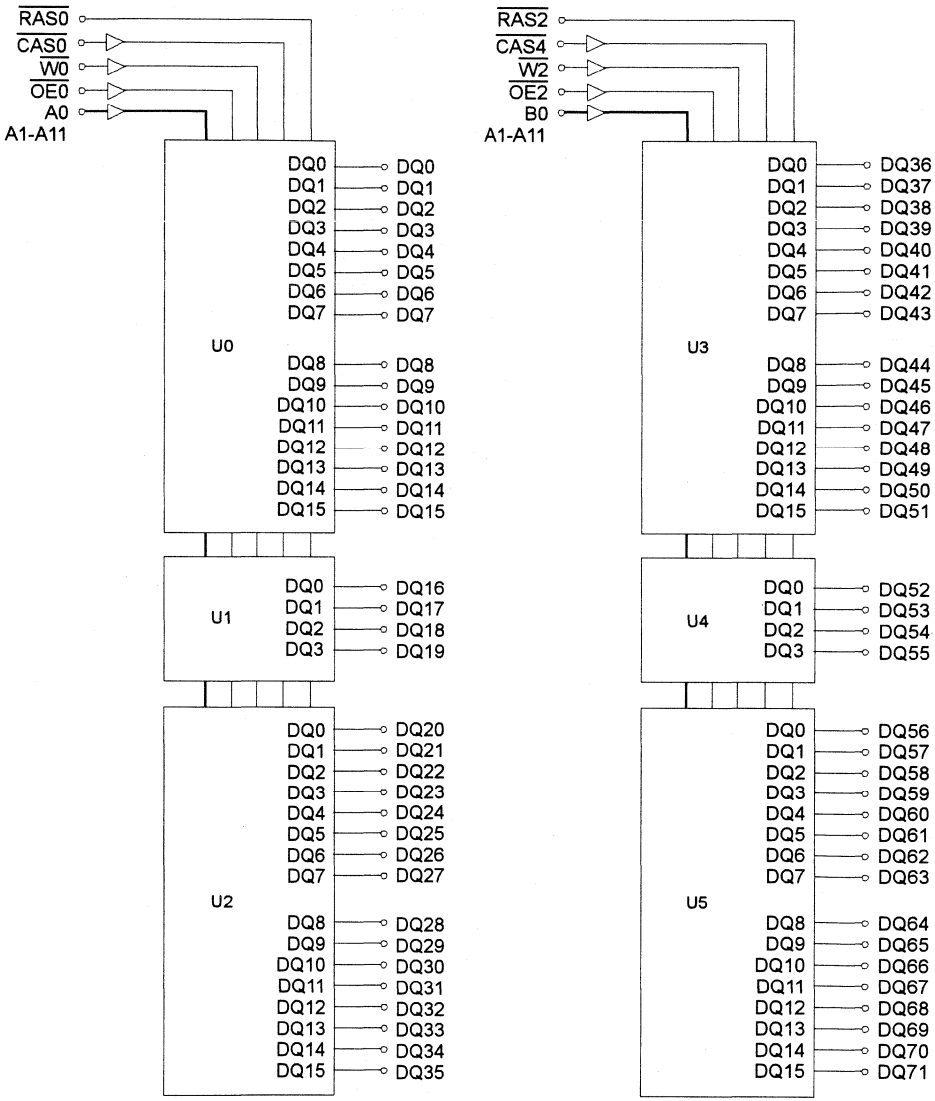
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	1	1
PD3	0	0
PD4	1	1
PD5	1	1
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	6	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372E404BS		Unit
		Min	Max	
I_{CC1}	-5 -6	- -	720 660	mA mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-5 -6	- -	720 660	mA mA
I_{CC4}	-5 -6	- -	660 600	mA mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-5 -6	- -	720 660	mA mA
$I_{I(L)}$ $I_{O(L)}$	Don't care	-10 -5	10 5	uA uA
V_{OH} V_{OL}	Don't care	2.4 -	- 0.4	V V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A11]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	31	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS4}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.6/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,13
Access time from column address	t_{AA}		30		35	ns	3,10,13
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,13
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,13
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	18	ns	6,11,13
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	13
$\overline{CAS}$ hold time	t_{CSH}	36		43		ns	13
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,13
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	13
Row address set-up time	t_{ASR}	5		5		ns	13
Row address hold time	t_{RAH}	8		8		ns	13
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	13
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,13
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	18		20		ns	13
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,13
Data hold time	t_{DH}	13		15		ns	9,13
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		38		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		83		ns	7,13

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	48		53		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	13
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	13
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,13
Hyper page cycle time	t_{HPC}	20		25		ns	12
Hyper page read-modify-write cycle time	t_{HPRWC}	70		77		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	13
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	13
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	13
$\overline{OE}$ access time	t_{OEA}		18		20	ns	13
$\overline{OE}$ to data delay	t_{OED}	18		18		ns	13
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	8	18	8	18	ns	13
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Output data hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{DOH}	10		10		ns	13
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	15	3	15	ns	6,11
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	8	18	8	20	ns	6,13
$\overline{W}$ to data delay	t_{WED}	20		20		ns	13
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
   If t_{RWD}¡Ât$_{RWD}$(min), t_{CWD}¡Ât$_{CWD}$(min), t_{AWD}¡Ât$_{AWD}$(min) and t_{CPWD}¡Ât$_{CPWD}$(min).
   The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

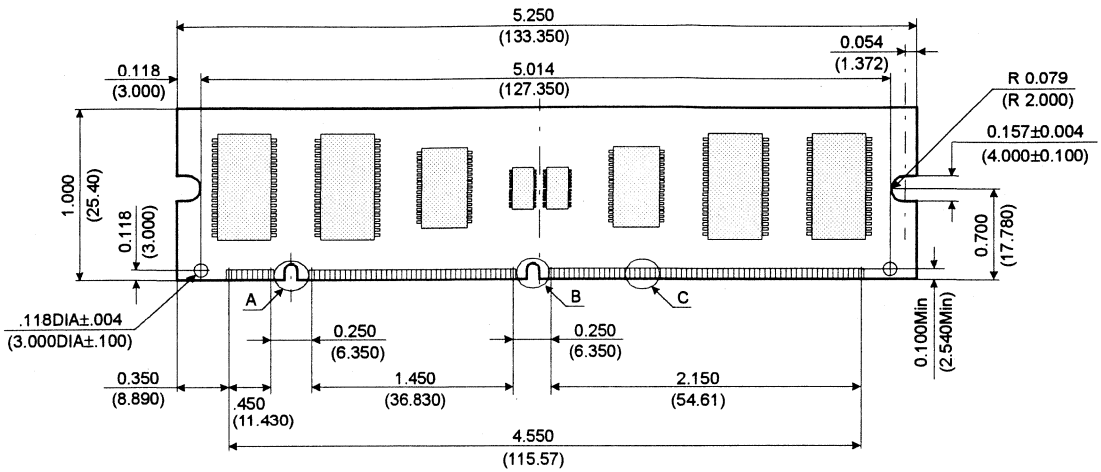
12. $t_{ASC} \geq 6ns$.

13. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

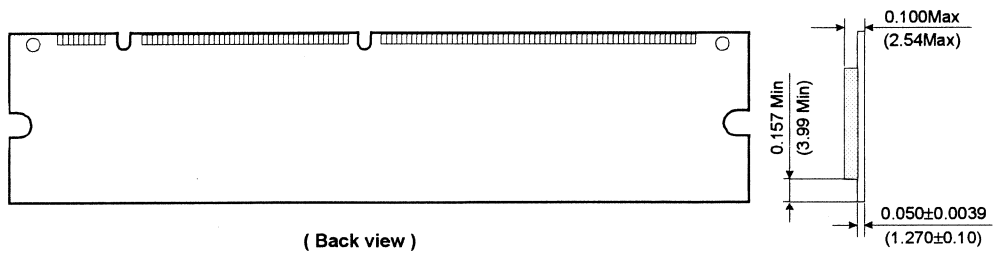
4

PACKAGE DIMENSIONS

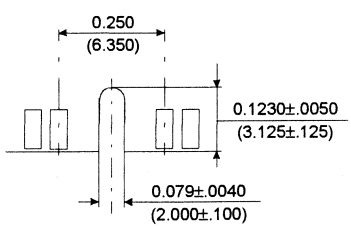
Units : Inches (millimeters)



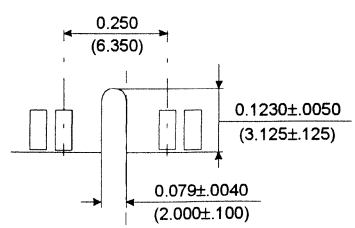
(Front view)



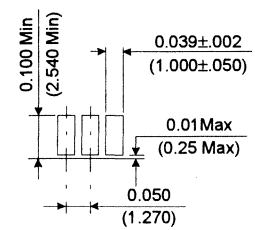
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 & 4Mx4 DRAM with EDO mode, TSOP II.
DRAM Part No. : KMM372E404BS -KM416C4104BS & KM44C4004CS

KMM364C80(8)3BK/BS Fast Page Mode

8M x 64 DRAM DIMM Using 8Mx8, 4K & 8K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM364C80(8)3B is a 8Mx64bits Dynamic RAM high density memory module. The Samsung KMM364C80(8)3B consists of eight CMOS 8Mx8bits DRAMs in SOJ/TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM364C80(8)3B is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	18ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

FEATURES

• Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM364C803BK	SOJ	4K	4K/64ms	
KMM364C803BS	TSOP			
KMM364C883BK	SOJ	8K	4K/64ms	8K/64ms
KMM364C883BS	TSOP			

- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1250mil), single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS2}$	57	DQ22	85	Vss	113	$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	*DQ26	94	DQ43	122	A11	150	*DQ62
11	*DQ8	39	A12	67	DQ27	95	*DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	$\overline{CAS6}$	75	DQ33	103	DQ50	131	$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	*DQ35	105	DQ52	133	Vcc	161	*DQ71
22	*DQ17	50	RSVD	78	Vss	106	*DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM364C880BK/BS (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a resistor to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
A0, B0, A1 - A12	Address Input(8K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

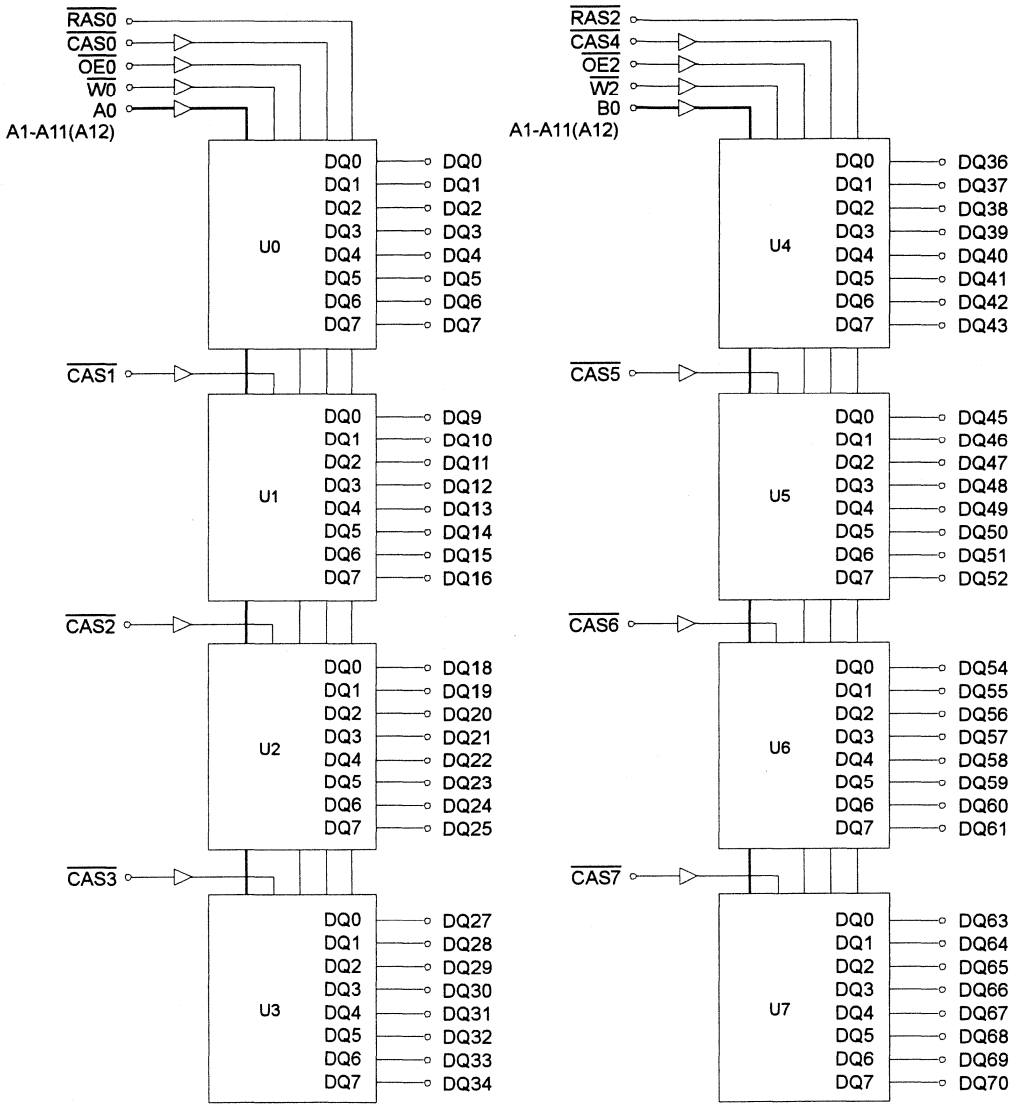
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	1	1
PD4	1	1
PD5	0	0
PD6	0	1
PD7	0	1
PD8	1	1
ID0	0	0
ID1	0	0

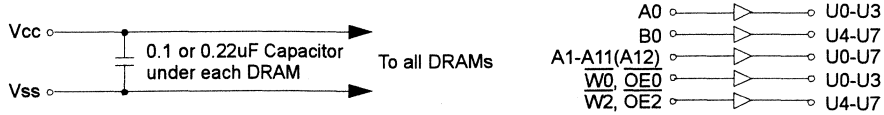
PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM364C880BK/BS(8K Ref.)



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM364C803BK/BS		KMM364C883BK/BS		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	960	-	720	mA
	-6	-	880	-	640	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	960	-	720	mA
	-6	-	880	-	640	mA
I_{CC4}	-5	-	560	-	480	mA
	-6	-	480	-	400	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	960	-	720	mA
	-6	-	880	-	640	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	38	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,11
Access time from column address	t_{AA}		30		35	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,11
Output buffer turn-off delay	t_{OFF}	5	18	5	20	ns	6,11
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	11
$\overline{CAS}$ hold time	t_{CSH}	45		55		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	11
Row address set-up time	t_{ASR}	5		5		ns	11
Row address hold time	t_{RAH}	8		8		ns	11
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	11
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referencde to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,11
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data in set-up time	t_{DS}	-2		-2		ns	9,11
Data in hold time	t_{DH}	15		15		ns	9,11
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ prechange to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7
$\overline{RAS}$ ro $\overline{W}$ delay time	t_{RWD}	73		85		ns	7,11

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	11
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	11
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3,11
Fast page mode cycle time	t_{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	76		85		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	11
$\overline{OE}$ access time	t_{OEA}		18		20	ns	11
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	11
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \ge t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \ge t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \ge t_{RWD}$(min), $t_{CWD} \ge t_{CWD}$(min), $t_{AWD} \ge t_{AWD}$(min) and $t_{CPWD} \ge t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

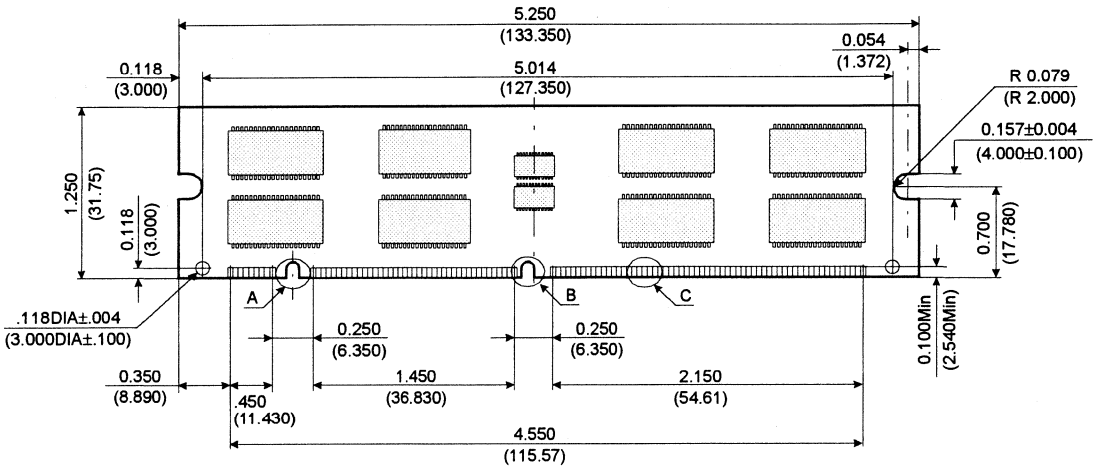
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

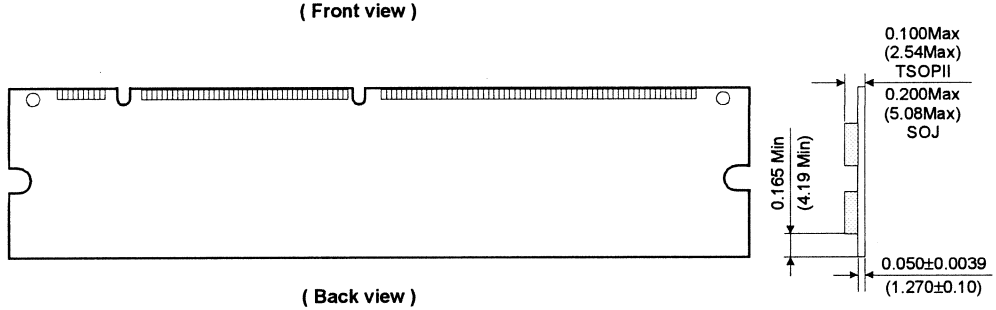
11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

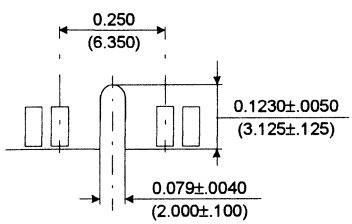
Units : Inches (millimeters)



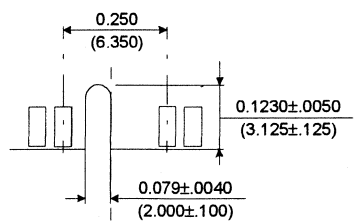
(Front view)



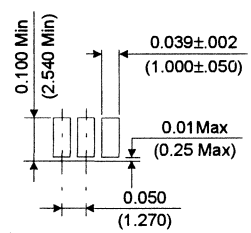
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 DRAM with Fast page mode, SOJ or TSOPII.
DRAM Part No. : KMM364C803BK/BS - KM48C8100BK, KM48C8100BS.
KMM364C883BK/BS - KM48C8000BK, KM48C8000BS.

KMM364E80(8)3BK/BS EDO Mode

8M x 64 DRAM DIMM Using 8Mx8, 4K & 8K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM364E80(8)3B is a 8Mx64bits Dynamic RAM high density memory module. The Samsung KMM364E80(8)3B consists of eight CMOS 8Mx8bits DRAMs in SOJ/TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM364E80(8)3B is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	18ns	84ns	20ns
-6	60ns	20ns	104ns	25ns

FEATURES

Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM364E803BK	SOJ	4K	4K/64ms	
KMM364E803BS	TSOP			
KMM364E883BK	SOJ	8K	4K/64ms	8K/64ms
KMM364E883BS	TSOP			

- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1250mil), single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS2}$	57	DQ22	85	Vss	113	$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	*DQ26	94	DQ43	122	A11	150	*DQ62
11	*DQ8	39	A12	67	DQ27	95	*DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	$\overline{CAS6}$	75	DQ33	103	DQ50	131	$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	*DQ35	105	DQ52	133	Vcc	161	*DQ71
22	*DQ17	50	RSVD	78	Vss	106	*DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM364E880BK/BS (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a resistor to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
A0, B0, A1 - A12	Address Input(8K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

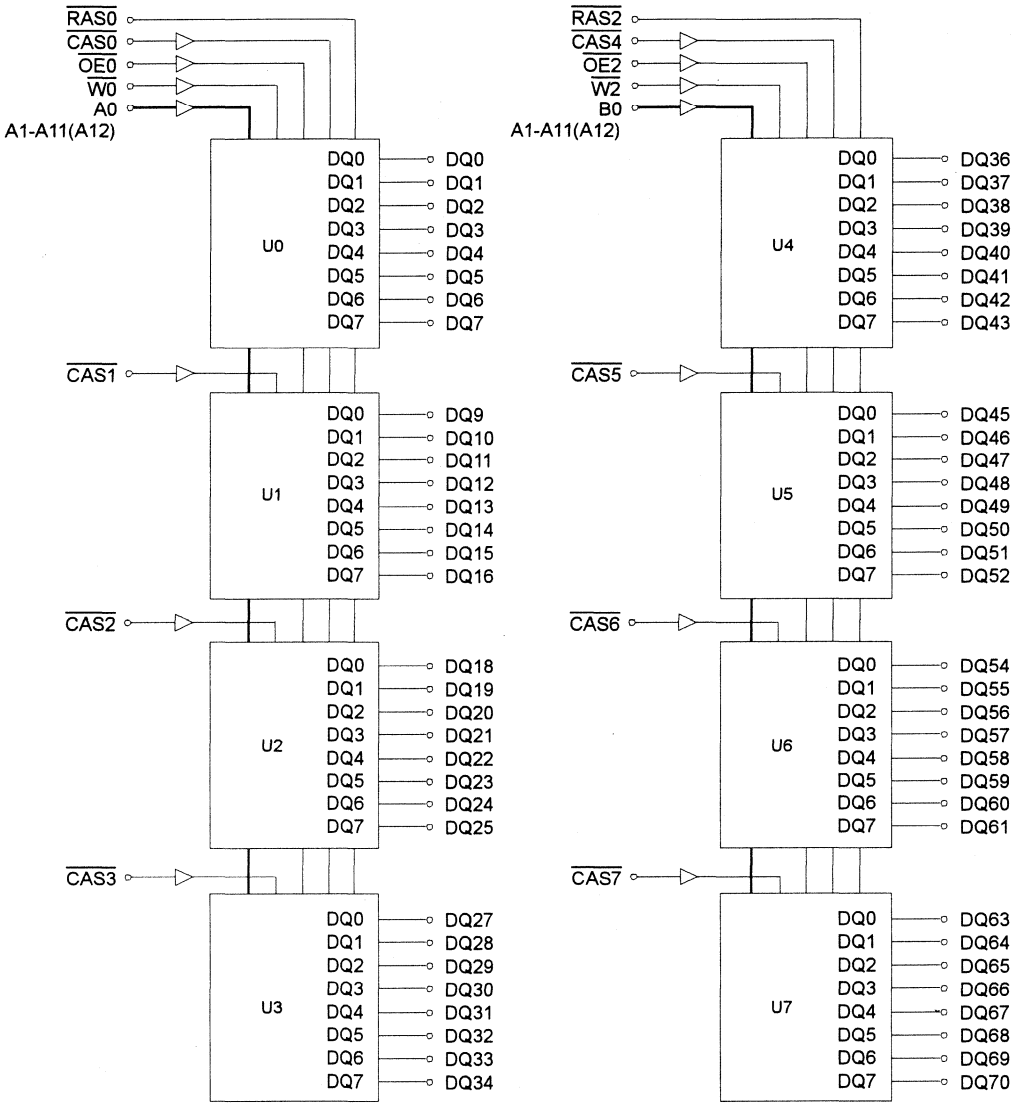
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	1	1
PD4	1	1
PD5	1	1
PD6	0	1
PD7	0	1
PD8	1	1
ID0	0	0
ID1	0	0

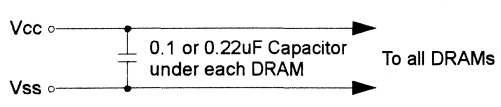
PD : 0 for Vol of Drive IC & 1 for N.C

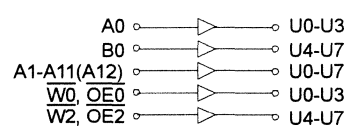
ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM364E880BK/BS(8K Ref.)





ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speedl	KMM364E803BK/BS		KMM364E883BK/BS		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	960	-	720	mA
	-6	-	880	-	640	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	960	-	720	mA
	-6	-	880	-	640	mA
I_{CC4}	-5	-	880	-	800	mA
	-6	-	800	-	720	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	960	-	720	mA
	-6	-	880	-	640	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}¡ÂVcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	38	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,13
Access time from column address	t_{AA}		30		35	ns	3,10,13
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,13
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,13
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	18	ns	6,11,13
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	13
$\overline{CAS}$ hold time	t_{CSH}	36		43		ns	13
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,13
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	13
Row address set-up time	t_{ASR}	5		5		ns	13
Row address hold time	t_{RAH}	8		8		ns	13
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	13
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,13
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	18		20		ns	13
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,13
Data hold time	t_{DH}	13		15		ns	9,13
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		38		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		83		ns	7,13

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	48		53		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	13
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	13
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,13
Hyper page cycle time	t_{HPC}	20		25		ns	12
Hyper page read-modify-write cycle time	t_{HPRWC}	70		77		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	13
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	13
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	13
$\overline{OE}$ access time	t_{OEA}		18		20	ns	13
$\overline{OE}$ to data delay	t_{OED}	18		18		ns	13
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	8	18	8	18	ns	13
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Output data hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{DOH}	10		10		ns	13
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	15	3	15	ns	6,11
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	8	18	8	20	ns	6,13
$\overline{W}$ to data delay	t_{WED}	20		20		ns	13
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

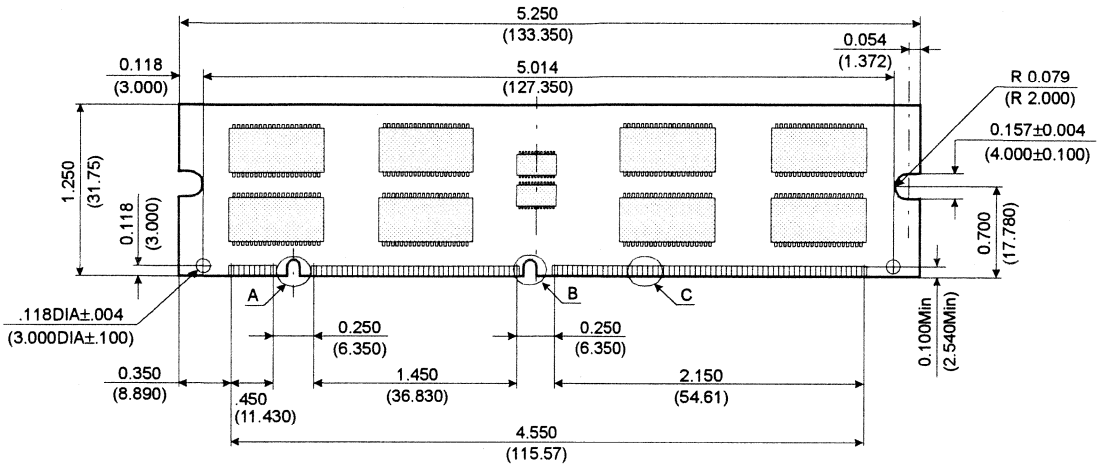
11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

12. $t_{ASC} \geq 6$ns.

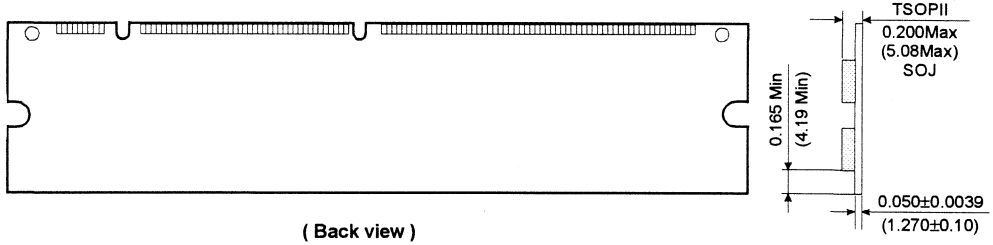
13. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

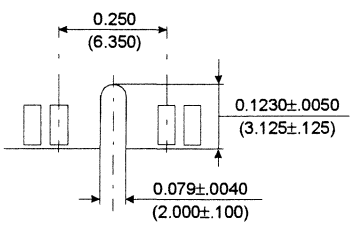
Units : Inches (millimeters)



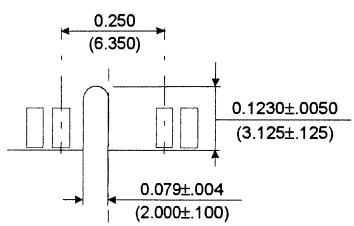
(Front view)



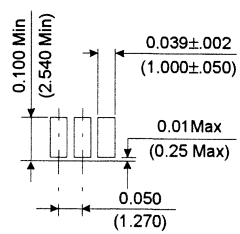
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 DRAM with EDO mode, SOJ or TSOPII.
DRAM Part No. : KMM364E803BK/BS - KM48C8104BK, KM48C8104BS.
KMM364E883BK/BS - KM48C8004BK, KM48C8004BS.

KMM364C80(8)4BS Fast Page Mode

8M x 64 DRAM DIMM Using 4Mx16, 4K & 8K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM364C80(8)4B is a 4Mx64bits Dynamic RAM high density memory module. The Samsung KMM364C80(8)4B consists of eight CMOS 4Mx16bits DRAMs in TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM364C80(8)4B is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	18ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

FEATURES

• Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM364C804BS	TSOPII	4K	4K/64ms	
KMM364C884BS	TSOPII	8K	4K/64ms	8K/64ms

- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS2}$	57	DQ22	85	Vss	113	$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	*DQ26	94	DQ43	122	A11	150	*DQ62
11	*DQ8	39	A12	67	DQ27	95	*DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	$\overline{CAS6}$	75	DQ33	103	DQ50	131	$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	*DQ35	105	DQ52	133	Vcc	161	*DQ71
22	*DQ17	50	RSVD	78	Vss	106	*DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM364C880BS (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a resistor to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
A0, B0, A1 - A12	Address Input(8K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future

Pins marked '*' are not used in this module.

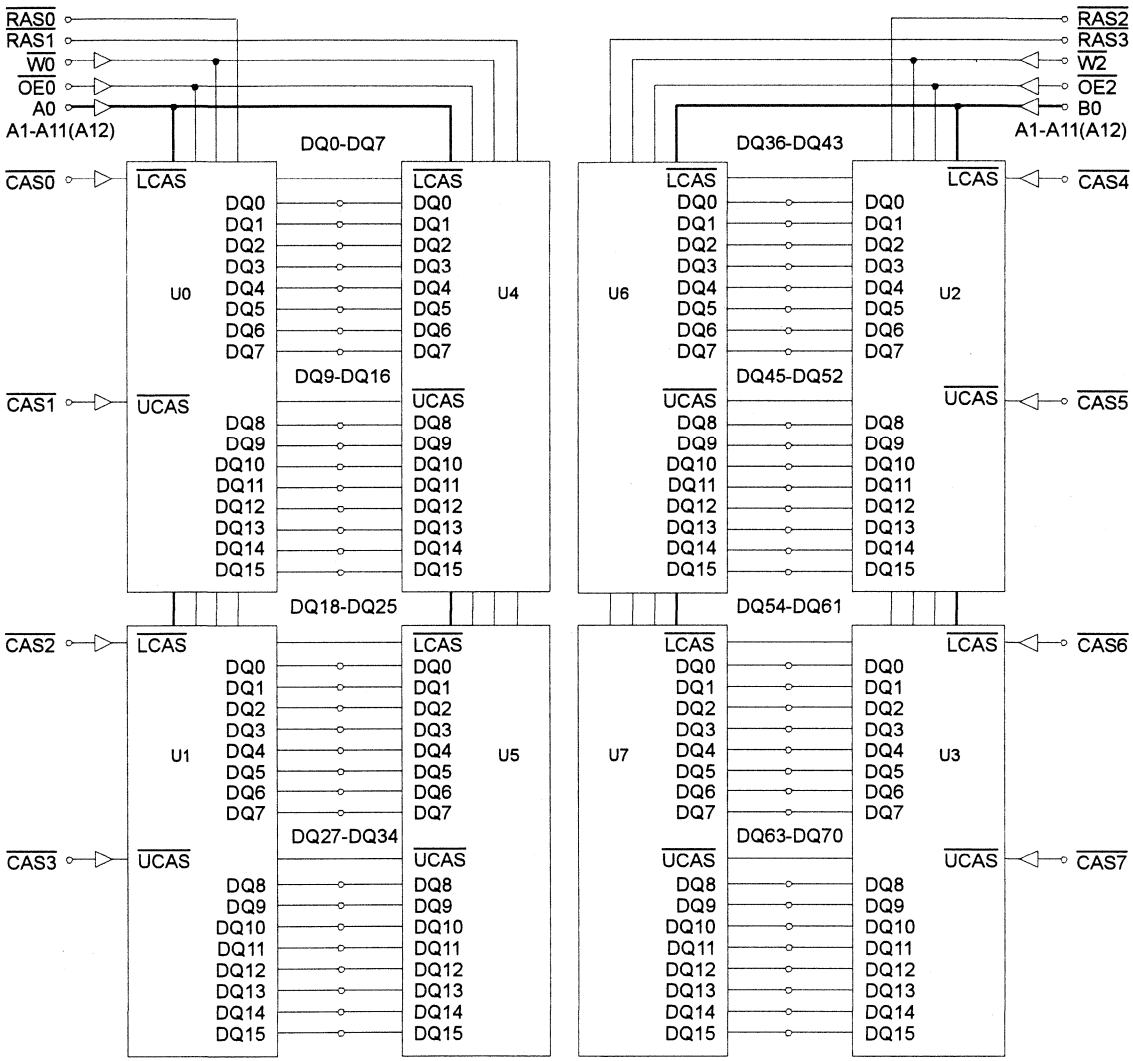
PD & ID Table

Pin	50NS	60NS
PD1	0	0
PD2	0	0
PD3	1	1
PD4	1	1
PD5	0	0
PD6	0	1
PD7	0	1
PD8	1	1
ID0	0	0
ID1	0	0

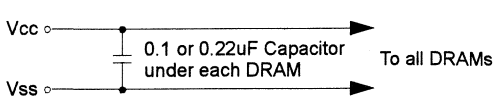
PD : 0 for Vol of Drive IC & 1 for N.C

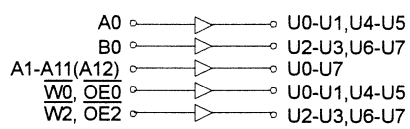
ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



Note : A12 is used for only KMM364C884BS (8K ref.)





ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM364C804BS		KMM364C884BS		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	580	-	460	mA
	-6	-	540	-	420	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	580	-	460	mA
	-6	-	540	-	420	mA
I_{CC4}	-5	-	380	-	340	mA
	-6	-	340	-	300	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	580	-	460	mA
	-6	-	540	-	420	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-10	10	-10	10	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	24	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	24	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.6/0.8V, V_{oh}/V_{ol}=2.4/0.4V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,11
Access time from column address	t_{AA}		25		30	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		ns	3,11
Output buffer turn-off delay	t_{OFF}	0	13	0	13	ns	6,11
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	11
$\overline{CAS}$ hold time	t_{CSH}	50		60		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	11
Row address set-up time	t_{ASR}	0		0		ns	11
Row address hold time	t_{RAH}	10		10		ns	11
Column address set-up time	t_{ASC}	0		0		ns	12
Column address hold time	t_{CAH}	10		10		ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	11
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referencde to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8,11
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	15
Data in set-up time	t_{DS}	0		0		ns	9,11
Data in hold time	t_{DH}	10		10		ns	9,11
Refresh period	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		38		ns	7,15
Column address to $\overline{W}$ delay time	t_{AWD}	48		53		ns	7
$\overline{CAS}$ prechange to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{RAS}$ ro $\overline{W}$ delay time	t_{RWD}	73		83		ns	7,11
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	11,16
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	11
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35	ns	3,11
Fast page mode cycle time	t_{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	76		85		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	13
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	11
$\overline{OE}$ access time	t_{OEA}		13		15	ns	11
$\overline{OE}$ to data delay	t_{OED}	13		13		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	13	ns	11
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

12. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.

13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

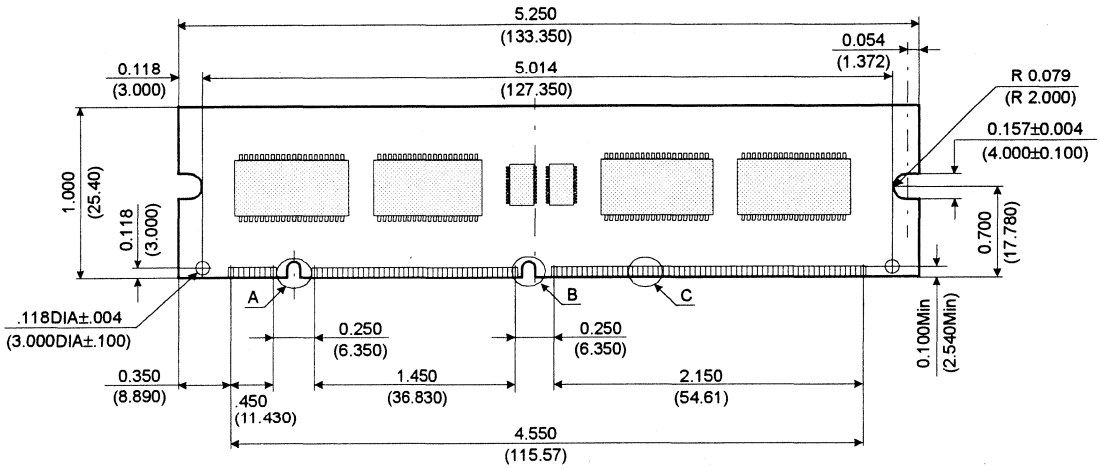
15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.

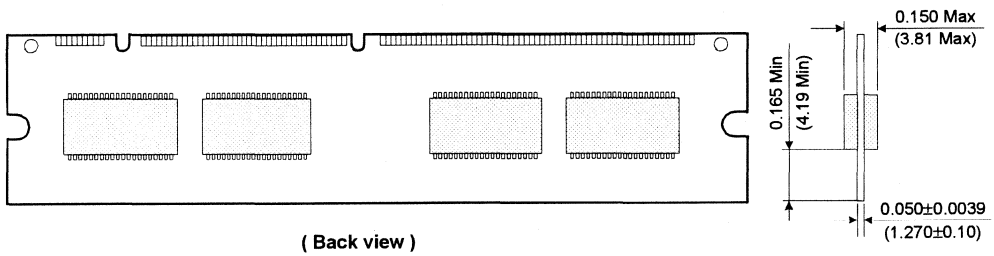
4

PACKAGE DIMENSIONS

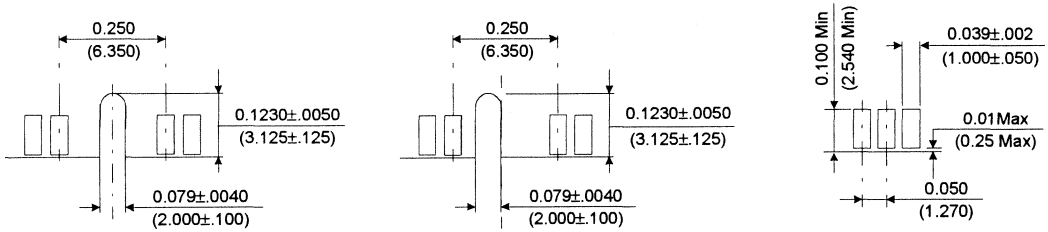
Units : Inches (millimeters)



(Front view)



(Back view)



Detail A **Detail B** **Detail C**

Tolerances :±.005(.13) unless otherwise specified

The used device is 4Mx16 DRAM with Fast page mode, TSOP II.
DRAM Part No. : KMM364C804BS - KM416C4100BS.
KMM364C884BS - KM416C4000BS.

KMM364E80(8)4BS EDO Mode

8M x 64 DRAM DIMM Using 4Mx16, 4K & 8K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM364E80(8)4B is a 4Mx64bits Dynamic RAM high density memory module. The Samsung KMM364E80(8)4B consists of eight CMOS 4Mx16bits DRAMs in TSOP-II 400mil packages and two 20 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM364E80(8)4B is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	18ns	84ns	20ns
-6	60ns	20ns	104ns	25ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM364E804BS	TSOPII	4K	4K/64ms	
KMM364E884BS	TSOPII	8K	4K/64ms	8K/64ms

- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS2}$	57	DQ22	85	Vss	113	$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	*DQ26	94	DQ43	122	A11	150	*DQ62
11	*DQ8	39	A12	67	DQ27	95	*DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	$\overline{CAS6}$	75	DQ33	103	DQ50	131	$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	*DQ35	105	DQ52	133	Vcc	161	*DQ71
22	*DQ17	50	RSVD	78	Vss	106	*DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	$\overline{RFU}$	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM364E884BS (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a resistor to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
A0, B0, A1 - A12	Address Input(8K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

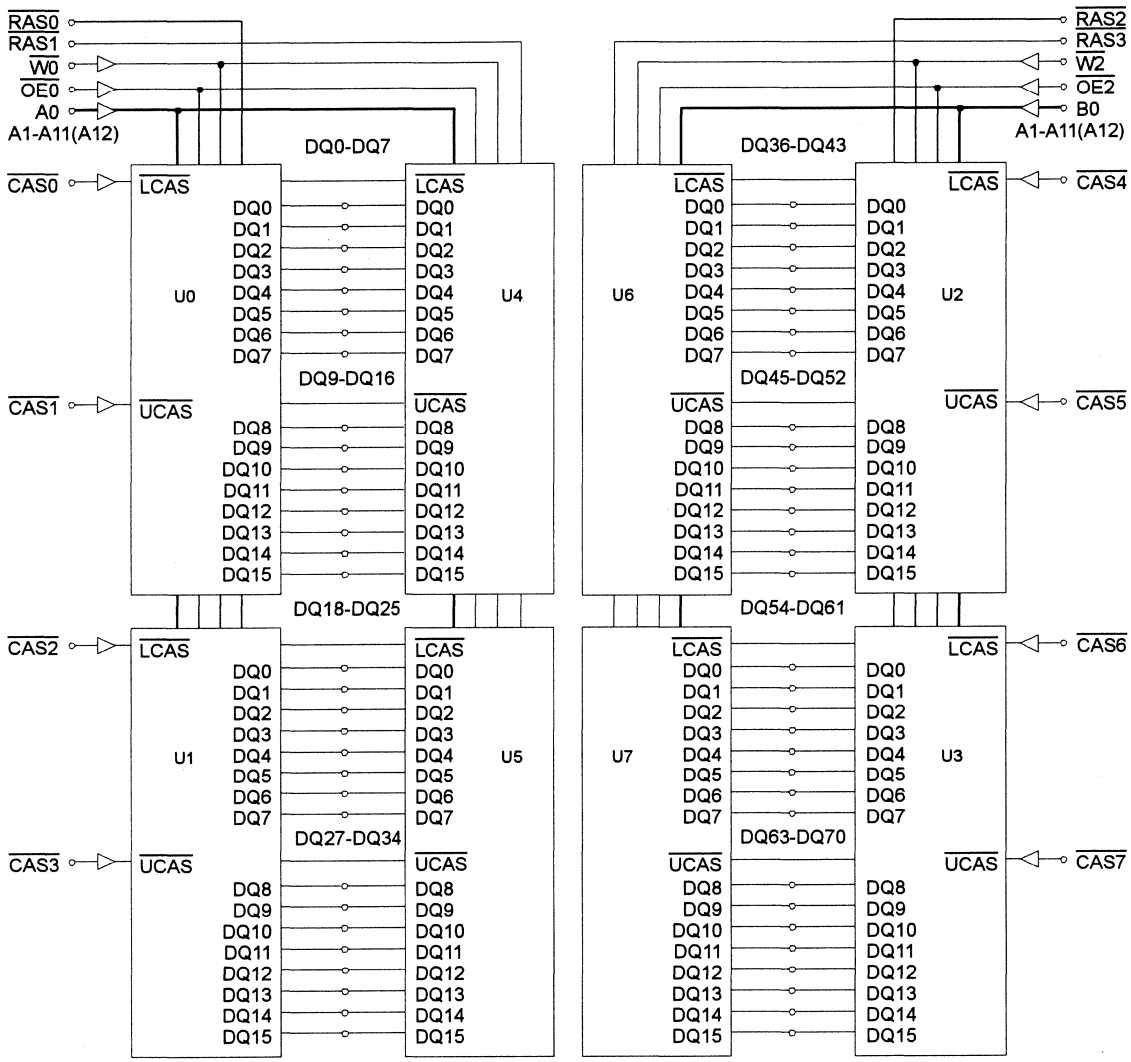
PD & ID Table

Pin	50NS	60NS
PD1	0	0
PD2	0	0
PD3	1	1
PD4	1	1
PD5	1	1
PD6	0	1
PD7	0	1
PD8	1	1
ID0	0	0
ID1	0	0

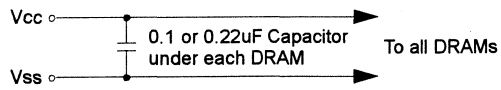
PD : 0 for Vol of Drive IC & 1 for N.C

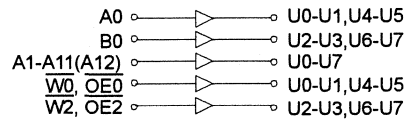
ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



Note : A12 is used for only KMM364E884BS (8K ref.)





ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM364E804BS		KMM364E884BS		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	580	-	460	mA
	-6	-	540	-	420	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	580	-	460	mA
	-6	-	540	-	420	mA
I_{CC4}	-5	-	540	-	500	mA
	-6	-	500	-	460	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	580	-	460	mA
	-6	-	540	-	420	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-10	10	-10	10	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	24	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	24	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.6/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,13
Access time from column address	t_{AA}		30		35	ns	3,10,13
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,13
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,13
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	18	ns	6,11,13
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	13
$\overline{CAS}$ hold time	t_{CSH}	36		43		ns	13
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,13
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	13
Row address set-up time	t_{ASR}	5		5		ns	13
Row address hold time	t_{RAH}	8		8		ns	13
Column address set-up time	t_{ASC}	0		0		ns	14
Column address hold time	t_{CAH}	8		10		ns	14
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	13
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,13
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	18		20		ns	13
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	17
Data set-up time	t_{DS}	-2		-2		ns	9,13
Data hold time	t_{DH}	13		15		ns	9,13
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		38		ns	7,16
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		83		ns	7,13

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	48		53		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	13,18
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	13
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,13
Hyper page cycle time	t_{HPC}	20		25		ns	12
Hyper page read-modify-write cycle time	t_{HPRWC}	70		77		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	8		10		ns	15
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	13
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	13
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	13
$\overline{OE}$ access time	t_{OEA}		18		20	ns	13
$\overline{OE}$ to data delay	t_{OED}	18		18		ns	13
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	8	18	8	18	ns	13
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Output data hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{DOH}	10		10		ns	13
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	15	3	15	ns	6,11
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	8	18	8	20	ns	6,13
$\overline{W}$ to data delay	t_{WED}	20		20		ns	13
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

12. $t_{ASC} \geq 6$ns.

13. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

14. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.

15. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

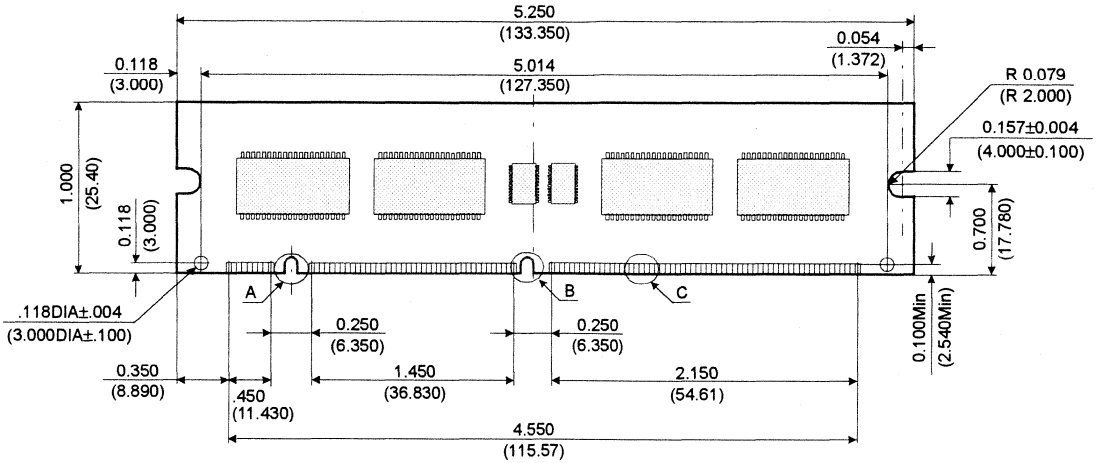
16. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

17. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

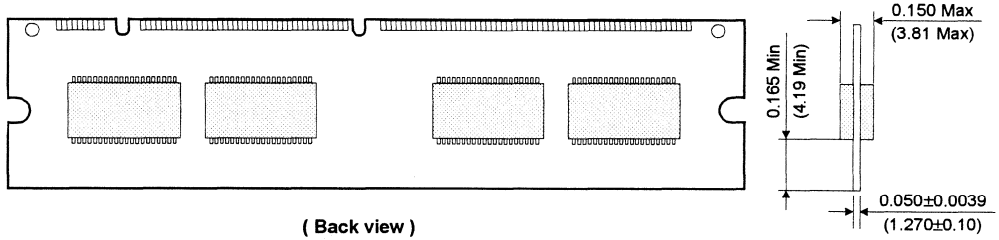
18. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.

PACKAGE DIMENSIONS

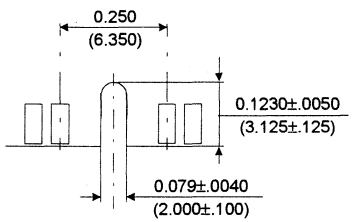
Units : Inches (millimeters)



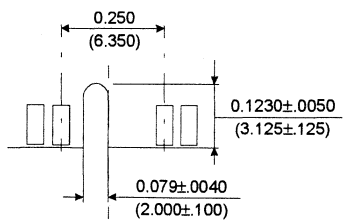
(Front view)



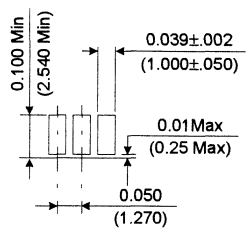
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 DRAM with EDO mode, TSOP II.
DRAM Part No. : KMM364E804BS - KM416C4104BS.
KMM364E884BS - KM416C4004BS.

KMM372C80(8)3BK/BS Fast Page Mode

8Mx72 DRAM DIMM with ECC Using 8Mx8, 4K & 8K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM372C80(8)3B is a 8Mx72bits Dynamic RAM high density memory module. The Samsung KMM372C80(8)3B consists of nine CMOS 8Mx8bits DRAMs in SOJ/TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372C80(8)3B is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	18ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

FEATURES

• Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM372C803BK	SOJ	4K	4K/64ms	
KMM372C803BS	TSOP			
KMM372C883BK	SOJ	8K	4K/64ms	8K/64ms
KMM372C883BS	TSOP			

- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1250mil), single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	*$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	$\overline{RFU}$	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	*$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM372C883BK/BS (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a resistor to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
A0, B0, A1 - A12	Address Input(8K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

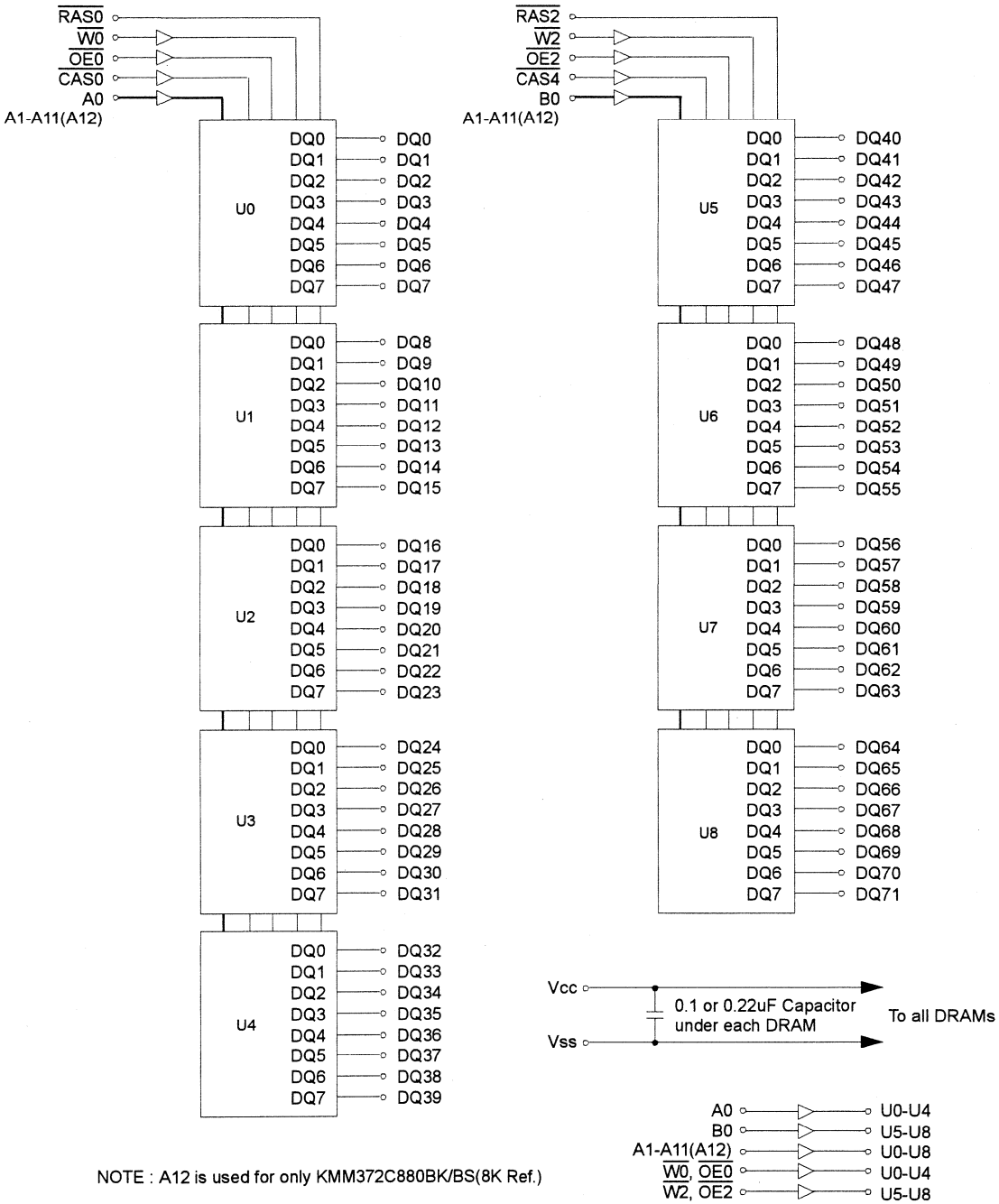
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	1	1
PD4	1	1
PD5	0	0
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM372C880BK/BS(8K Ref.)

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	9	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372C803BK/BS		KMM372C883BK/BS		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	1080	-	810	mA
	-6	--	990	-	720	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	1080	-	810	mA
	-6	-	990	-	720	mA
I_{CC4}	-5	-	630	-	540	mA
	-6	-	540	-	450	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	1080	-	810	mA
	-6	-	990	-	720	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	45	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS4}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,11
Access time from column address	t_{AA}		30		35	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,11
Output buffer turn-off delay	t_{OFF}	5	18	5	20	ns	6,11
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	11
$\overline{CAS}$ hold time	t_{CSH}	45		55		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	11
Row address set-up time	t_{ASR}	5		5		ns	11
Row address hold time	t_{RAH}	8		8		ns	11
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	11
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referencde to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,11
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data in set-up time	t_{DS}	-2		-2		ns	9,11
Data in hold time	t_{DH}	15		15		ns	9,11
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ prechange to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7
$\overline{RAS}$ ro $\overline{W}$ delay time	t_{RWD}	73		85		ns	7,11

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	11
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	11
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3,11
Fast page mode cycle time	t_{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	76		85		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	11
$\overline{OE}$ access time	t_{OEA}		18		20	ns	11
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	11
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

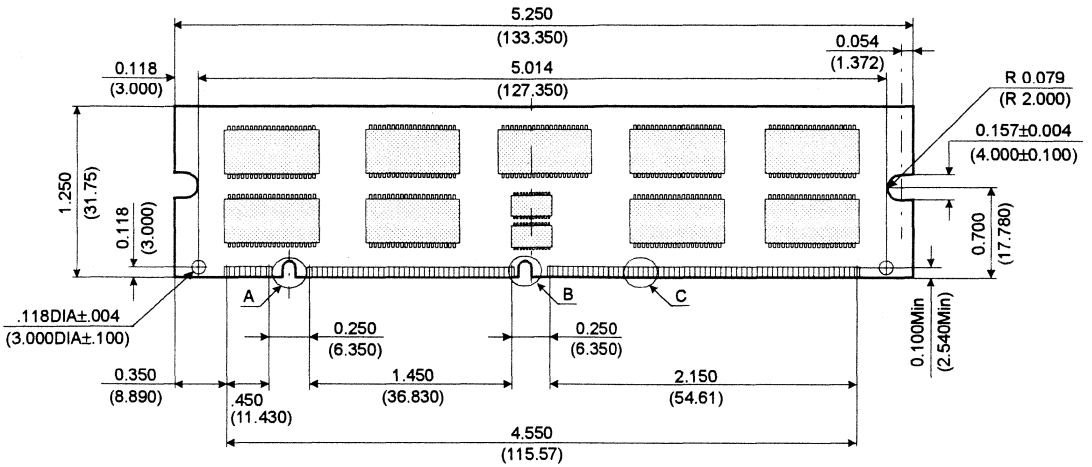
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

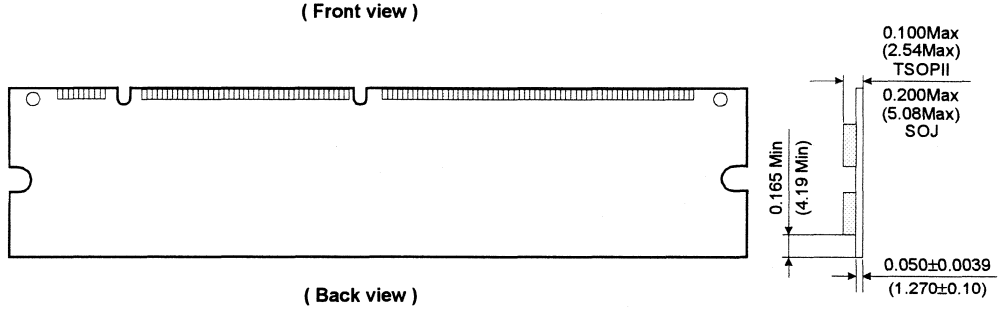
11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

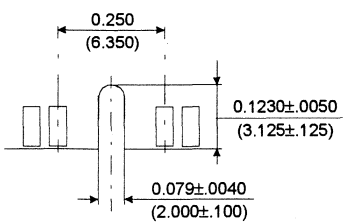
Units : Inches (millimeters)



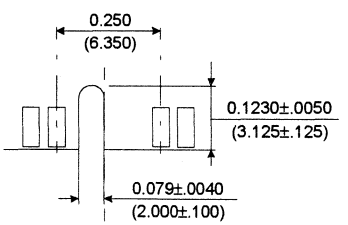
(Front view)



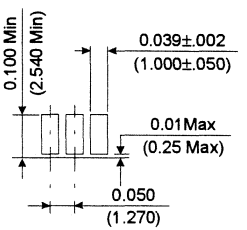
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 DRAM with Fast Page mode, SOJ or TSOP II.
DRAM Part No. : KMM372C803BK/BS - KM48C8100BK, KM48C8100BS.
KMM372C883BK/BS - KM48C8000BK, KM48C8000BS.

KMM372E80(8)3BK/BS EDO Mode

8M x 72 DRAM DIMM with ECC Using 8Mx8, 4K & 8K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM372E80(8)3B is a 8Mx72bits Dynamic RAM high density memory module. The Samsung KMM372E80(8)3B consists of nine CMOS 8Mx8bits DRAMs in SOJ/TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372E80(8)3B is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	18ns	84ns	20ns
-6	60ns	20ns	104ns	25ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM372E803BK	SOJ	4K	4K/64ms	
KMM372E803BS	TSOP			
KMM372E883BK	SOJ	8K	4K/64ms	8K/64ms
KMM372E883BS	TSOP			

- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1250mil), single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	*$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	*$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM372E883BK/BS (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a resistor to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
A0, B0, A1 - A12	Address Input(8K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

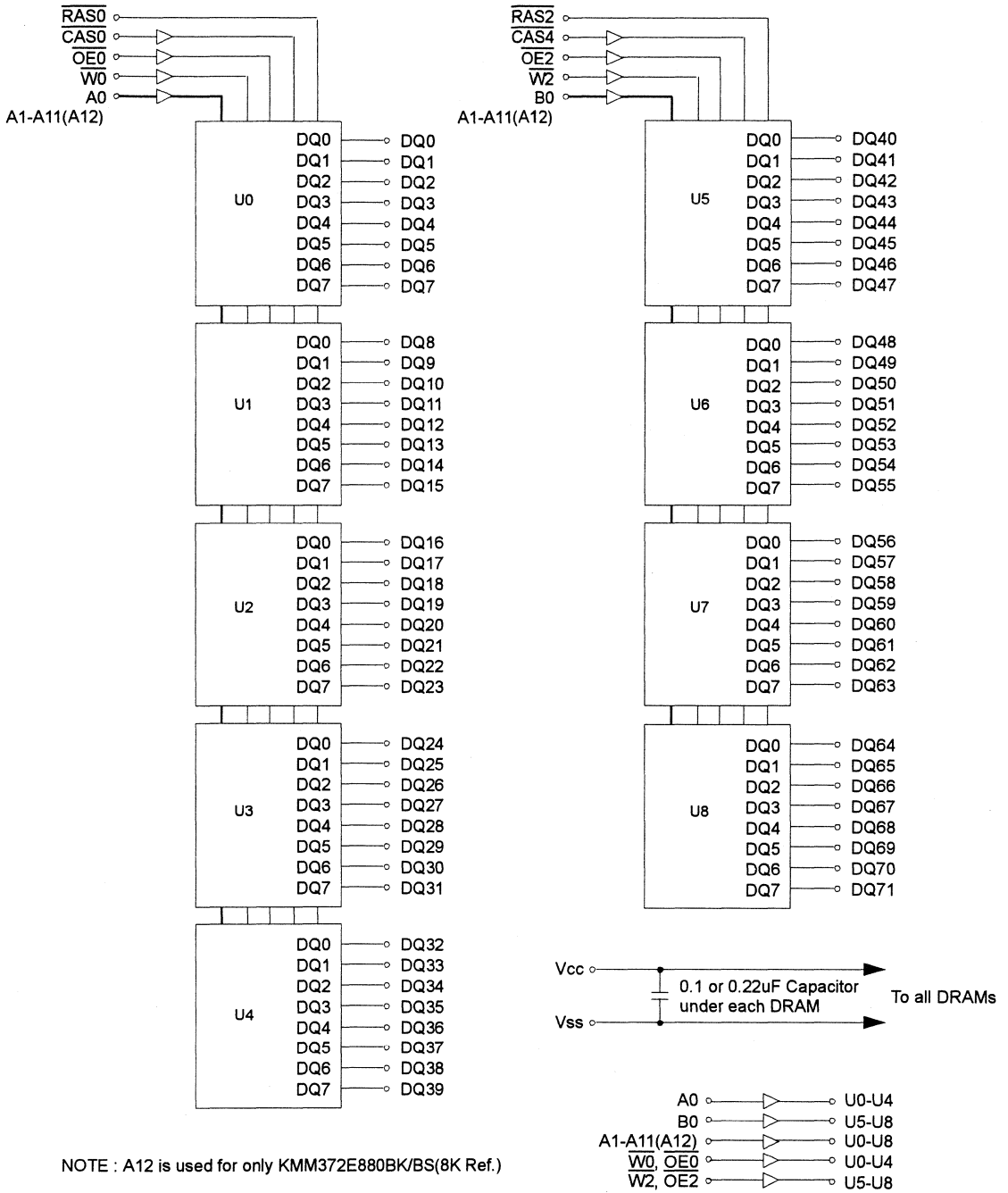
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	1	1
PD4	1	1
PD5	1	1
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM372E880BK/BS(8K Ref.)

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	9	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : V_{CC}+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372E803BK/BS		KMM372E883BK/BS		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	1080	-	810	mA
	-6	--	990	-	720	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	1080	-	810	mA
	-6	-	990	-	720	mA
I_{CC4}	-5	-	990	-	900	mA
	-6	-	900	-	810	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	1080	-	810	mA
	-6	-	990	-	720	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}¡ÂVcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	45	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS4}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,13
Access time from column address	t_{AA}		30		35	ns	3,10,13
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,13
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,13
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	18	ns	6,11,13
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	13
$\overline{CAS}$ hold time	t_{CSH}	36		43		ns	13
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,13
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	13
Row address set-up time	t_{ASR}	5		5		ns	13
Row address hold time	t_{RAH}	8		8		ns	13
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	13
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,13
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	18		20		ns	13
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,13
Data hold time	t_{DH}	13		15		ns	9,13
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		38		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		83		ns	7,13

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	48		53		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	13
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	13
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,13
Hyper page cycle time	t_{HPC}	20		25		ns	12
Hyper page read-modify-write cycle time	t_{HPRWC}	70		77		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	13
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	13
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	13
$\overline{OE}$ access time	t_{OEA}		18		20	ns	13
$\overline{OE}$ to data delay	t_{OED}	18		18		ns	13
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	8	18	8	18	ns	13
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Output data hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{DOH}	10		10		ns	13
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	15	3	15	ns	6,11
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	8	18	8	20	ns	6,13
$\overline{W}$ to data delay	t_{WED}	20		20		ns	13
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{IH}/V_{IL}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

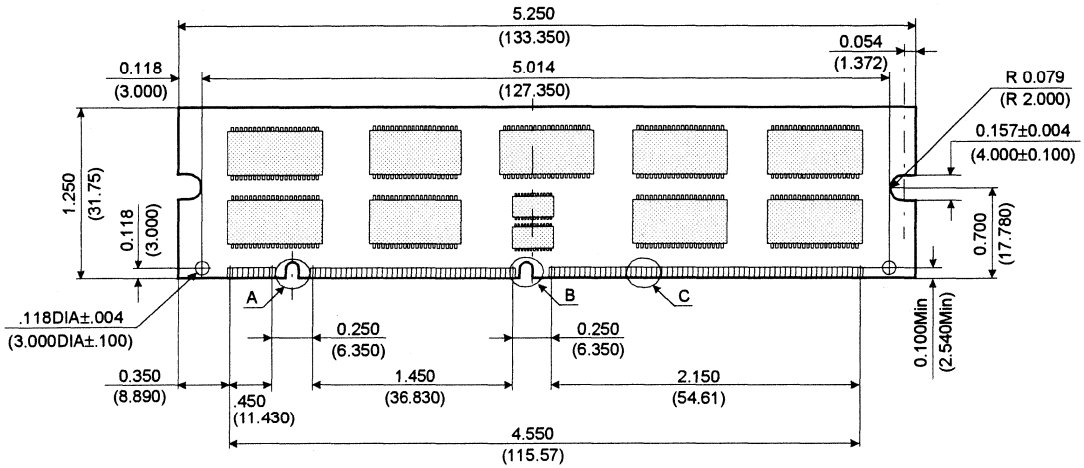
12. $t_{ASC} \geq 6$ns.

13. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

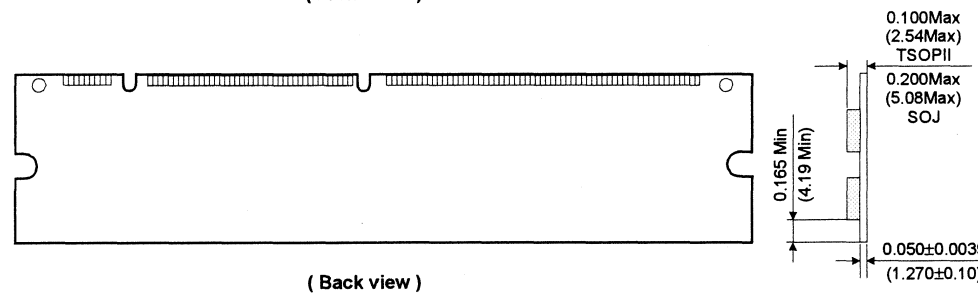
4

PACKAGE DIMENSIONS

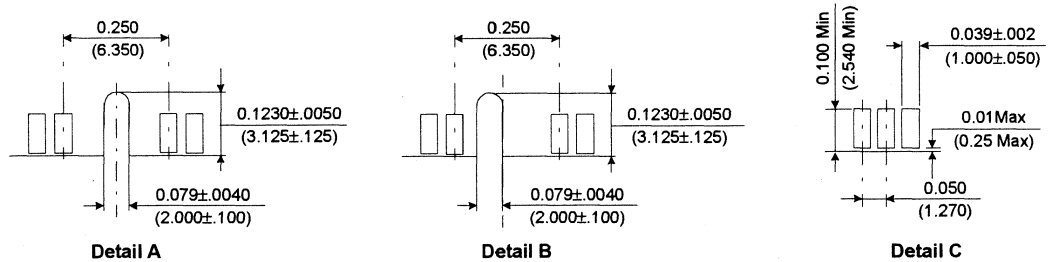
Units : Inches (millimeters)



(Front view)



(Back view)



Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 DRAM with EDO mode, SOJ or TSOP II.
DRAM Part No. : KMM372E803BK/BS - KM48C8104BK, KM48C8104BS.
KMM372E883BK/BS - KM48C8004BK, KM48C8004BS.

KMM372C804BS Fast Page Mode

8M x 72 DRAM DIMM with ECC Using 4Mx16 & 4Mx4, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM372C804B is a 8Mx72bits Dynamic RAM high density memory module. The Samsung KMM372C804B consists of eight 4Mx16bits & four 4Mx4bits CMOS DRAMs in TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372C804B is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	18ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

FEATURES

- Part Identification
  - KMM372C804BS(4096cycles/64ms Ref. TSOP II)
- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

PD Note :PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$, 1,4,5	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

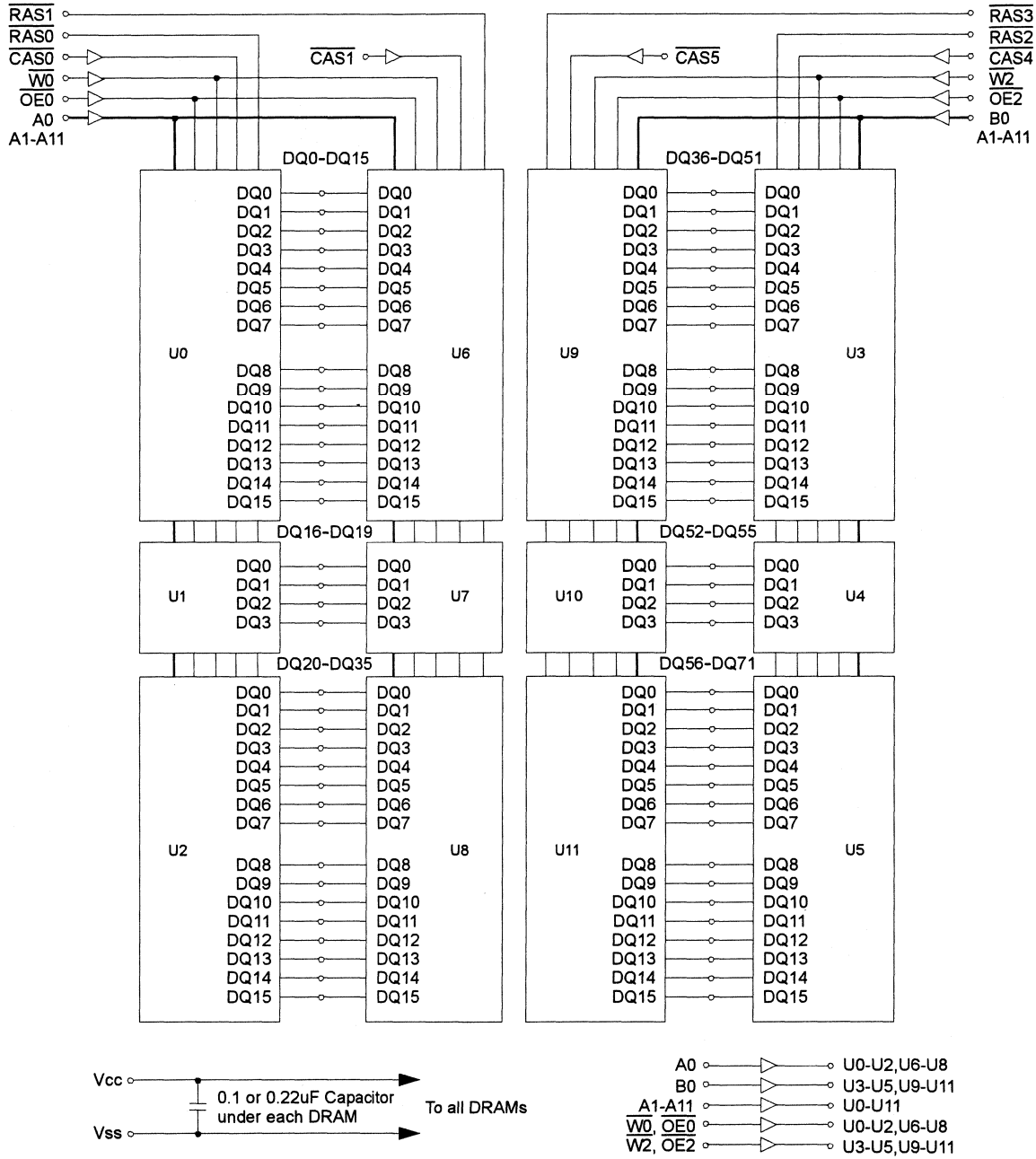
PD & ID Table

Pin	50NS	60NS
PD1	0	0
PD2	0	0
PD3	1	1
PD4	1	1
PD5	0	0
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	12	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372C804BS		Unit
		Min	Max	
I_{CC1}	-5	-	760	mA
	-6	-	700	mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-5	-	760	mA
	-6	-	700	mA
I_{CC4}	-5	-	540	mA
	-6	-	480	mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-5	-	760	mA
	-6	-	700	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-10	10	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast Page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A11]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	31	pF
Input capacitance[$\overline{CAS0}$, 1,4,5]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	24	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.6/0.8V, V_{oh}/V_{ol}=2.4/0.4V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,11
Access time from column address	t_{AA}		30		35	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,11
Output buffer turn-off delay	t_{OFF}	5	18	5	20	ns	6,11
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	11
$\overline{CAS}$ hold time	t_{CSH}	45		55		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	11
Row address set-up time	t_{ASR}	5		5		ns	11
Row address hold time	t_{RAH}	8		8		ns	11
Column address set-up time	t_{ASC}	0		0		ns	12
Column address hold time	t_{CAH}	10		10		ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	11
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referencde to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,11
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	15
Data in set-up time	t_{DS}	-2		-2		ns	9,11
Data in hold time	t_{DH}	15		15		ns	9,11
Refresh period	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7,15
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ prechange to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{RAS}$ ro $\overline{W}$ delay time	t_{RWD}	73		85		ns	7,11
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	11,16
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	11
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3,11
Fast page mode cycle time	t_{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	76		85		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	13
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	11
$\overline{OE}$ access time	t_{OEA}		18		20	ns	11
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	11
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

12. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.

13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

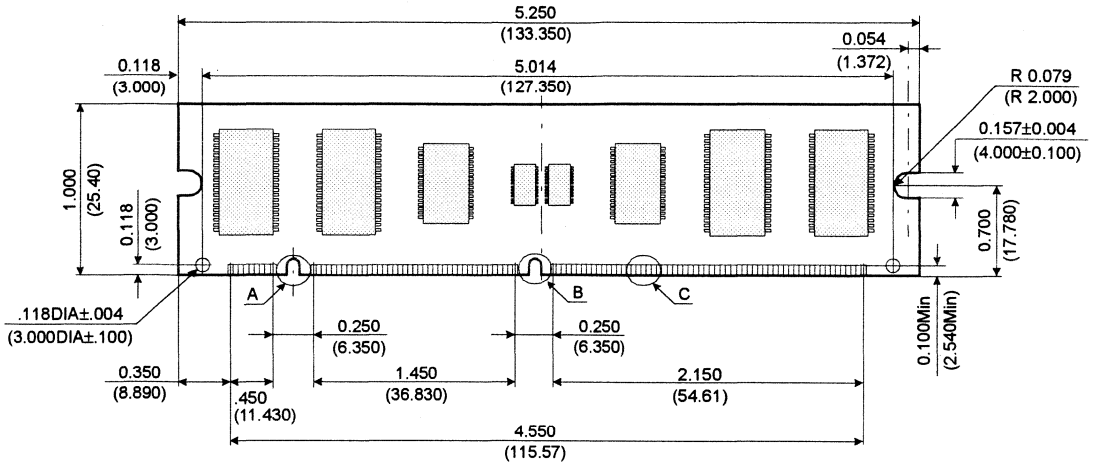
14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

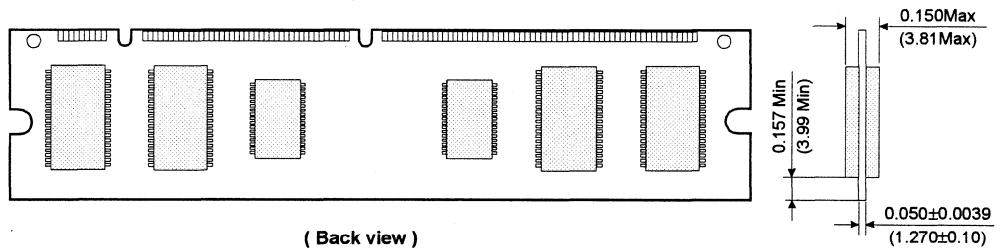
16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.

PACKAGE DIMENSIONS

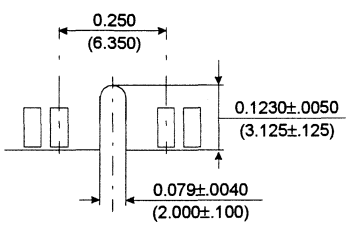
Units : Inches (millimeters)



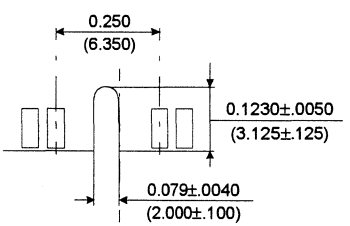
(Front view)



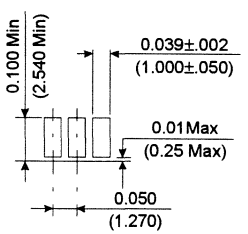
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 & 4Mx4 DRAM with Fast Page mode, TSOP II.
DRAM Part No. : KMM372C804BS -KM416C4100BS & KM44C4000CS

KMM372E804BS EDO Mode

8M x 72 DRAM DIMM with ECC Using 4Mx16 & 4Mx4, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM372E804B is a 8Mx72bits Dynamic RAM high density memory module. The Samsung KMM372E804B consists of eight 4Mx16bits & four 4Mx4bits CMOS DRAMs in TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372E804B is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	18ns	84ns	20ns
-6	60ns	20ns	104ns	25ns

FEATURES

- Part Identification
  - KMM372E804BS(4096cycles/64ms Ref. TSOP II)
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

PD Note :PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$, 1,4,5	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

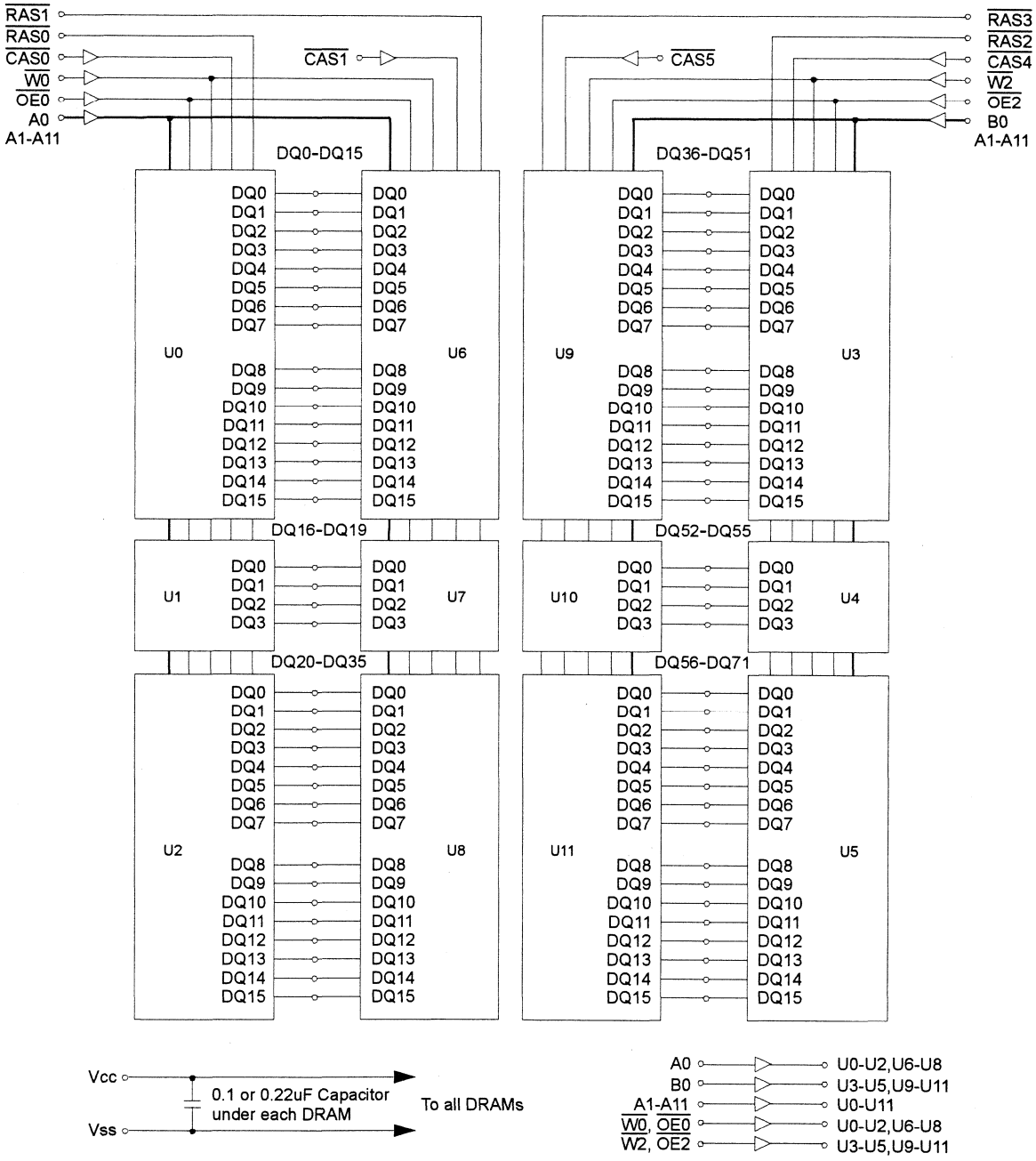
PD & ID Table

Pin	50NS	60NS
PD1	0	0
PD2	0	0
PD3	1	1
PD4	1	1
PD5	1	1
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	12	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372E804BS		Unit
		Min	Max	
I_{CC1}	-5	-	760	mA
	-6	-	700	mA
I_{CC2}	Don't care	-	100	mA
I_{CC3}	-5	-	760	mA
	-6	-	700	mA
I_{CC4}	-5	-	700	mA
	-6	-	640	mA
I_{CC5}	Don't care	-	30	mA
I_{CC6}	-5	-	760	mA
	-6	-	700	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-10	10	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A11]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	31	pF
Input capacitance[$\overline{CAS0}$, 1,4,5]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	24	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.6/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,13
Access time from column address	t_{AA}		30		35	ns	3,10,13
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,13
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,13
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	18	ns	6,11,13
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	13
$\overline{CAS}$ hold time	t_{CSH}	36		43		ns	13
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,13
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	13
Row address set-up time	t_{ASR}	5		5		ns	13
Row address hold time	t_{RAH}	8		8		ns	13
Column address set-up time	t_{ASC}	0		0		ns	14
Column address hold time	t_{CAH}	8		10		ns	14
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	13
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,13
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	18		20		ns	13
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	17
Data set-up time	t_{DS}	-2		-2		ns	9,13
Data hold time	t_{DH}	13		15		ns	9,13
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		38		ns	7,16
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		83		ns	7,13

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	48		53		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	13,18
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	13
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,13
Hyper page cycle time	t_{HPC}	20		25		ns	12
Hyper page read-modify-write cycle time	t_{HPRWC}	70		77		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	8		10		ns	15
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	13
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	13
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	13
$\overline{OE}$ access time	t_{OEA}		18		20	ns	13
$\overline{OE}$ to data delay	t_{OED}	18		18		ns	13
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	8	18	8	18	ns	13
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Output data hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{DOH}	10		10		ns	13
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	15	3	15	ns	6,11
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	8	18	8	20	ns	6,13
$\overline{W}$ to data delay	t_{WED}	20		20		ns	13
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If t_{RWD}¡Ät$_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

12. $t_{ASC} \geq 6$ns.

13. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

14. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.

15. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

16. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

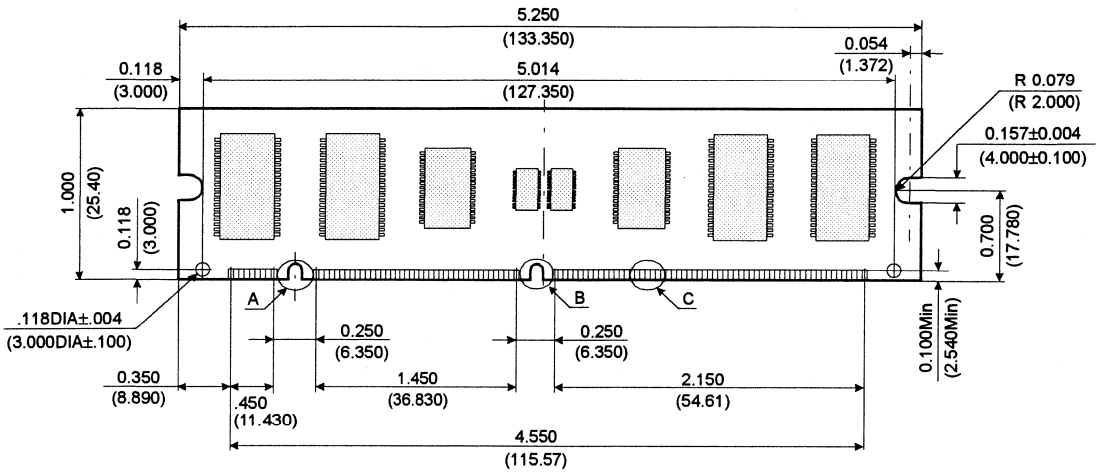
17. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

18. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.

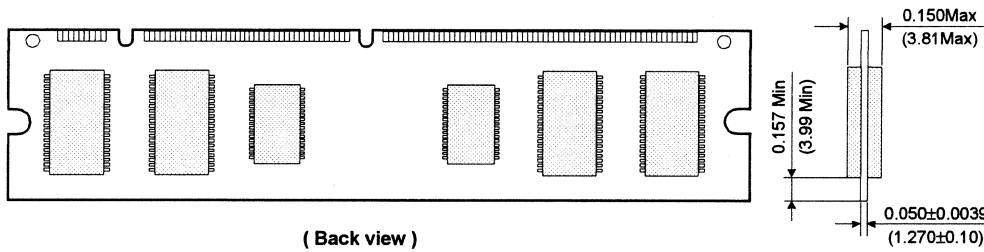
4

PACKAGE DIMENSIONS

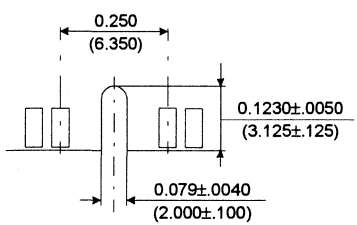
Units : Inches (millimeters)



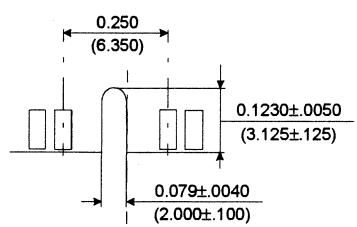
(Front view)



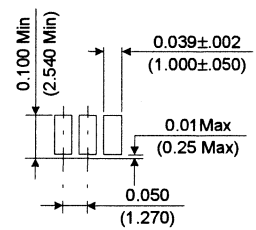
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 & 4Mx4 DRAM with EDO mode, TSOP II.
DRAM Part No. : KMM372E804BS -KM416C4104BS & KM44C4004CS

KMM364C160(8)0BK/BS Fast Page Mode
16M x 64 DRAM DIMM Using 16Mx4, 4K & 8K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM364C160(8)0B is a 16Mx64bits Dynamic RAM high density memory module. The Samsung KMM364C160(8)0B consists of sixteen CMOS 16Mx4bits DRAMs in SOJ/TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM364C160(8)0B is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	18ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM364C1600BK	SOJ	4K	4K/64ms	
KMM364C1600BS	TSOP			
KMM364C1680BK	SOJ	8K	4K/64ms	8K/64ms
KMM364C1680BS	TSOP			

- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1250mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS2}$	57	DQ22	85	Vss	113	$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	*DQ26	94	DQ43	122	A11	150	*DQ62
11	*DQ8	39	A12	67	DQ27	95	*DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	$\overline{CAS6}$	75	DQ33	103	DQ50	131	$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	*DQ35	105	DQ52	133	Vcc	161	*DQ71
22	*DQ17	50	RSVD	78	Vss	106	*DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM364C1680BK/BS (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a resistor to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
A0, B0, A1 - A12	Address Input(8K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

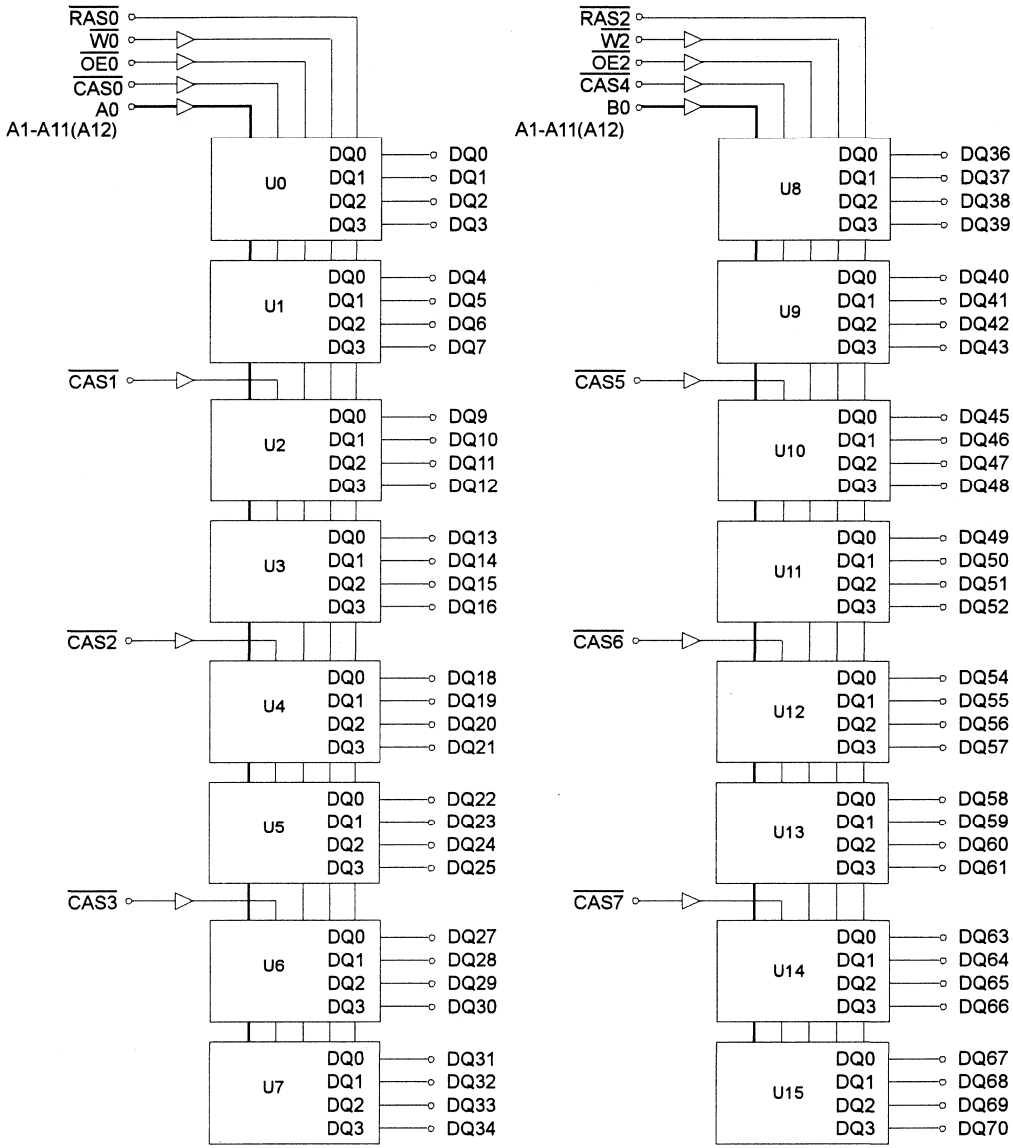
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	1	1
PD3	1	1
PD4	1	1
PD5	0	0
PD6	0	1
PD7	0	1
PD8	1	1
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM364C1680BK/BS(8K Ref.)

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	16	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM364C1600BK/BS		KMM364C1680BK/BS		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	1920	-	1440	mA
	-6	-	1760	-	1280	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	1920	-	1440	mA
	-6	-	1760	-	1280	mA
I_{CC4}	-5	-	1120	-	960	mA
	-6	-	960	-	800	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	1920	-	1920	mA
	-6	-	1760	-	1760	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C , f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	66	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	17	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,11
Access time from column address	t_{AA}		30		35	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,11
Output buffer turn-off delay	t_{OFF}	5	18	5	20	ns	6,11
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	11
$\overline{CAS}$ hold time	t_{CSH}	45		55		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	11
Row address set-up time	t_{ASR}	5		5		ns	11
Row address hold time	t_{RAH}	8		8		ns	11
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	11
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referencde to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,11
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data in set-up time	t_{DS}	-2		-2		ns	9,11
Data in hold time	t_{DH}	15		15		ns	9,11
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ prechange to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7
$\overline{RAS}$ ro $\overline{W}$ delay time	t_{RWD}	73		85		ns	7,11

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	11
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	11
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3,11
Fast page mode cycle time	t_{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	76		85		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	11
$\overline{OE}$ access time	t_{OEA}		18		20	ns	11
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	11
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

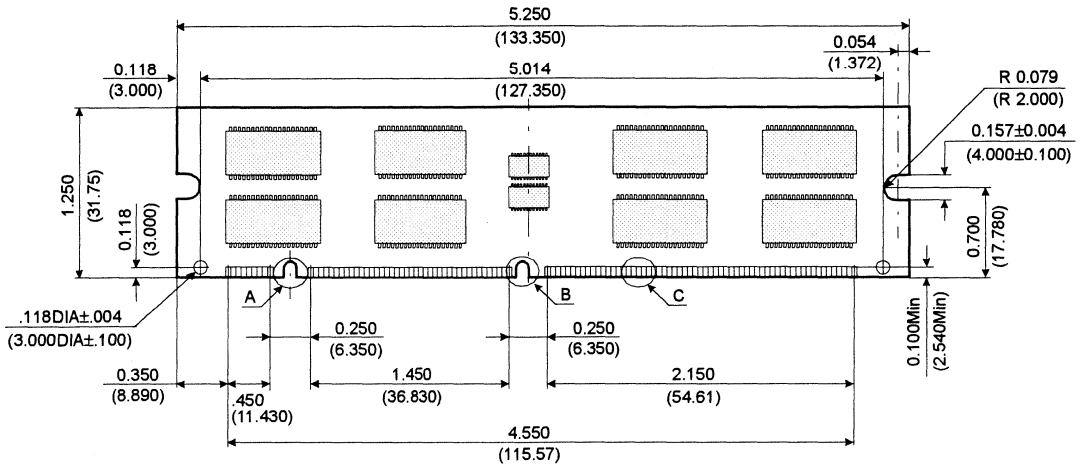
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

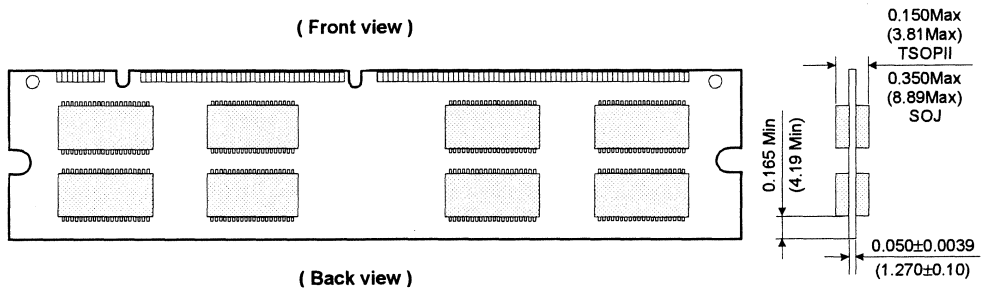
11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

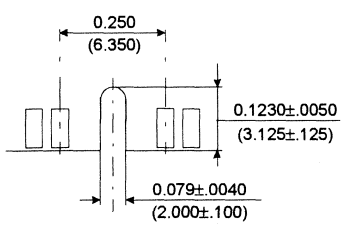
Units : Inches (millimeters)



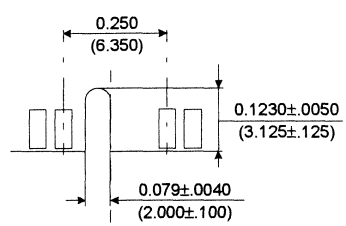
(Front view)



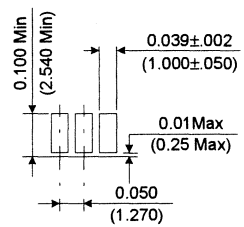
(Back view)



Detail A



Detail B



Detail C

Tolerances :±.005(.13) unless otherwise specified

The used device is 16Mx4 DRAM with Fast Page mode, SOJ or TSOPII.
DRAM Part No. : KMM364C1600BK/BS - KM44C16100BK, KM44C16100BS.
KMM364C1680BK/BS - KM44C16000BK, KM44C16000BS.

KMM364E160(8)0BK/BS EDO Mode

16M x 64 DRAM DIMM Using 16Mx4, 4K & 8K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM364E160(8)0B is a 16Mx64bits Dynamic RAM high density memory module. The Samsung KMM364E160(8)0B consists of sixteen CMOS 16Mx4bits DRAMs in SOJ/TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM364E160(8)0B is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	18ns	84ns	20ns
-6	60ns	20ns	104ns	25ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM364E1600BK	SOJ	4K	4K/64ms	
KMM364E1600BS	TSOP			
KMM364E1680BK	SOJ	8K	4K/64ms	8K/64ms
KMM364E1680BS	TSOP			

- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1250mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS2}$	57	DQ22	85	Vss	113	$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	*DQ26	94	DQ43	122	A11	150	*DQ62
11	*DQ8	39	A12	67	DQ27	95	*DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	$\overline{CAS6}$	75	DQ33	103	DQ50	131	$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	*DQ35	105	DQ52	133	Vcc	161	*DQ71
22	*DQ17	50	RSVD	78	Vss	106	*DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	$\overline{RFU}$	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM364E1680BK/BS (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a resistor to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
A0, B0, A1 - A12	Address Input(8K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

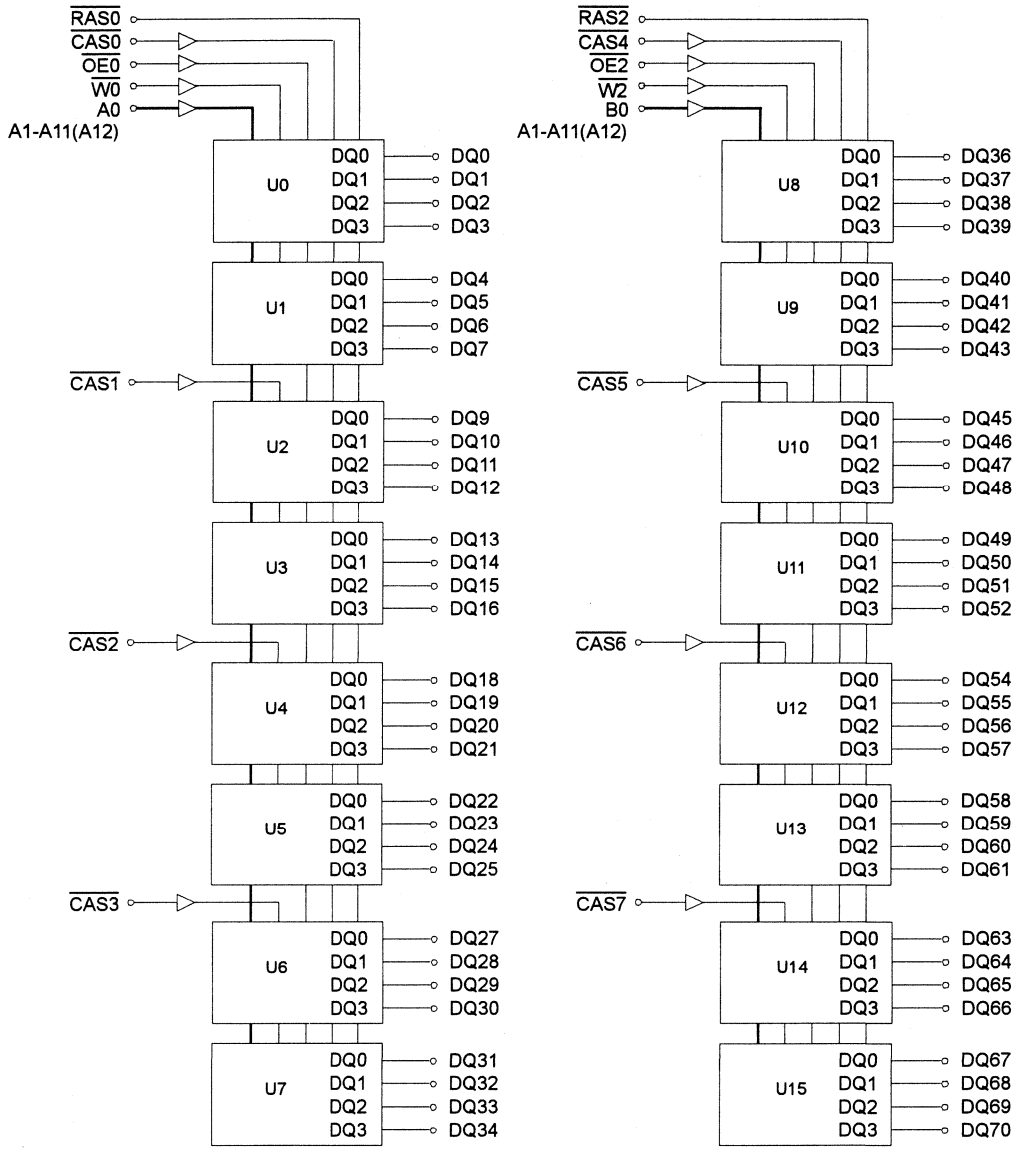
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	1	1
PD3	1	1
PD4	1	1
PD5	1	1
PD6	0	1
PD7	0	1
PD8	1	1
ID0	0	0
ID1	0	0

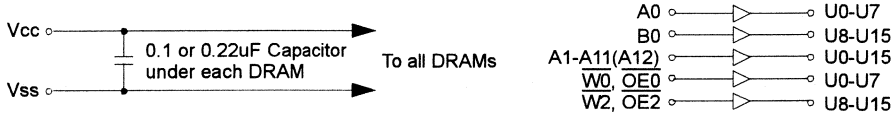
PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM364E1680BK/BS(8K Ref.)



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	16	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM364E1600AK/BS		KMM364E1680AK/BS		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	1920	-	1440	mA
	-6	-	1760	-	1280	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	1920	-	1440	mA
	-6	-	1760	-	1280	mA
I_{CC4}	-5	-	1760	-	1600	mA
	-6	-	1600	-	1440	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	1920	-	1440	mA
	-6	-	1760	-	1280	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OU}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	66	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,13
Access time from column address	t_{AA}		30		35	ns	3,10,13
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,13
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,13
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	18	ns	6,11,13
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	13
$\overline{CAS}$ hold time	t_{CSH}	36		43		ns	13
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,13
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	13
Row address set-up time	t_{ASR}	5		5		ns	13
Row address hold time	t_{RAH}	8		8		ns	13
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	13
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,13
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	18		20		ns	13
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,13
Data hold time	t_{DH}	13		15		ns	9,13
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		38		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		83		ns	7,13

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	48		53		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	13
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	13
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,13
Hyper page cycle time	t_{HPC}	20		25		ns	12
Hyper page read-modify-write cycle time	t_{HPRWC}	70		77		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	13
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	13
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	13
$\overline{OE}$ access time	t_{OEA}		18		20	ns	13
$\overline{OE}$ to data delay	t_{OED}	18		18		ns	13
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	8	18	8	18	ns	13
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Output data hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{DOH}	10		10		ns	13
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	15	3	15	ns	6,11
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	8	18	8	20	ns	6,13
$\overline{W}$ to data delay	t_{WED}	20		20		ns	13
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{IH}/V_{IL}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

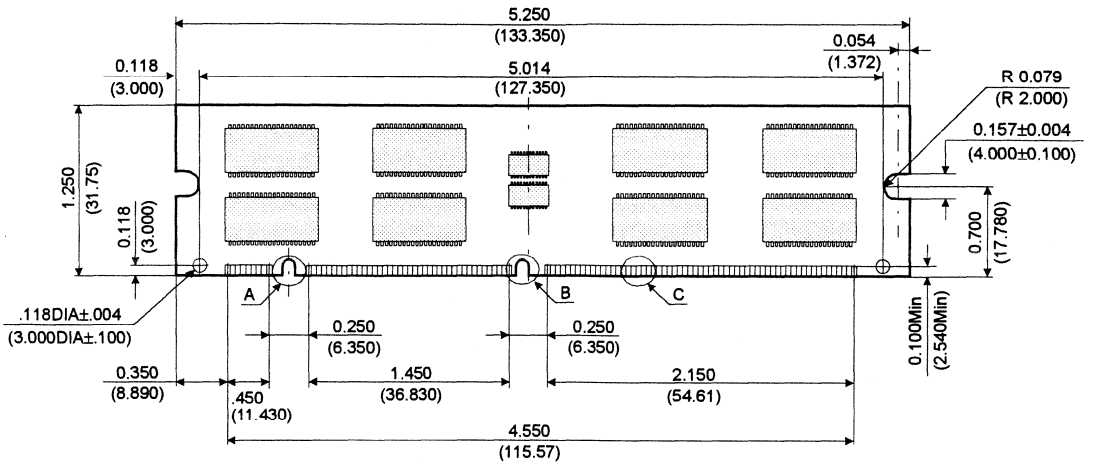
11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

12. $t_{ASC} \geq 6$ns.

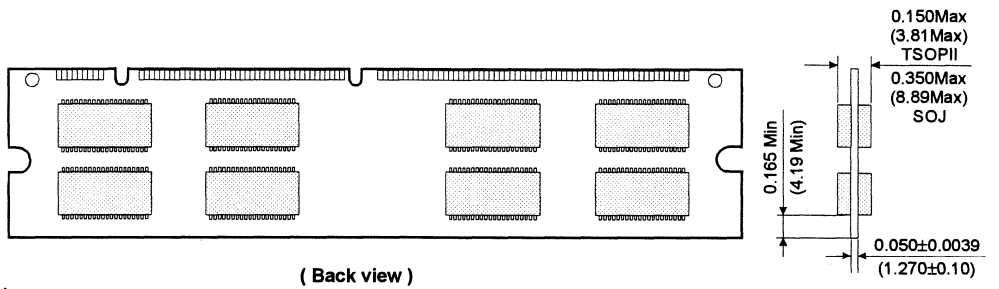
13. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

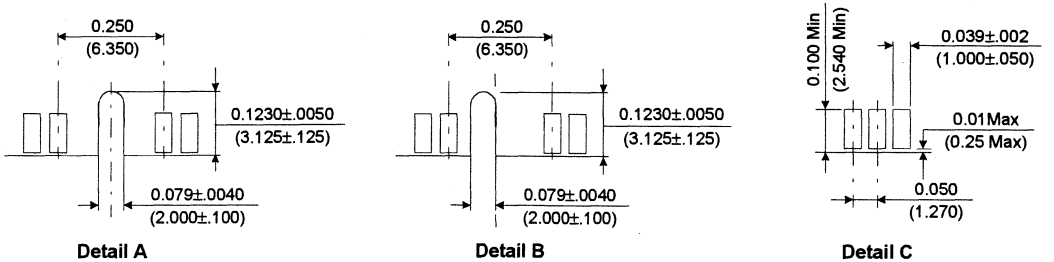
Units : Inches (millimeters)



(Front view)



(Back view)



Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx4 DRAM with EDO mode, SOJ or TSOPII.
DRAM Part No. : KMM364E1600BK/BS - KM44C16104BK, KM44C16104BS.
KMM364E1680BK/BS - KM44C16004BK, KM44C16004BS.

KMM372C160(8)0BK/BS Fast Page Mode

16M x 72 DRAM DIMM with ECC Using 16Mx4, 4K & 8K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM372C160(8)0B is a 16Mx72bits Dynamic RAM high density memory module. The Samsung KMM372C160(8)0B consists of eighteen CMOS 16Mx4bits DRAMs in SOJ/TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372C160(8)0B is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	18ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

FEATURES

• Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM372C1600BK	SOJ	4K	4K/64ms	
KMM372C1600BS	TSOP			
KMM372C1680BK	SOJ	8K	4K/64ms	8K/64ms
KMM372C1680BS	TSOP			

- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1250mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	RSVD
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	*$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	RSVD	105	DQ52	133	Vcc	161	DQ71
22	RSVD	50	RSVD	78	Vss	106	RSVD	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	*$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM372C1680BK/BS (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a resistor to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
A0, B0, A1 - A12	Address Input(8K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

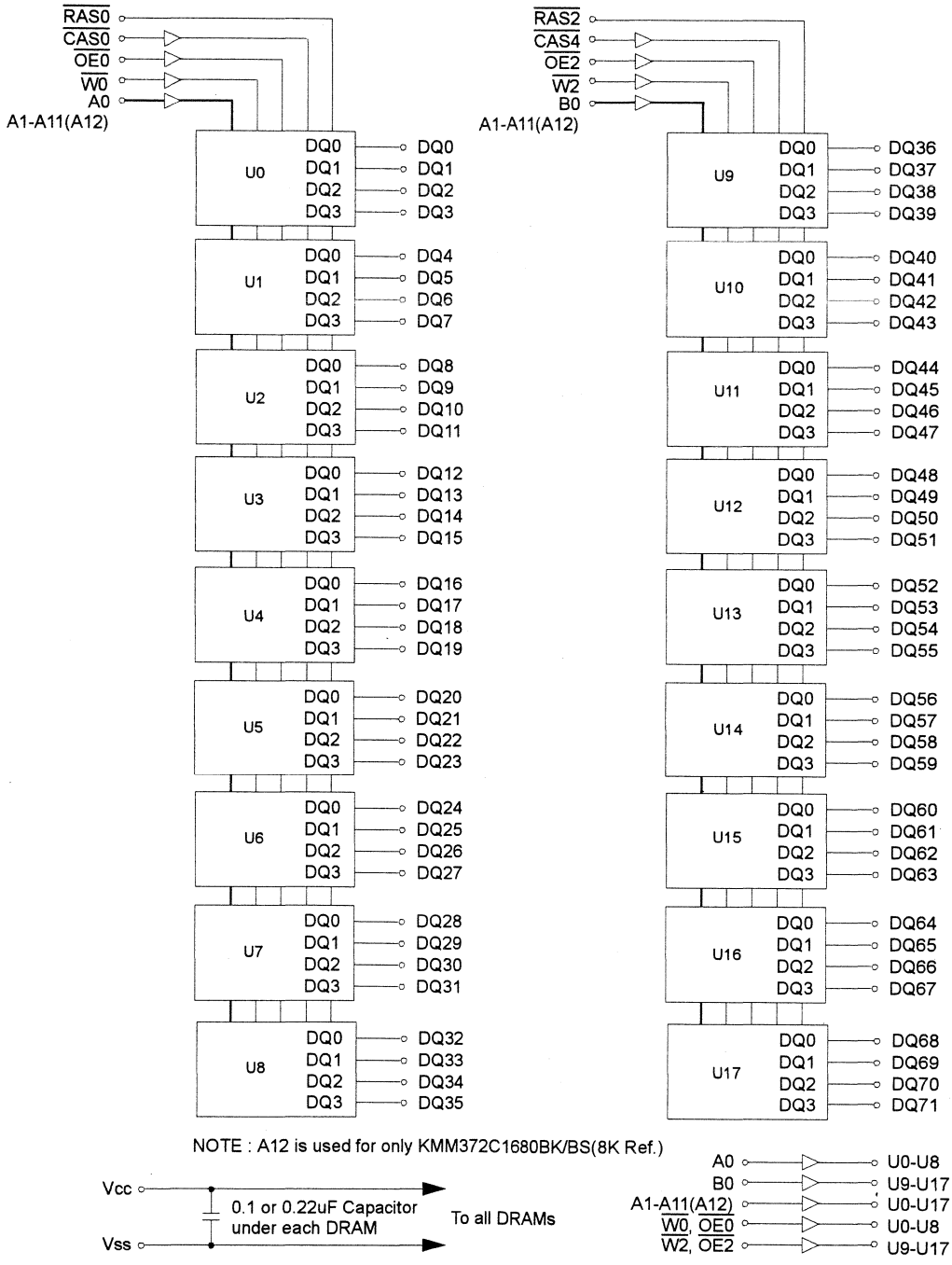
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	1	1
PD3	1	1
PD4	1	1
PD5	0	0
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	18	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372C1600BK/BS		KMM372C1680BK/BS		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	2160	-	1620	mA
	-6	-	1980	-	1440	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	2160	-	1620	mA
	-6	-	1980	-	1440	mA
I_{CC4}	-5	-	1260	-	1080	mA
	-6	-	1080	-	900	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	2160	-	1260	mA
	-6	-	1980	-	1440	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	73	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS4}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,11
Access time from column address	t_{AA}		30		35	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,11
Output buffer turn-off delay	t_{OFF}	5	18	5	20	ns	6,11
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	11
$\overline{CAS}$ hold time	t_{CSH}	45		55		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	11
Row address set-up time	t_{ASR}	5		5		ns	11
Row address hold time	t_{RAH}	8		8		ns	11
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	11
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referencde to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,11
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data in set-up time	t_{DS}	-2		-2		ns	9,11
Data in hold time	t_{DH}	15		15		ns	9,11
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ prechange to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7
$\overline{RAS}$ ro $\overline{W}$ delay time	t_{RWD}	73		85		ns	7,11

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	11
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	11
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3,11
Fast page mode cycle time	t_{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	76		85		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	11
$\overline{OE}$ access time	t_{OEA}		18		20	ns	11
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	11
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

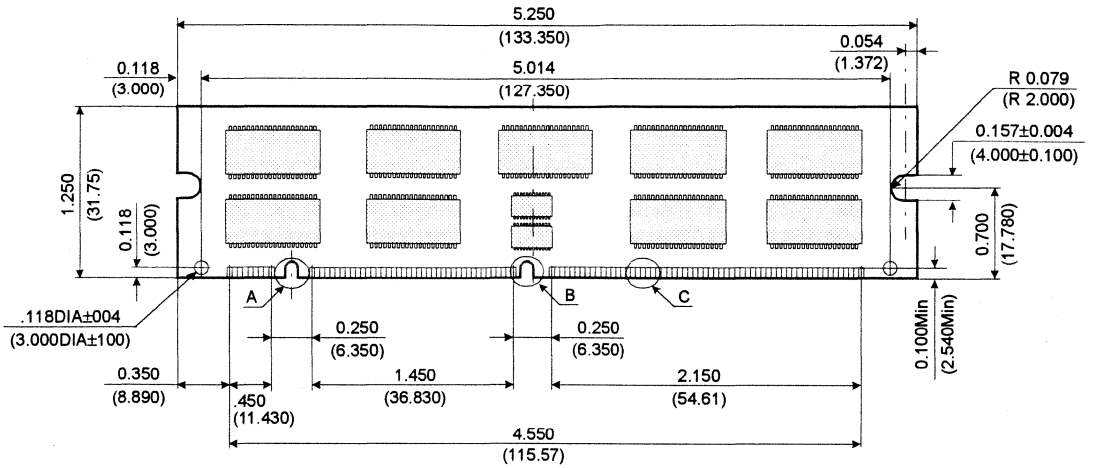
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

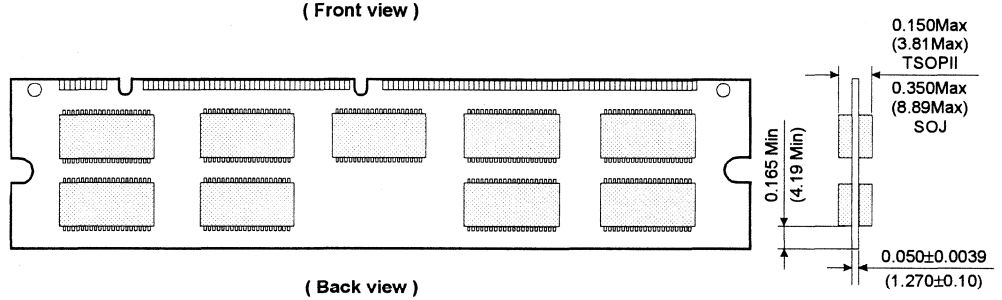
11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

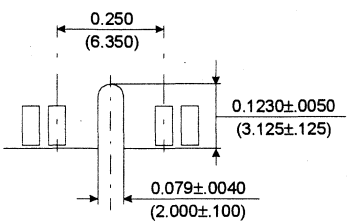
Units : Inches (millimeters)



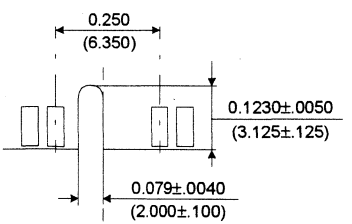
(Front view)



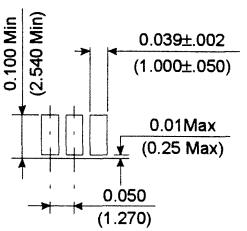
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx4 DRAM with Fast Page mode, SOJ or TSOP II.
DRAM Part No. : KMM372C1600BK/BS - KM44C16100BK, KM44C16100BS.
KMM372C1680BK/BS - KM44C16000BK, KM44C16000BS.

KMM372E160(8)0BK/BS EDO Mode

16M x 72 DRAM DIMM with ECC Using 16Mx4, 4K & 8K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM372E160(8)0B is a 16Mx72bits Dynamic RAM high density memory module. The Samsung KMM372E160(8)0B consists of eighteen CMOS 16Mx4bits DRAMs in SOJ/TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372E160(8)0B is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	18ns	84ns	20ns
-6	60ns	20ns	104ns	25ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM372E1600BK	SOJ	4K	4K/64ms	
KMM372E1600BS	TSOP			
KMM372E1680BK	SOJ	8K	4K/64ms	8K/64ms
KMM372E1680BS	TSOP			

- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1250mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	$\overline{Vss}$	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	$\overline{RFU}$	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	*$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	RSVD	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	$\overline{RFU}$	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	*$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM372E1680BK/BS (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a resistor to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
A0, B0, A1 - A12	Address Input(8K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

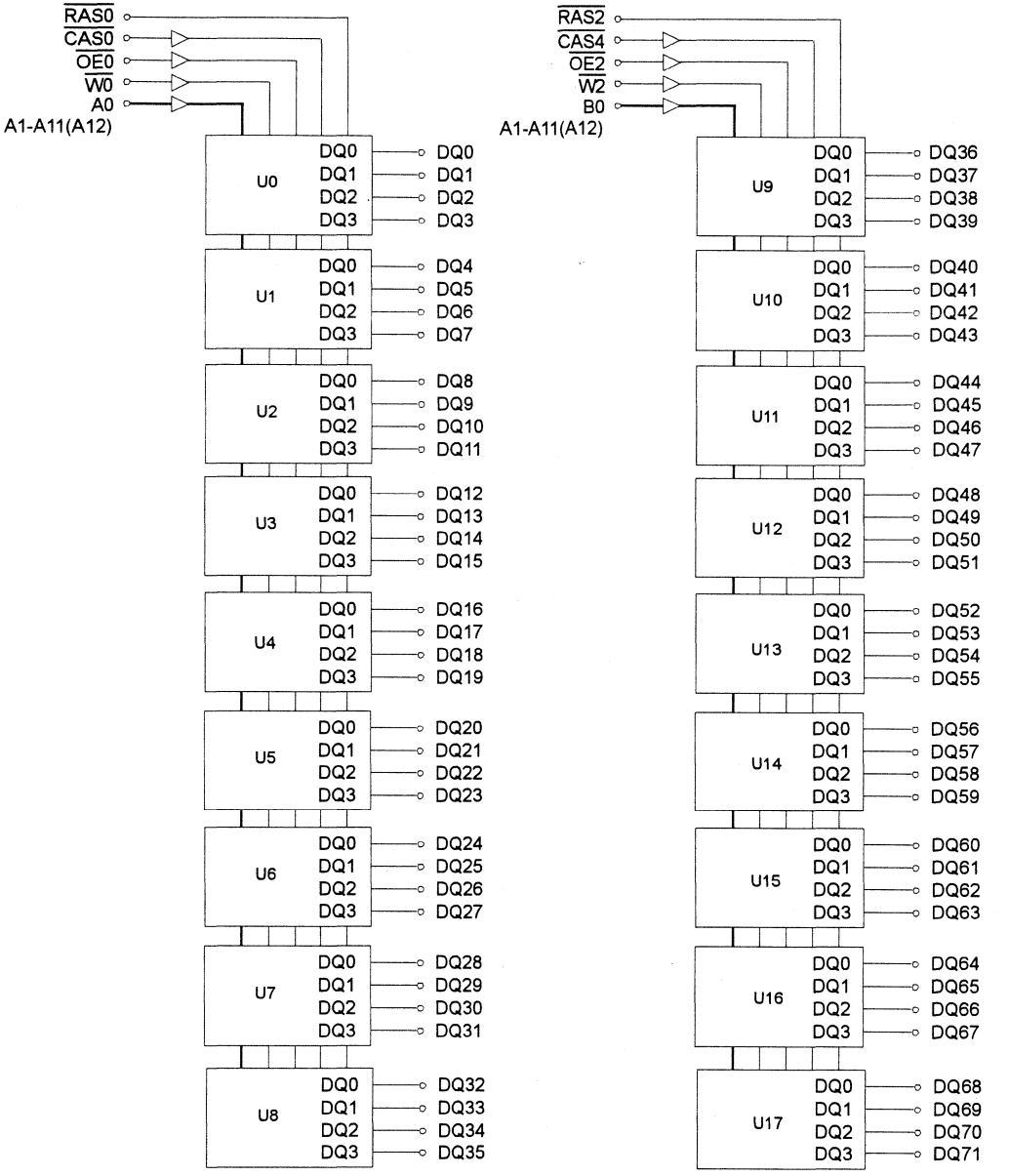
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	1	1
PD3	1	1
PD4	1	1
PD5	1	1
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	18	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372E1600BK/BS		KMM372E1680BK/BS		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	2160	-	1620	mA
	-6	-	1980	-	1440	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	2160	-	1620	mA
	-6	-	1980	-	1440	mA
I_{CC4}	-5	-	1980	-	1800	mA
	-6	-	1800	-	1620	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	2160	-	1620	mA
	-6	-	1980	-	1440	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	73	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS4}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,13
Access time from column address	t_{AA}		30		35	ns	3,10,13
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,13
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,13
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	18	ns	6,11,13
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	13
$\overline{CAS}$ hold time	t_{CSH}	36		43		ns	13
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,13
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	13
Row address set-up time	t_{ASR}	5		5		ns	13
Row address hold time	t_{RAH}	8		8		ns	13
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	13
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,13
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	18		20		ns	13
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,13
Data hold time	t_{DH}	13		15		ns	9,13
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		38		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		83		ns	7,13

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	48		53		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	13
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	13
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,13
Hyper page cycle time	t_{HPC}	20		25		ns	12
Hyper page read-modify-write cycle time	t_{HPRWC}	70		77		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	13
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	13
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	13
$\overline{OE}$ access time	t_{OEA}		18		20	ns	13
$\overline{OE}$ to data delay	t_{OED}	18		18		ns	13
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	8	18	8	18	ns	13
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Output data hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{DOH}	10		10		ns	13
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	15	3	15	ns	6,11
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	8	18	8	20	ns	6,13
$\overline{W}$ to data delay	t_{WED}	20		20		ns	13
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

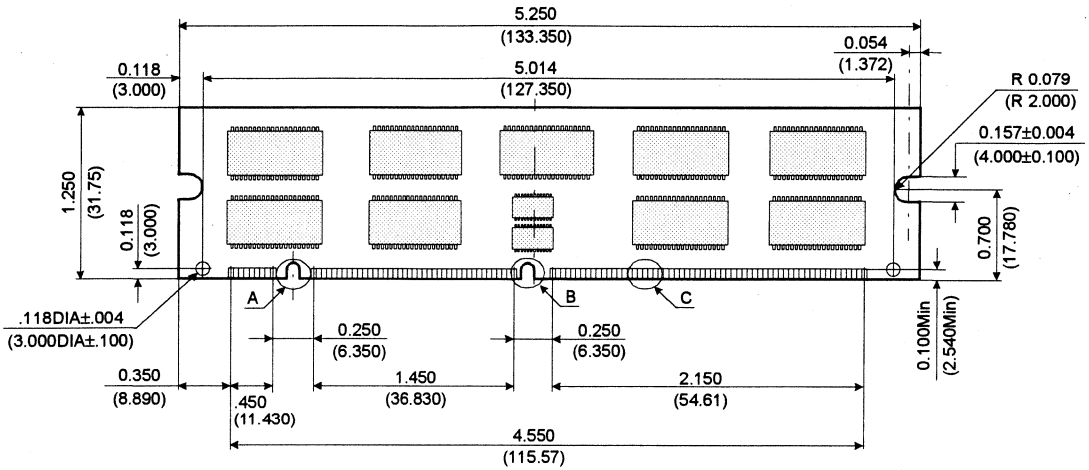
12. $t_{ASC} \geq 6ns$

13. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

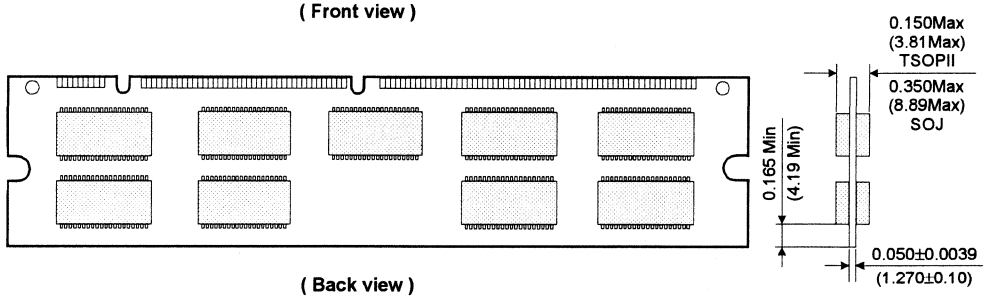
4

PACKAGE DIMENSIONS

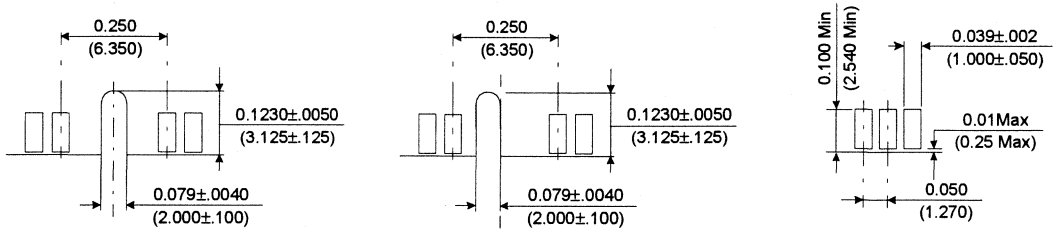
Units : Inches (millimeters)



(Front view)



(Back view)



Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx4 DRAM with EDO mode, SOJ or TSOPII.
DRAM Part No. : KMM372E1600BK/BS - KM44C16104BK, KM44C16104BS.
KMM372E1680BK/BS - KM44C16004BK, KM44C16004BS.

KMM372C320(8)0BK Fast Page Mode

32M x 72 DRAM DIMM with ECC Using 16Mx4, 4K & 8K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM372C320(8)0B is a 32Mx72bits Dynamic RAM high density memory module. The Samsung KMM372C320(8)0B consists of thirty-six CMOS 16Mx4bits DRAMs in SOJ 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372C320(8)0B is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-5	50ns	18ns	90ns	35ns
-6	60ns	20ns	110ns	40ns

FEATURES

• Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM372C3200BK	SOJ	4K	4K/64ms	
KMM372C3280BK	SOJ	8K	4K/64ms	8K/64ms

- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(2000mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM372C3280BK (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a resistor to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
A0, B0, A1 - A12	Address Input(8K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$, 1,4,5	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

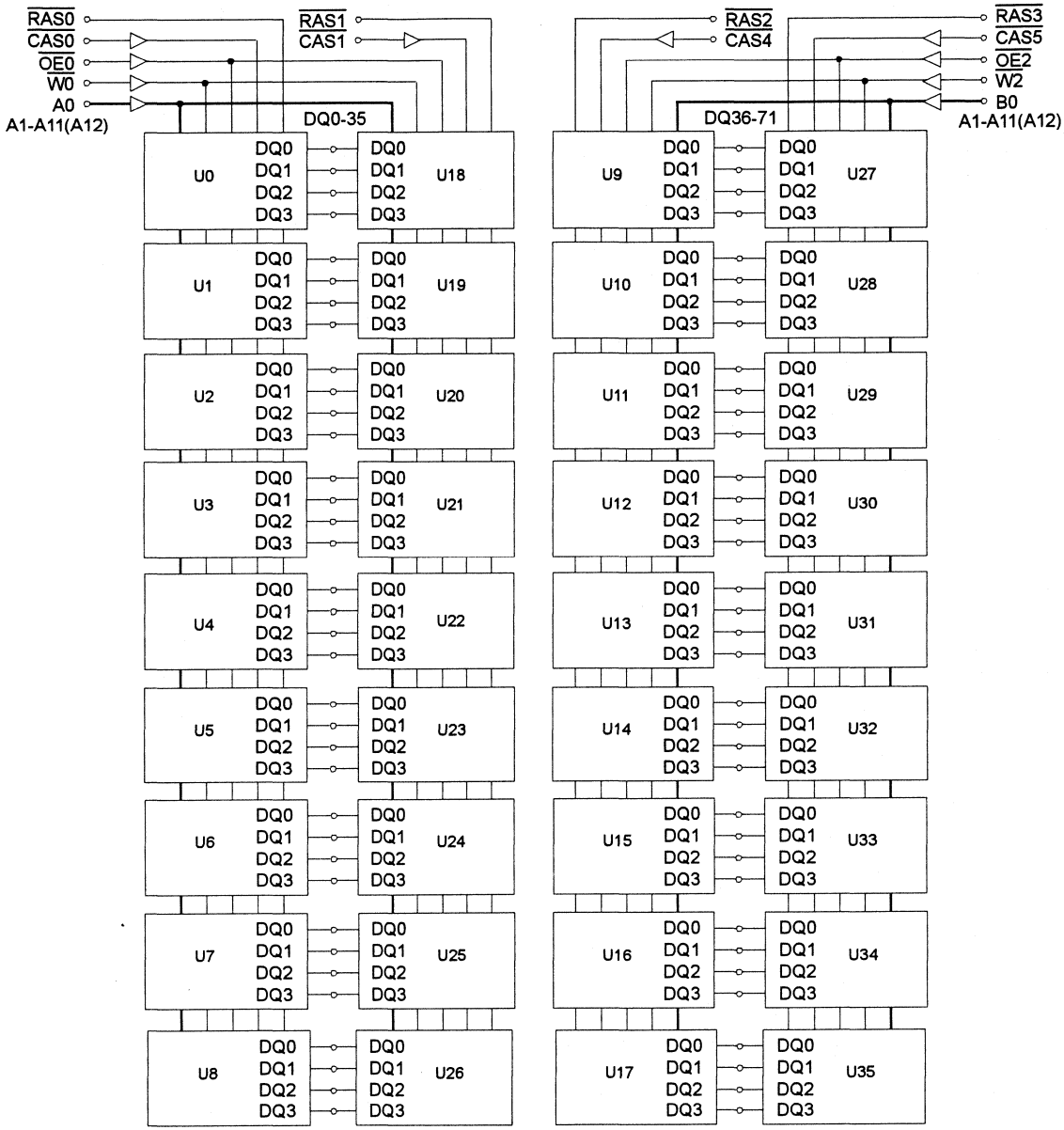
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	0	0
PD4	0	0
PD5	0	0
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

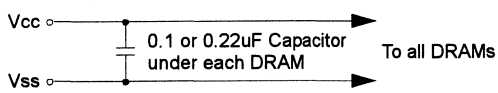
PD : 0 for Vol of Drive IC & 1 for N.C

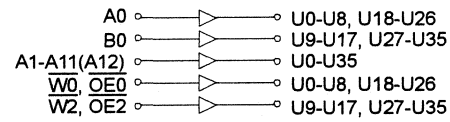
ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM372C3280BK(8K Ref.)





SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	36	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372C3200BK		KMM372C3280BK		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	2260	-	1720	mA
	-6	-	2080	-	1540	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	2260	-	1720	mA
	-6	-	2080	-	1540	mA
I_{CC4}	-5	-	1360	-	1180	mA
	-6	-	1180	-	1000	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	2260	-	1720	mA
	-6	-	2080	-	1540	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-10	10	-10	10	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}* : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}* : Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{PC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	73	pF
Input capacitance[$\overline{CAS0}$, 1, 4, 5]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	24	pF

AC CHARACTERISTICS (0°C ≤T_A≤70°C , V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,11
Access time from column address	t_{AA}		30		35	ns	3,10,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,11
Output buffer turn-off delay	t_{OFF}	5	18	5	20	ns	6,11
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	11
$\overline{CAS}$ hold time	t_{CSH}	45		55		ns	11
$\overline{CAS}$ pulse width	t_{CAS}	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,11
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	11
Row address set-up time	t_{ASR}	5		5		ns	11
Row address hold time	t_{RAH}	8		8		ns	11
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	11
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referencde to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,11
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		ns	11
Write command to $\overline{CAS}$ lead time	t_{CWL}	13		15		ns	
Data in set-up time	t_{DS}	-2		-2		ns	9,11
Data in hold time	t_{DH}	15		15		ns	9,11
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		40		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ prechange to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	7
$\overline{RAS}$ ro $\overline{W}$ delay time	t_{RWD}	73		85		ns	7,11

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	11
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	11
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	3,11
Fast page mode cycle time	t_{PC}	35		40		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	76		85		ns	
$\overline{CAS}$ precharge time(Fast page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width(Fast page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	11
$\overline{OE}$ access time	t_{OEA}		18		20	ns	11
$\overline{OE}$ to data delay	t_{OED}	18		20		ns	11
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	5	18	5	20	ns	11
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{IH}/V_{IL}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

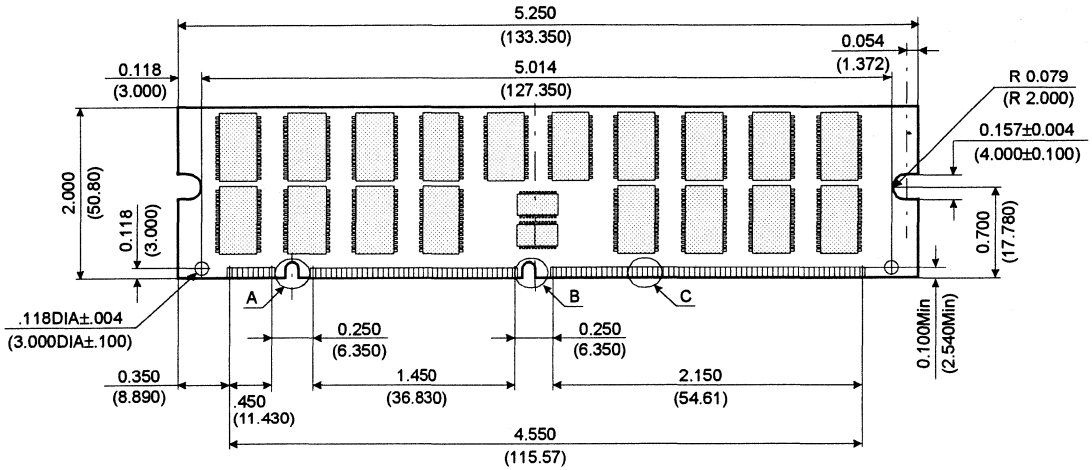
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

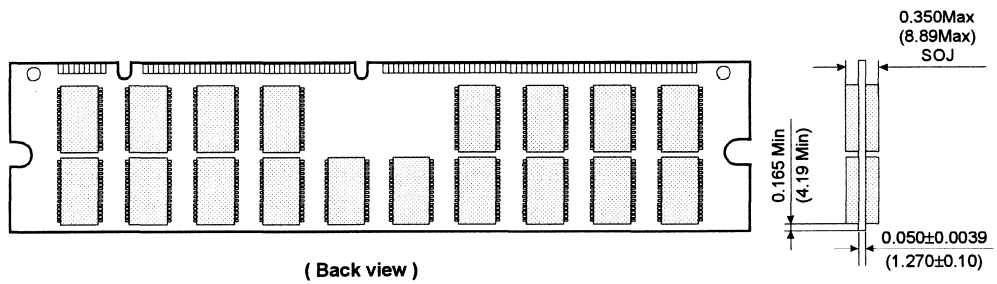
11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

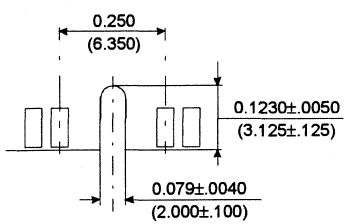
Units : Inches (millimeters)



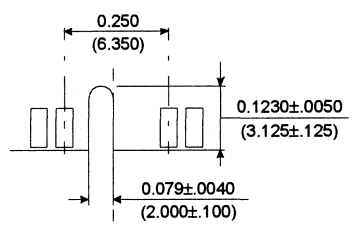
(Front view)



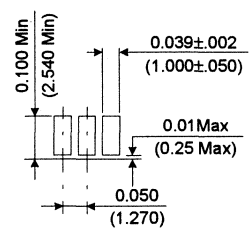
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx4 DRAM with Fast Page mode, SOJ
DRAM Part No. : KMM372C3200BK - KM44C16100BK
KMM372C3280BK - KM44C16000BK

KMM372E320(8)0BK EDO Mode

32M x 72 DRAM DIMM with ECC Using 16Mx4, 4K & 8K Refresh, 5V

GENERAL DESCRIPTION

The Samsung KMM372E320(8)0B is a 32Mx72bits Dynamic RAM high density memory module. The Samsung KMM372E320(8)0B consists of thirty-six CMOS 16Mx4bits DRAMs in SOJ 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372E320(8)0B is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	18ns	84ns	20ns
-6	60ns	20ns	104ns	25ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM372E3200BK	SOJ	4K	4K/64ms	
KMM372E3280BK	SOJ	8K	4K/64ms	8K/64ms

- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(2000mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*$\overline{CAS2}$	57	DQ22	85	Vss	113	*$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ49	129	$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS4}$	74	DQ32	102	Vcc	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	*$\overline{CAS6}$	75	DQ33	103	DQ50	131	*$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vcc	112	$\overline{CAS1}$	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM372E3280BK (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a resistor to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
A0, B0, A1 - A12	Address Input(8K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$, 1,4,5	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

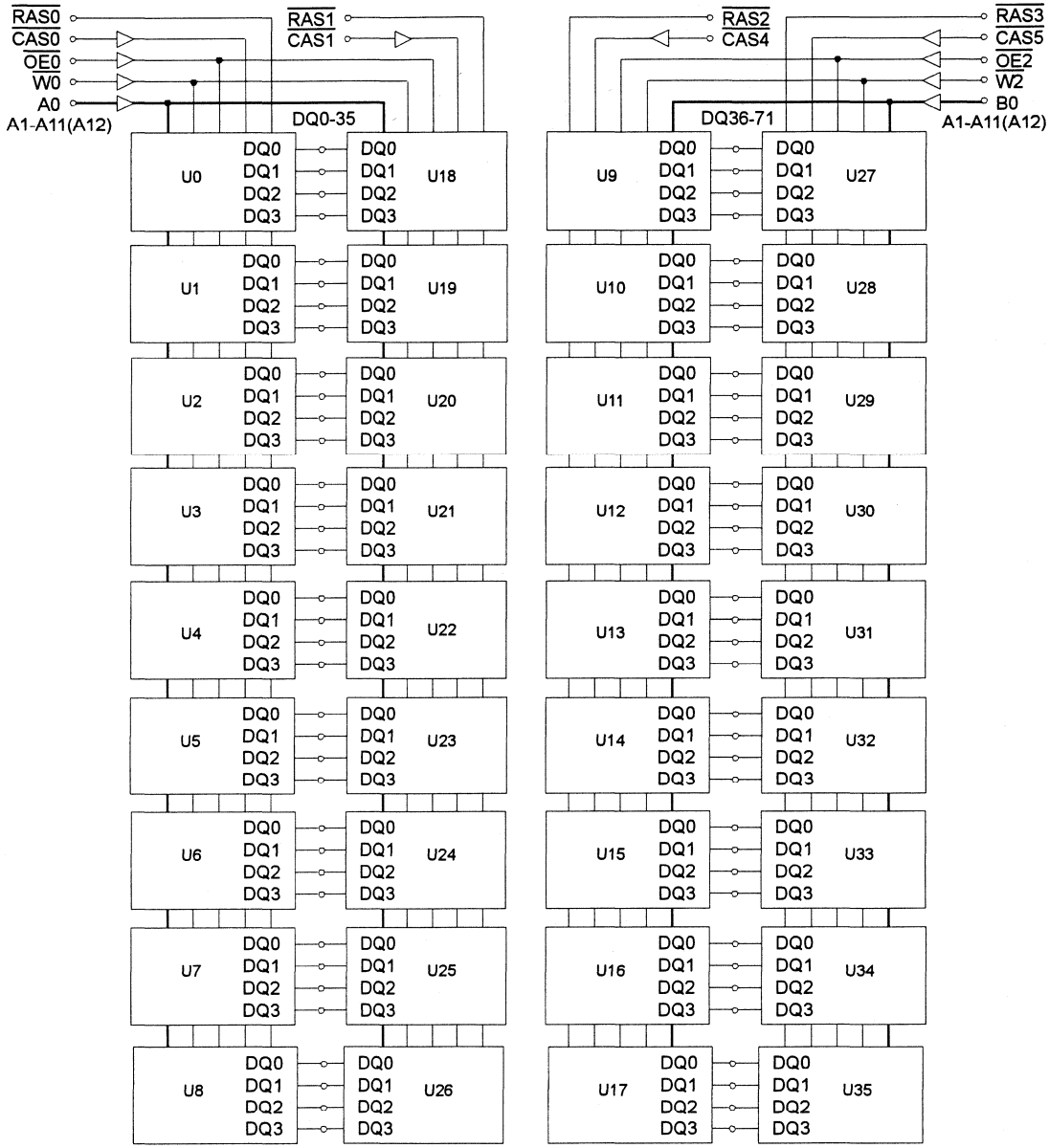
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	0	0
PD4	0	0
PD5	1	1
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

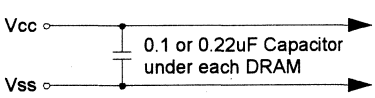
PD : 0 for Vol of Drive IC & 1 for N.C

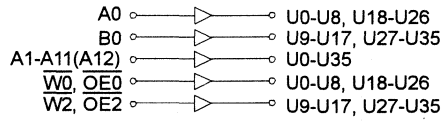
ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM372E3280BK(8K Ref.)





ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	36	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width≤20ns, which is measured at Vcc.

*2 : -2.0V at pulse width≤20ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372E3200BK		KMM372E3280BK		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	2260	-	1720	mA
	-6	-	2080	-	1540	mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-5	-	2260	-	1720	mA
	-6	-	2080	-	1540	mA
I_{CC4}	-5	-	2080	-	1900	mA
	-6	-	1900	-	1720	mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-5	-	2260	-	1720	mA
	-6	-	2080	-	1540	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-10	10	-10	10	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	73	pF
Input capacitance[$\overline{CAS0}$, 1,4,5]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	24	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,13
Access time from column address	t_{AA}		30		35	ns	3,10,13
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,13
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,13
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	18	ns	6,11,13
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	13
$\overline{CAS}$ hold time	t_{CSH}	36		43		ns	13
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,13
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	13
Row address set-up time	t_{ASR}	5		5		ns	13
Row address hold time	t_{RAH}	8		8		ns	13
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	13
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,13
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	18		20		ns	13
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,13
Data hold time	t_{DH}	13		15		ns	9,13
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		38		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		83		ns	7,13

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	48		53		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	13
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	13
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,13
Hyper page cycle time	t_{HPC}	20		25		ns	12
Hyper page read-modify-write cycle time	t_{HPRWC}	70		77		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	13
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	13
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	13
$\overline{OE}$ access time	t_{OEA}		18		20	ns	13
$\overline{OE}$ to data delay	t_{OED}	18		18		ns	13
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	8	18	8	18	ns	13
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Output data hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{DOH}	10		10		ns	13
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	15	3	15	ns	6,11
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	8	18	8	20	ns	6,13
$\overline{W}$ to data delay	t_{WED}	20		20		ns	13
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{IH}/V_{IL}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

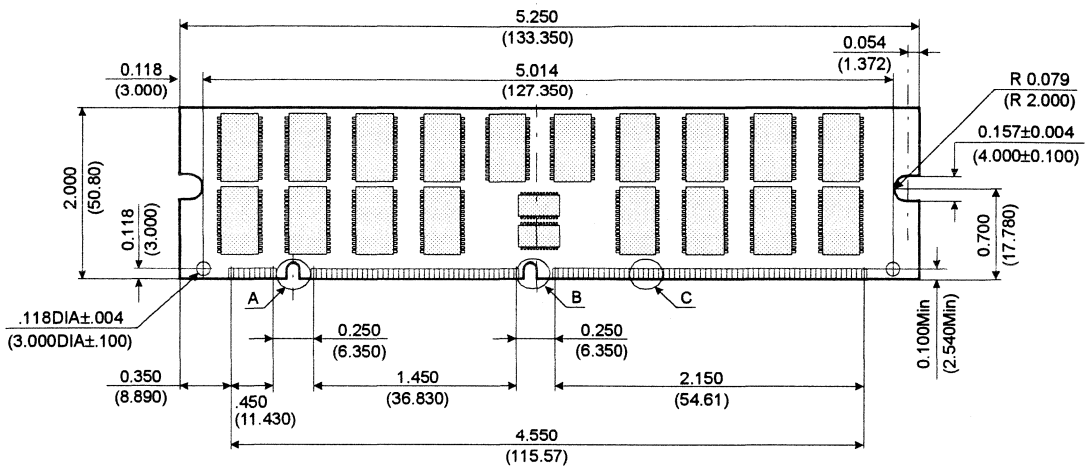
11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

12. $t_{ASC} \geq 6ns$

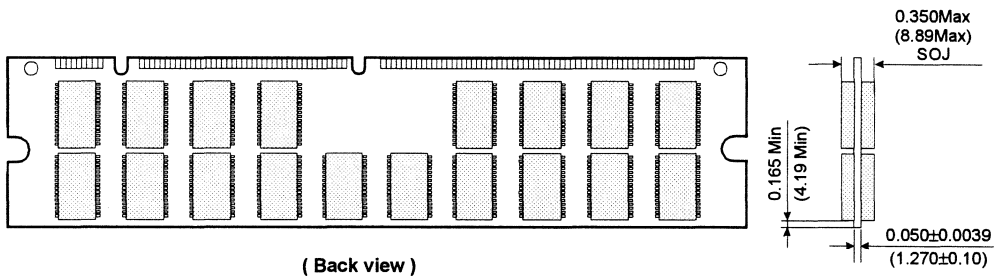
13. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

PACKAGE DIMENSIONS

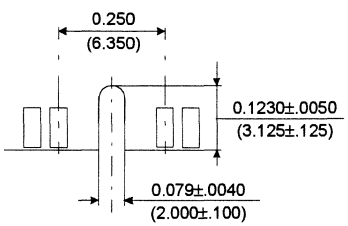
Units : Inches (millimeters)



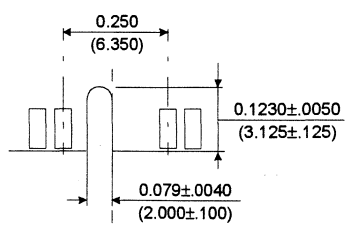
(Front view)



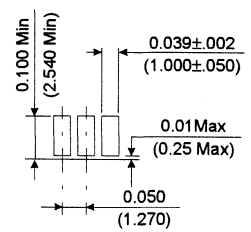
(Back view)



Detail A



Detail B

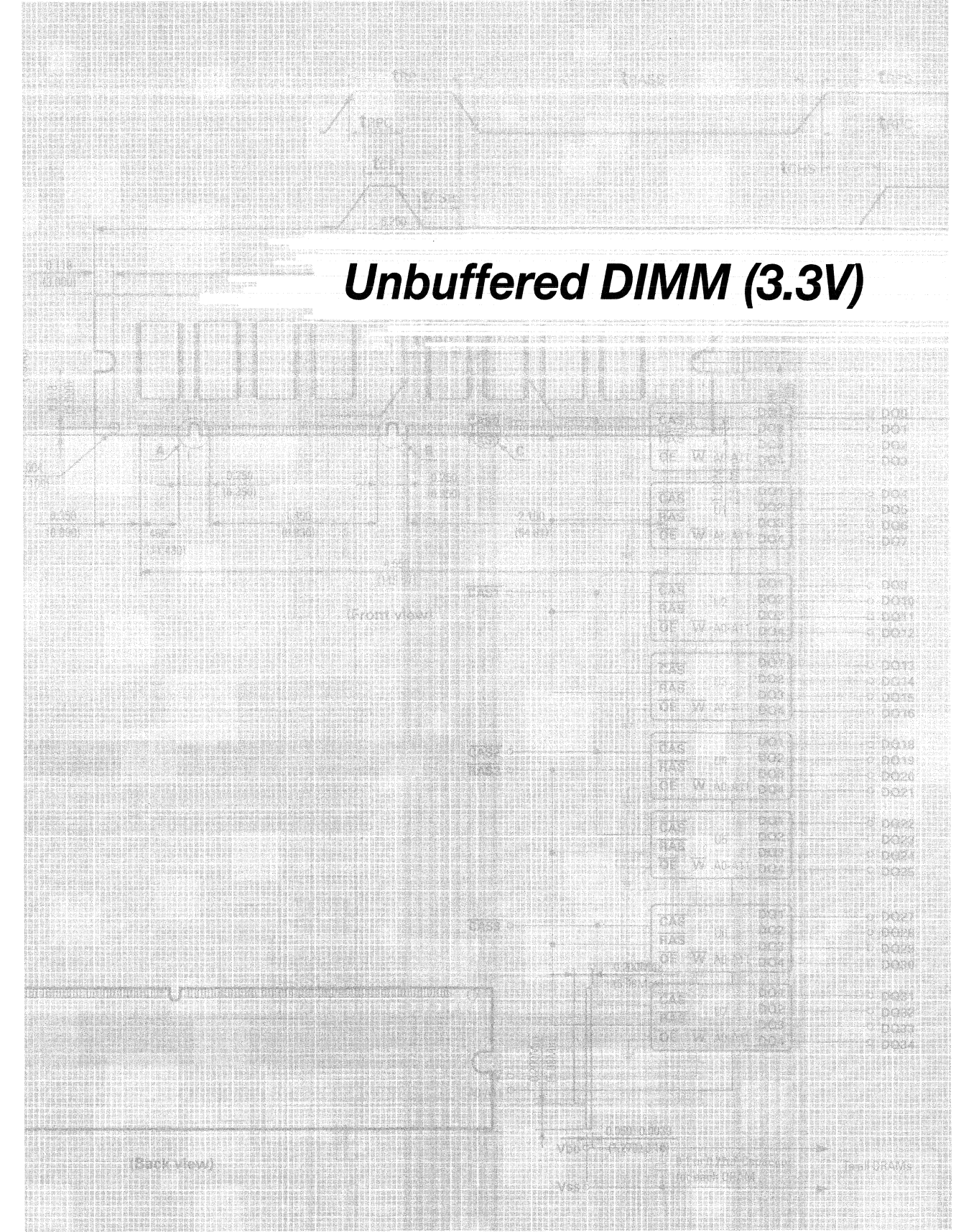


Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx4 DRAM with EDO mode, SOJ.
DRAM Part No. : KMM372E3200BK - KM44C16104BK.
KMM372E3280BK - KM44C16004BK.

Unbuffered DIMM (3.3V)



KMM366F124CJ1 EDO Mode without buffer

1M x 64 DRAM DIMM using 1Mx16, 3.3V

GENERAL DESCRIPTION

The Samsung KMM366F124CJ1 is a 1Mx64bits Dynamic RAM high density memory module. The Samsung KMM366F124CJ1 consists of four CMOS 1Mx16bits DRAMs in SOJ 400mil package and one 1K/2K EEPROM for SPD in 8-pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM366F124CJ1 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	15ns	84ns	20ns
-6	60ns	17ns	104ns	25ns

FEATURES

- Part Identification
  - KMM366F124CJ1(1024 cycles/16ms Ref., SOJ)
- New JEDEC standard proposal without buffer
- Serial Presence Detect with EEPROM
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), single sided component

4

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS1}$	57	DQ18	85	Vss	113	$\overline{CAS5}$	141	DQ50
2	DQ0	30	$\overline{RAS0}$	58	DQ19	86	DQ32	114	*$\overline{RAS1}$	142	DQ51
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ33	115	DU	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	DU	90	Vcc	118	A3	146	DU
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	*A10	66	DQ22	94	DQ39	122	*A11	150	DQ54
11	DQ8	39	*A12	67	DQ23	95	DQ40	123	*A13	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	DU	153	DQ56
14	DQ10	42	DU	70	DQ25	98	DQ42	126	DU	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	$\overline{OE2}$	72	DQ27	100	DQ44	128	DU	156	DQ59
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ45	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS2}$	74	DQ28	102	Vcc	130	$\overline{CAS6}$	158	DQ60
19	DQ14	47	$\overline{CAS3}$	75	DQ29	103	DQ46	131	$\overline{CAS7}$	159	DQ61
20	DQ15	48	$\overline{W2}$	76	DQ30	104	DQ47	132	DU	160	DQ62
21	*CB0	49	Vcc	77	DQ31	105	*CB4	133	Vcc	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	NC	107	Vss	135	NC	163	NC
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	Vcc	54	Vss	82	**SDA	110	Vcc	138	Vss	166	**SA1
27	$\overline{W0}$	55	DQ16	83	**SCL	111	$\overline{DU}$	139	DQ48	167	**SA2
28	$\overline{CAS0}$	56	DQ17	84	Vcc	112	$\overline{CAS4}$	140	DQ49	168	Vcc

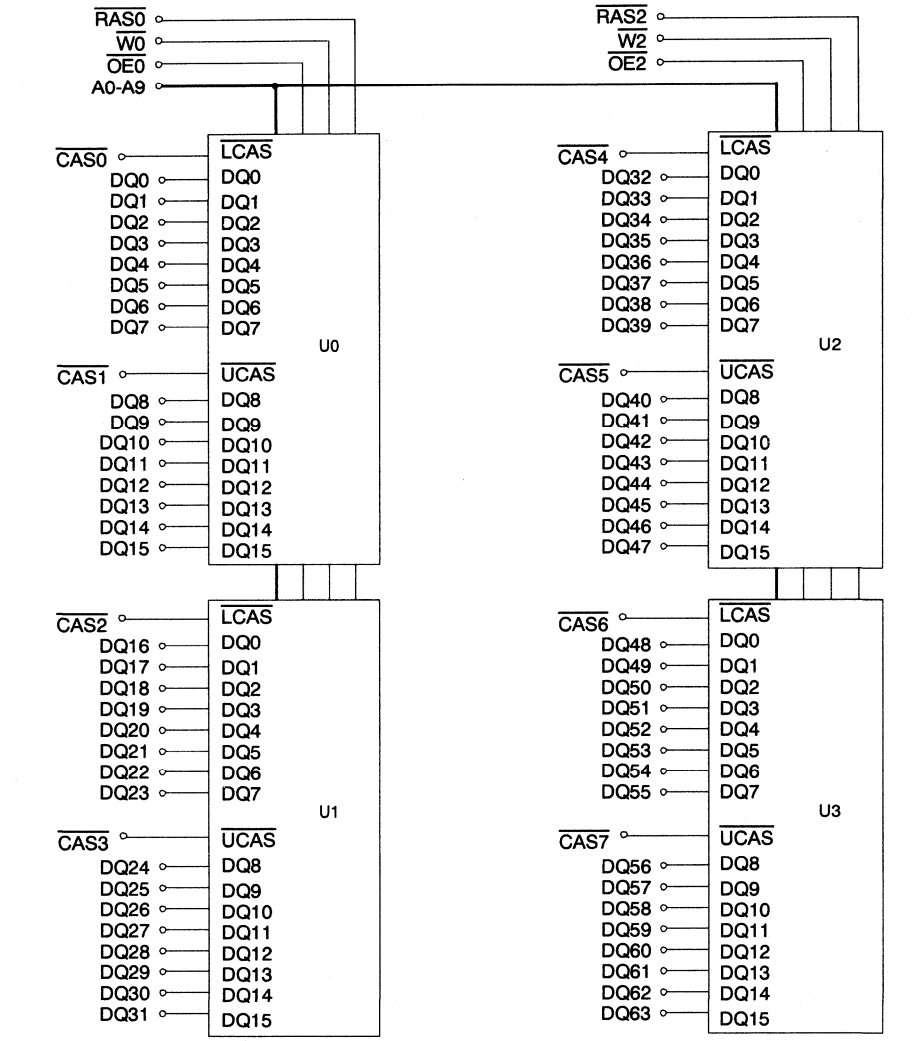
PIN NAMES

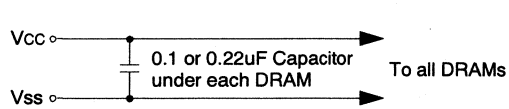
Pin Name	Function
A0 - A9	Address Input (1K Ref.)
DQ0 - DQ63	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Colume Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
DU	Don't use
**SDA	Serial Address /Data I/O
**SCL	Serial Clock
SA0 -SA2	Address in EEPROM
*CB0 - *CB7	Check Bit

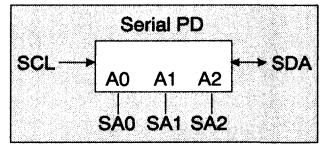
* These pins are not used in this module.

** These pins should be NC in the system which does not support SPD.

FUNCTIONAL BLOCK DIAGRAM







ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_d	4	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V/15ns, Pulse width is measured at V_{CC}.

*2 : -1.3V/15ns, Pulse width is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM366F124CJ1		Unit
		Min	Max	
I_{CC1}	-5	-	560	mA
	-6	-	520	mA
I_{CC2}	Don't care	-	8	mA
I_{CC3}	-5	-	560	mA
	-6	-	520	mA
I_{CC4}	-5	-	400	mA
	-6	-	360	mA
I_{CC5}	Don't care	-	2	mA
I_{CC6}	-5	-	560	mA
	-6	-	520	mA
$I_{I(L)}$	Don't care	-20	20	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{I(L)}$: Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.3V, all other pins not under test=0 V)

$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V≤ V_{OUT}≤V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A9]	C_{IN1}	-	30	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	24	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	24	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	17	pF
Input/Output capacitance[DQ0-DQ63]	C_{DQ1}	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, Output loading C_L=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	130		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		15		17	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	15	ns	6
Transition time(rise and fall)	t_T	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		17		ns	
$\overline{CAS}$ hold time	t_{CSH}	40		50		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	35	20	43	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	13
Column address hold time	t_{CAH}	8		10		ns	13
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	16
Data set-up time	t_{DS}	0		0		ns	9,19
Data hold time	t_{DH}	8		10		ns	9,19
Refresh period (1K Ref)	t_{REF}		16		16	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ dealy time	t_{CWD}	38		42		ns	7
$\overline{RAS}$ to $\overline{W}$ dealy time	t_{RWD}	73		85		ns	7

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.2/0.7V$, $V_{oh}/V_{ol}=2.0/0.8V$, Output loading $C_L=100pF$

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	17
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	18
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}*		28		35	ns	3
Hyper page mode cycle time	t_{HPC}	20		25		ns	11
Hyper page mode read-modify-write cycle time	t_{HPRWC}	68		77		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	8		10		ns	14
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{OE}$ access time	t_{OEA}		13		15	ns	3
$\overline{OE}$ to data delay	t_{OED}	13		15		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	13	3	15	ns	6
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	6,12
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	6
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	t_{WPE}	5		5		ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF, Voh=2.0V and Vol=0.8V.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non-restrictive operating parameter. They are inclueded in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above contitions are satisfied, the condition of the data out is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. $t_{ASC} \geq 6ns$

12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condtion of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condtion of the output is achieved by $\overline{RAS}$ high going.

13. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.

14. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

15. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

16. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

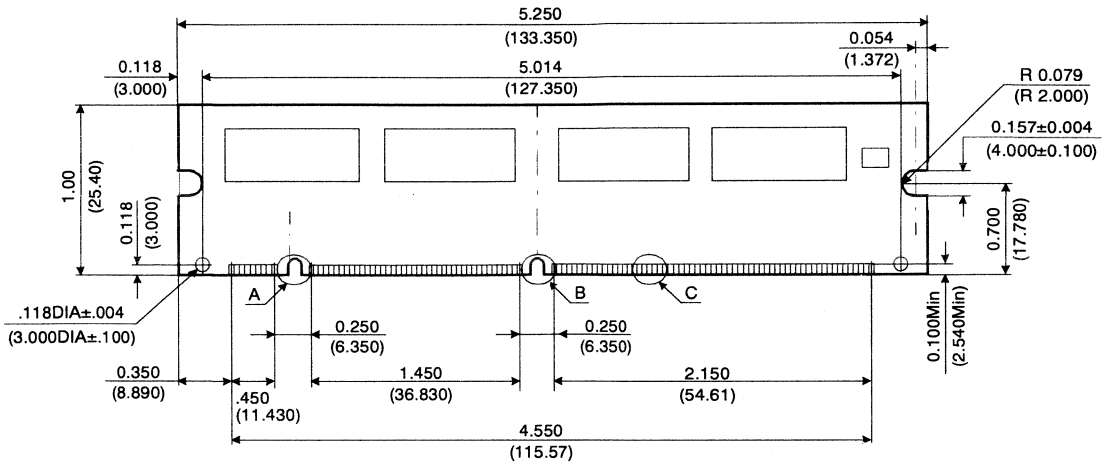
17. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.

18. t_{CHR} is referenced to later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.

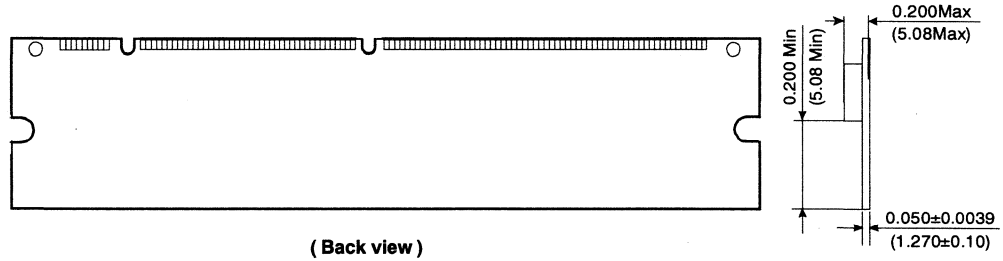
19. t_{DS}, t_{DH} is independently specified for lower byte DIN(0~7), upper byte DIN(8~15).

PACKAGE DIMENSIONS

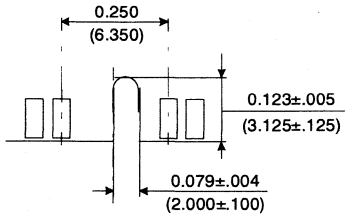
Units : Inches (millimeters)



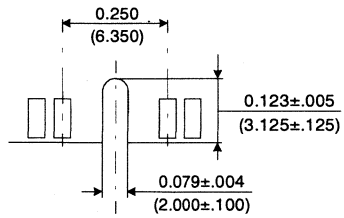
(Front view)



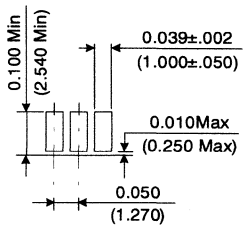
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 1Mx16 DRAM with EDO mode, SOJ
DRAM Part No. : KMM366F124CJ1 -- KM416V1204CJ

KMM374F124CJ1 EDO Mode without buffer

1M x 72 DRAM DIMM with ECC using 1Mx16 & 1Mx4, 1K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM374F124CJ1 is a 1Mx72bits Dynamic RAM high density memory module. The Samsung KMM374F124CJ1 consists of four CMOS 1Mx16bits DRAMs in SOJ 400mil package, two CMOS 1Mx4bits DRAMs in SOJ 300mil package and one 1K/2K EEPROM for SPD in 8-pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM374F124CJ1 is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

FEATURES

- Part Identification
  - KMM374F124CJ1 (1024 cycles/16ms, SOJ)
- New JEDEC standard proposal without buffer
- Serial Presence Detect with EEPROM
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), single sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-6	60ns	17ns	104ns	25ns

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS1}$	57	DQ18	85	Vss	113	$\overline{CAS5}$	141	DQ50
2	DQ0	30	$\overline{RAS0}$	58	DQ19	86	DQ32	114	*$\overline{RAS1}$	142	DQ51
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ33	115	DU	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	DU	90	Vcc	118	A3	146	DU
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	*A10	66	DQ22	94	DQ39	122	*A11	150	DQ54
11	DQ8	39	*A12	67	DQ23	95	DQ40	123	*A13	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	DU	153	DQ56
14	DQ10	42	DU	70	DQ25	98	DQ42	126	DU	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	$\overline{OE2}$	72	DQ27	100	DQ44	128	DU	156	DQ59
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ45	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS2}$	74	DQ28	102	Vcc	130	$\overline{CAS6}$	158	DQ60
19	DQ14	47	$\overline{CAS3}$	75	DQ29	103	DQ46	131	$\overline{CAS7}$	159	DQ61
20	DQ15	48	$\overline{W2}$	76	DQ30	104	DQ47	132	DU	160	DQ62
21	CB0	49	Vcc	77	DQ31	105	CB4	133	Vcc	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	NC	107	Vss	135	NC	163	NC
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	**SA0
26	Vcc	54	Vss	82	**SDA	110	Vcc	138	Vss	166	**SA1
27	$\overline{W0}$	55	DQ16	83	**SCL	111	DU	139	DQ48	167	**SA2
28	$\overline{CAS0}$	56	DQ17	84	Vcc	112	$\overline{CAS4}$	140	DQ49	168	Vcc

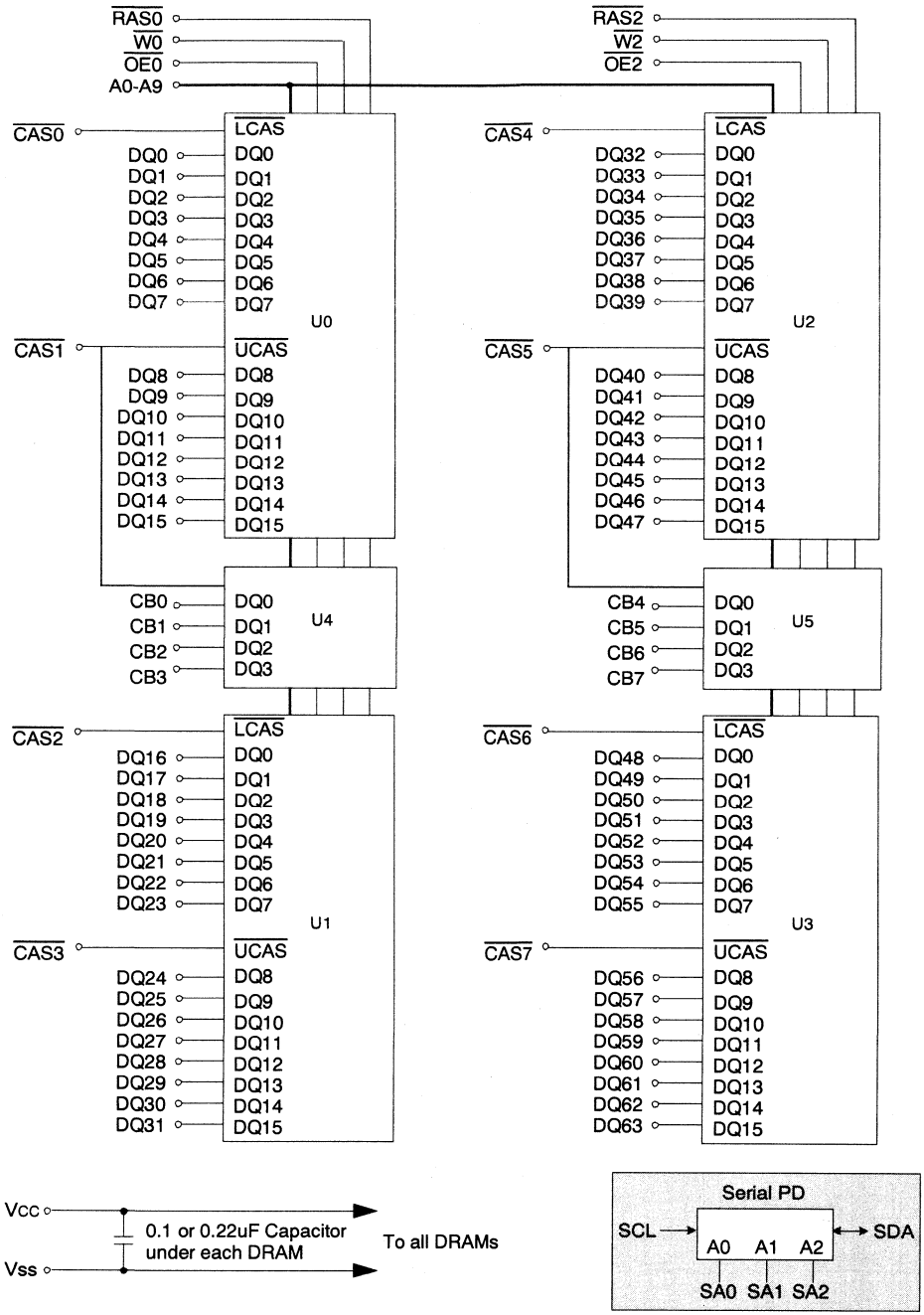
PIN NAMES

Pin Name	Function
A0 - A9	Address Input (1K Ref.)
DQ0 - DQ63	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Colume Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
DU	Don't use
**SDA	Serial Address /Data I/O
**SCL	Serial Clock
SA0 -SA2	Address in EEPROM
CB0 - CB7	Check Bit

* These pins are not used in this module.

** These pins should be NC in the system which does not support SPD.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_d	5.2	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for in tended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V/15ns, Pulse width is measured at V_{CC}.

*2 : -1.3V/15ns, Pulse width is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM374F124CJ1		Unit
		Min	Max	
I_{CC1}	6	-	640	mA
I_{CC2}	Don't care	-	10	mA
I_{CC3}	-6	-	640	mA
I_{CC4}	-6	-	480	mA
I_{CC5}	Don't care	-	5	mA
I_{CC6}	-6	-	640	mA
$I_{I(L)}$ $I_{O(L)}$	Don't care	-30 -5	30 5	uA uA
V_{OH} V_{OL}	Don't care	2.4 -	- 0.4	V V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{I(L)}$: Input Leakage Current (Any input 0≤ V_{IN}≤V_{CC}+0.3V, all other pins not under test=0 V)

$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V≤ V_{OUT}≤V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle, t_{HPC} .

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A9]	C_{IN1}	-	40	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	31	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	31	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	24	pF
Input/Output capacitance[DQ0-DQ63, CB0-CB7]	C_{DQ1}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, Output loading C_L=100pF

Parameter	Symbol	-6		Unit	Note
		Min	Max		
Random read or write cycle time	t_{RC}	104		ns	
Read-modify-write cycle time	t_{RWC}	155		ns	
Access time from $\overline{RAS}$	t_{RAC}		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		17	ns	3,4,5
Access time from column address	t_{AA}		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	15	ns	6
Transition time(rise and fall)	t_T	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	17		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	43	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		ns	
Row address set-up time	t_{ASR}	0		ns	
Row address hold time	t_{RAH}	10		ns	
Column address set-up time	t_{ASC}	0		ns	13
Column address hold time	t_{CAH}	10		ns	13
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		ns	
Read command set-up time	t_{RCS}	0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		ns	8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		ns	8
Write command hold time	t_{WCH}	10		ns	
Write command pulse width	t_{WP}	10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10		ns	16
Data set-up time	t_{DS}	0		ns	9,19
Data hold time	t_{DH}	10		ns	9,19
Refresh period (1K Ref.)	t_{REF}		16	ms	
Write command set-up time	t_{WCS}	0		ns	7
$\overline{CAS}$ to $\overline{W}$ dealy time	t_{CWD}	42		ns	7
$\overline{RAS}$ to $\overline{W}$ dealy time	t_{RWD}	85		ns	7

4

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.2/0.7V$, $V_{oh}/V_{ol}=2.0/0.8V$, Output loading $C_L=100pF$

Parameter	Symbol	-6		Unit	Note
		Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	55		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	60		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		ns	17
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		ns	18
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35	ns	3
Hyper page mode cycle time	t_{HPC}	25		ns	11
Hyper page mode read-modify write cycle time	t_{HPRWC}	77		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	10		ns	14
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		ns	
$\overline{OE}$ access time	t_{OEA}		15	ns	3
$\overline{OE}$ to data delay	t_{OED}	15		ns	
Output buffer turn off delay from $\overline{OE}$	t_{OEZ}	3	15	ns	6
$\overline{OE}$ command hold time	t_{OEH}	15		ns	
Output data hold time	t_{DOH}	5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	15	ns	6,12
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	15	ns	6
$\overline{W}$ to data delay	t_{WED}	15		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	t_{WPE}	5		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF, Voh=2.0V and Vol=0.8V.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non-restrictive operating parameter. They are inclueded in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above contitions are satisfied, the condition of the data out is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. $t_{ASC} \geq 6ns$

12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condtion of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condtion of the output is achieved by $\overline{RAS}$ high going.

13. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.

14. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

15. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

16. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

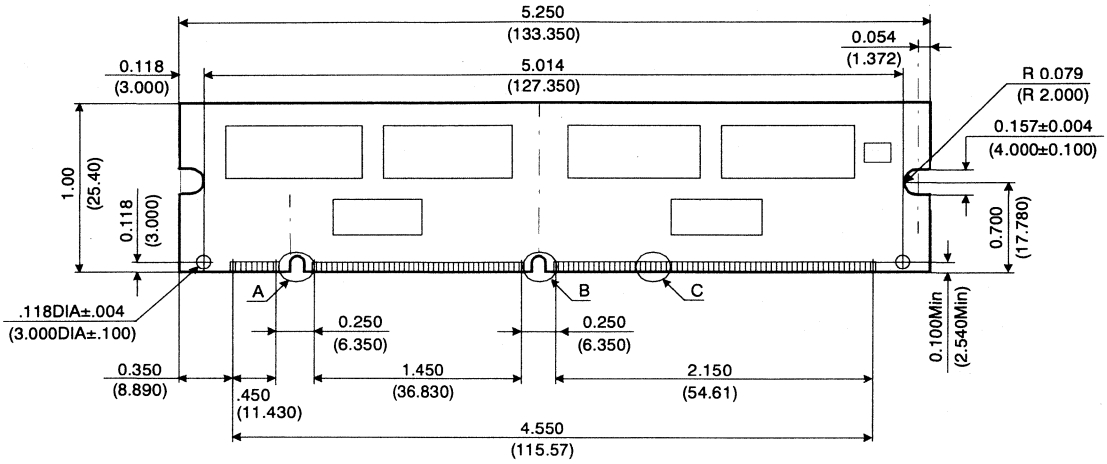
17. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.

18. t_{CHR} is referenced to later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.

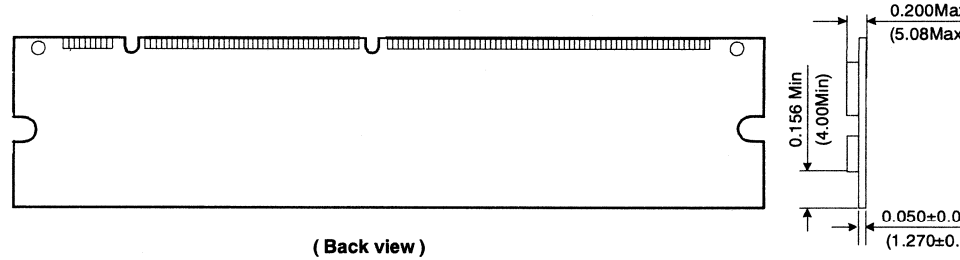
19. t_{DS}, t_{DH} is independently specified for lower byte DIN(0~7), upper byte DIN(8~15).

PACKAGE DIMENSIONS

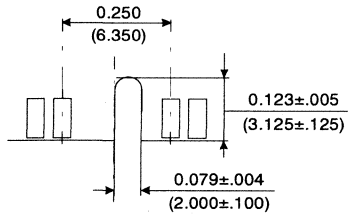
Units : Inches (millimeters)



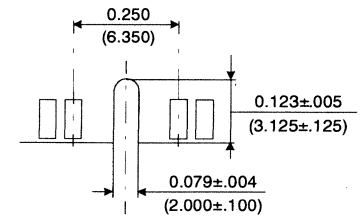
(Front view)



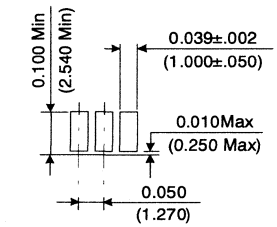
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 1Mx16 DRAM with EDO mode, SOJ and 1Mx4 DRAM with EDO mode, SOJ.
DRAM Part No. : KMM374F124CJ1 -- KM416V1204CJ and KM44V1004DJ

KMM366F224CJ1 EDO Mode without buffer

2M x 64 DRAM DIMM using 1Mx16, Dual Bank, 3.3V

GENERAL DESCRIPTION

The Samsung KMM366F224CJ1 is a 2Mx64bits Dynamic RAM high density memory module. The Samsung KMM366F224CJ1 consists of eight CMOS 1Mx16bits DRAMs in SOJ 400mil package and one 1K/2K EEPROM for SPD in 8-pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM366F224CJ1 is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	15ns	84ns	20ns
-6	60ns	17ns	104ns	25ns

FEATURES

- Part Identification
  - KMM366F224CJ1(1024 cycles/16ms, SOJ)
- New JEDEC standard proposal without buffer
- Serial Presence Detect with EEPROM
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), Double sided component

4

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS1}$	57	DQ18	85	Vss	113		141	DQ50
2	DQ0	30	$\overline{RAS0}$	58	DQ19	86	DQ32	114	$\overline{CAS5}$	142	DQ51
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ33	115	$\overline{RAS1}$	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	DU	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	Vss	145	NC
6	Vcc	34	A2	62	DU	90	Vcc	118	A1	146	DU
7	DQ4	35	A4	63	NC	91	DQ36	119	A3	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A5	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A7	149	DQ53
10	DQ7	38	*A10	66	DQ22	94	DQ39	122	A9	150	DQ54
11	DQ8	39	*A12	67	DQ23	95	DQ40	123	*A11	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	*A13	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	Vcc	153	DQ56
14	DQ10	42	DU	70	DQ25	98	DQ42	126	DU	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	DU	155	DQ58
16	DQ12	44	$\overline{OE2}$	72	DQ27	100	DQ44	128	Vss	156	DQ59
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ45	129	DU	157	Vcc
18	Vcc	46	$\overline{CAS2}$	74	DQ28	102	Vcc	130	$\overline{RAS3}$	158	DQ60
19	DQ14	47	$\overline{CAS3}$	75	DQ29	103	DQ46	131	$\overline{CAS6}$	159	DQ61
20	DQ15	48	$\overline{W2}$	76	DQ30	104	DQ47	132	CAS7	160	DQ62
21	*CB0	49	Vcc	77	DQ31	105	*CB4	133	DU	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	Vcc	162	Vss
23	Vss	51	NC	79	NC	107	Vss	135	NC	163	NC
24	NC	52	*CB2	80	NC	108	NC	136	NC	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB6	165	**SA0
26	Vcc	54	Vss	82	**SDA	110	Vcc	138	*CB7	166	**SA1
27	$\overline{W0}$	55	DQ16	83	**SCL	111	DU	139	Vss	167	**SA2
28	$\overline{CAS0}$	56	DQ17	84	Vcc	112	$\overline{CAS4}$	140	DQ48	168	Vcc

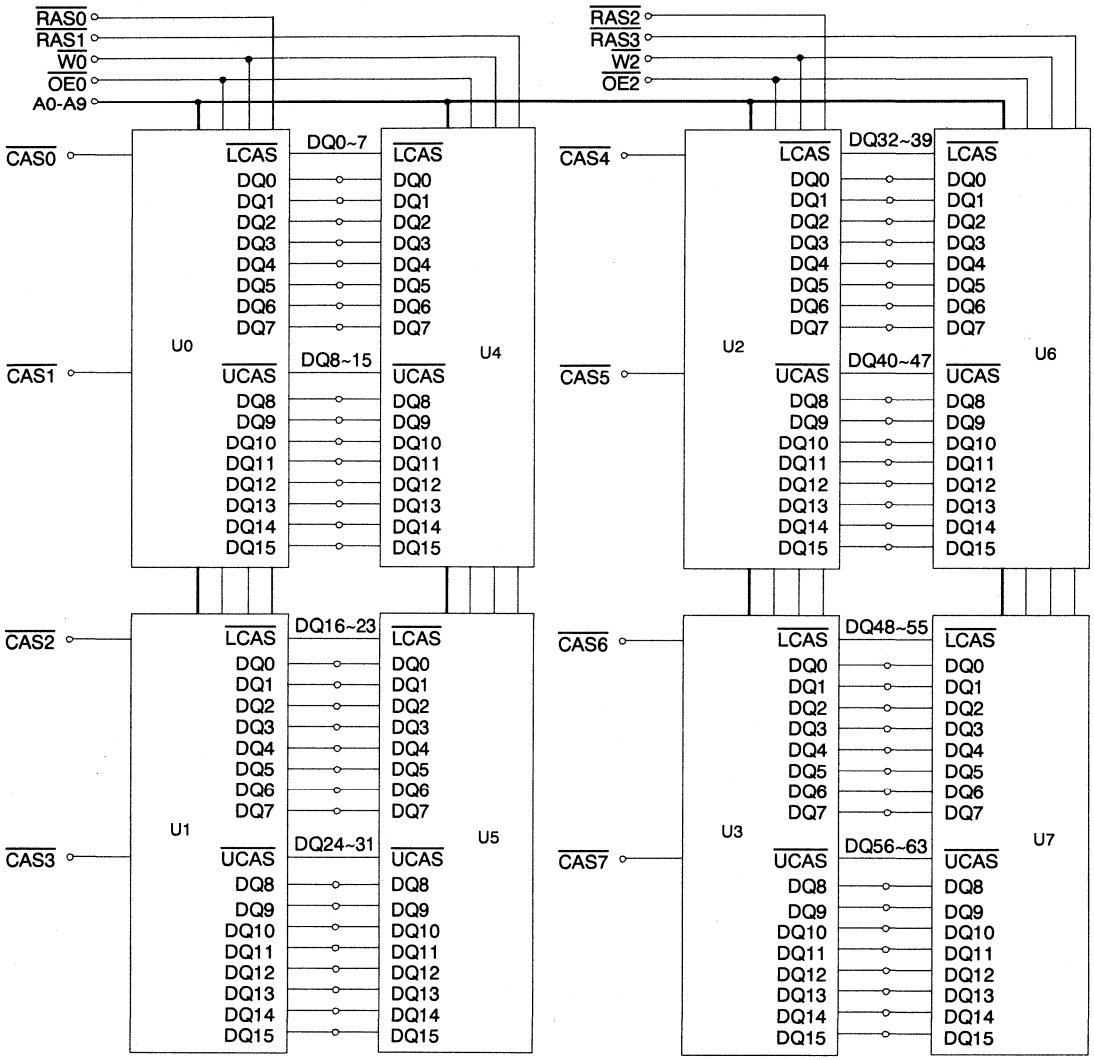
PIN NAMES

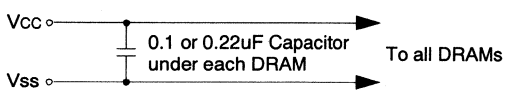
Pin Name	Function
A0 - A9	Address Input (1K Ref.)
DQ0 - DQ63	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Colume Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
DU	Don't use
**SDA	Serial Address /Data I/O
**SCL	Serial Clock
SA0 -SA2	Address in EEPROM
*CB0 - *CB7	Check Bit

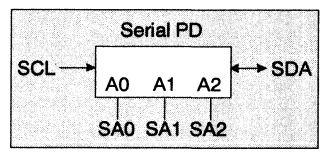
* These pins are not used in this module.

** These pins should be NC in the system which does not support SPD.

FUNCTIONAL BLOCK DIAGRAM







ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_d	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V/15ns, Pulse width is measured at V_{CC}.

*2 : -1.3V/15ns, Pulse width is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM366F224CJ1		Unit
		Min	Max	
I_{CC1}	-5 -6	- -	568 528	mA mA
I_{CC2}	Don't care	-	8	mA
I_{CC3}	-5 -6	- -	568 528	mA mA
I_{CC4}	-5 -6	- -	408 368	mA mA
I_{CC5}	Don't care	-	2	mA
I_{CC6}	-5 -6	- -	568 528	mA mA
$I_{I(L)}$ $I_{O(L)}$	Don't care	-40 -10	40 10	uA uA
V_{OH} V_{OL}	Don't care	2.4 -	- 0.4	V V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{I(L)}$: Input Leakage Current (Any input 0≤ V_{IN}≤V_{CC}+0.3V, all other pins not under test=0 V)

$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V≤ V_{OUT}≤V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A9]	C_{IN1}	-	50	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	38	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	24	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	24	pF
Input/Output capacitance[DQ0-DQ63]	C_{DQ1}	-	24	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, Output loading C_L=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	130		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		15		17	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	15	ns	6
Transition time(rise and fall)	t_T	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		17		ns	
$\overline{CAS}$ hold time	t_{CSH}	40		50		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	35	20	43	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	13
Column address hold time	t_{CAH}	8		10		ns	13
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	16
Data set-up time	t_{DS}	0		0		ns	9,19
Data hold time	t_{DH}	8		10		ns	9,19
Refresh period (1K Ref)	t_{REF}		16		16	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ dealy time	t_{CWD}	38		42		ns	7
$\overline{RAS}$ to $\overline{W}$ dealy time	t_{RWD}	73		85		ns	7

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.2/0.7V$, $V_{oh}/V_{ol}=2.0/0.8V$, output loading $C_L=100pF$

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	17
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	18
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3
Hyper page mode cycle time	t_{HPC}	20		25		ns	11
Hyper page mode read-modify-write cycle time	t_{HPRWC}	68		77		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	8		10		ns	14
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{OE}$ access time	t_{OEA}		13		15	ns	3
$\overline{OE}$ to data delay	t_{OED}	13		15		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	13	3	15	ns	6
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	6,12
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	6
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	t_{WPE}	5		5		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF, Voh=2.0V and Vol=0.8V.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non-restrictive operating parameter. They are inclueded in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above contitions are satisfied, the condition of the data out is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. $t_{ASC} \geq 6ns$

12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condtion of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condtion of the output is achieved by $\overline{RAS}$ high going.

13. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.

14. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

15. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

16. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

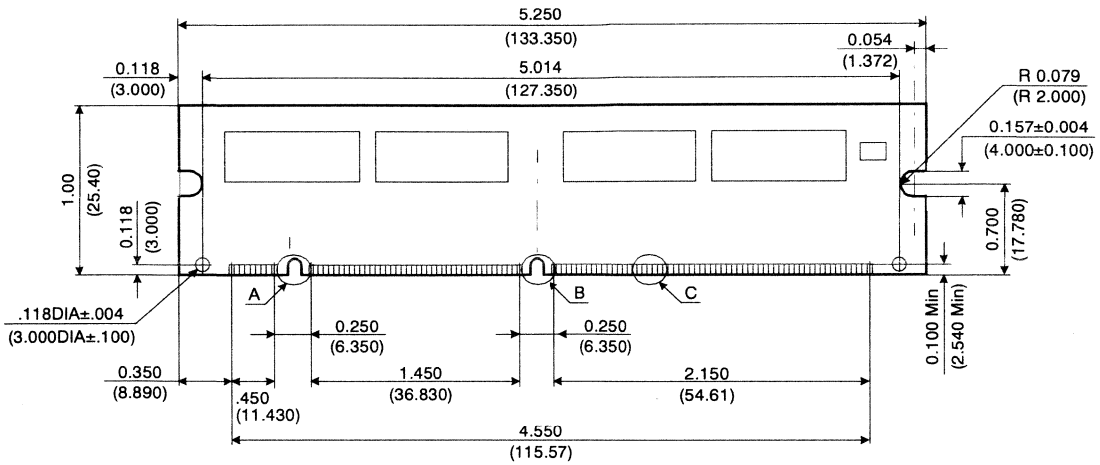
17. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.

18. t_{CHR} is referenced to later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.

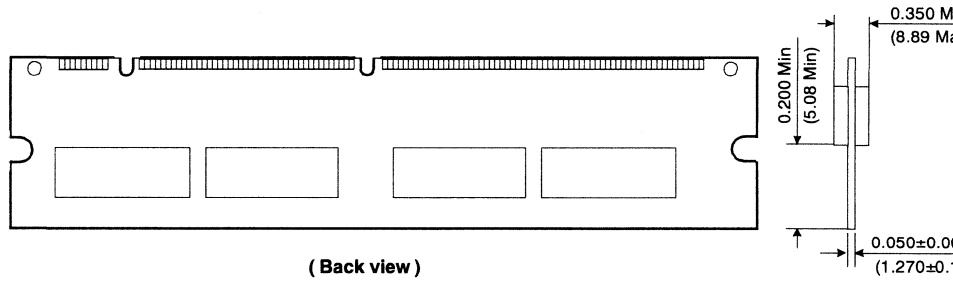
19. t_{DS}, t_{DH} is independently specified for lower byte DIN(0~7), upper byte DIN(8~15).

PACKAGE DIMENSIONS

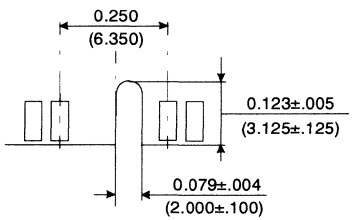
Units : Inches (millimeters)



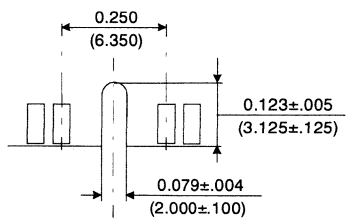
(Front view)



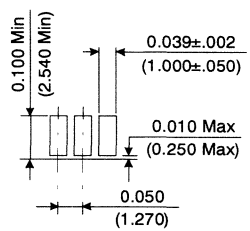
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 1Mx16 DRAM with EDO mode, SOJ
DRAM Part No. : KMM366F224BJ -- KM416V1204BJ

KMM366F203CK & KMM366F213CK EDO Mode without buffer

2M x 64 DRAM DIMM based on 2Mx8, 4K & 2K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM366F20(1)3CK is a 2M bit x 64 Dynamic RAM high density memory module. The Samsung KMM366F20(1)3CK consists of eight CMOS 2Mx8bits DRAMs in SOJ 300mil package and one 1K/2K EEPROM for SPD in 8-pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM366F20(1)3CK is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

FEATURES

- Part Identification
  - KMM366F203CK (4096 cycles/64ms Ref. SOJ)
  - KMM366F213CK (2048 cycles/32ms Ref. SOJ)
- New JEDEC standard proposal without buffer
- Serial Presence Detect with EEPROM
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS1}$	57	DQ18	85	Vss	113	$\overline{CAS5}$	141	DQ50
2	DQ0	30	$\overline{RAS0}$	58	DQ19	86	DQ32	114	*$\overline{RAS1}$	142	DQ51
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ33	115	DU	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	DU	90	Vcc	118	A3	146	DU
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	A11	150	DQ54
11	DQ8	39	*A12	67	DQ23	95	DQ40	123	*A13	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	DU	153	DQ56
14	DQ10	42	DU	70	DQ25	98	DQ42	126	DU	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	$\overline{OE2}$	72	DQ27	100	DQ44	128	DU	156	DQ59
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ45	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS2}$	74	DQ28	102	Vcc	130	$\overline{CAS6}$	158	DQ60
19	DQ14	47	$\overline{CAS3}$	75	DQ29	103	DQ46	131	$\overline{CAS7}$	159	DQ61
20	DQ15	48	$\overline{W2}$	76	DQ30	104	DQ47	132	DU	160	DQ62
21	*CB0	49	Vcc	77	DQ31	105	*CB4	133	Vcc	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	NC	107	Vss	135	NC	163	NC
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	Vcc	54	Vss	82	**SDA	110	Vcc	138	Vss	166	**SA1
27	$\overline{W0}$	55	DQ16	83	**SCL	111	DU	139	DQ48	167	**SA2
28	$\overline{CAS0}$	56	DQ17	84	Vcc	112	$\overline{CAS4}$	140	DQ49	168	Vcc

NOTE : A11 is used for only KMM366F203CK (4K ref.)

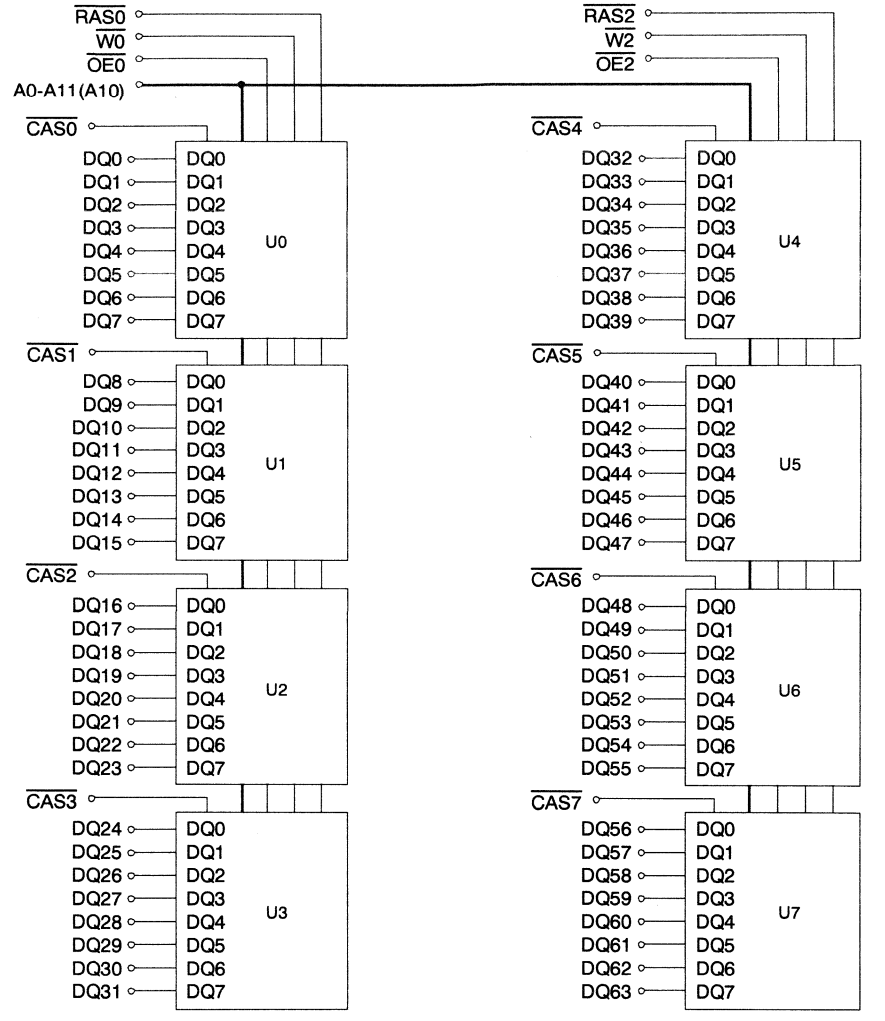
PIN NAMES

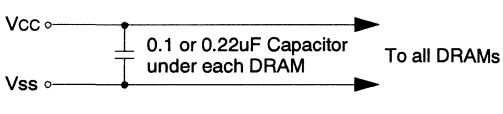
Pin Name	Function
A0 - A11	Address Input(4K ref.)
A0 - A10	Address Input(2K ref.)
DQ0 - DQ63	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Colume Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
DU	Don't use
**SDA	Serial Address /Data I/O
**SCL	Serial Clock
SA0 -SA2	Address in EEPROM
*CB0 - *CB7	Check Bit

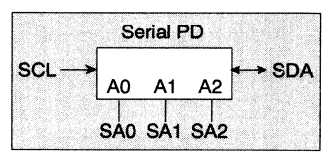
* These pins are not used in this module.

** These pins should be NC in the system which does not support SPD.

FUNCTIONAL BLOCK DIAGRAM







4

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_d	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V at pulse width≤15ns which is measured at V_{CC}.

*2 : -1.3V at pulse width≤15ns which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM366F203CK		KMM366F213CK		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	720	-	880	mA
	-6	-	640	-	800	mA
I_{CC2}	Don't care	-	8	-	8	mA
I_{CC3}	-5	-	720	-	880	mA
	-6	-	640	-	800	mA
I_{CC4}	-5	-	640	-	720	mA
	-6	-	560	-	640	mA
I_{CC5}	Don't care	-	4	-	4	mA
I_{CC6}	-5	-	720	-	880	mA
	-6	-	640	-	800	mA
$I_{I(L)}$	Don't care	-40	40	-40	40	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{I(L)}$: Input Leakage Current (Any input 0 ≤V_{IN}≤V_{CC}+0.3V, all other pins not under test=0 V)

$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT} ≤V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11(A10)]	C_{IN1}	-	50	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	38	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	38	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	17	pF
Input/Output capacitance[DQ0-DQ63]	C_{DQ1}	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	131		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5,14
Access time from column address	t_{AA}		25		30	ns	3,10,14
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3,14
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		ns	3,14
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	15	ns	6,11,12,14
Transition time(rise and fall)	t_T	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	14
$\overline{CAS}$ hold time	t_{CSH}	38		45		ns	14
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	13
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	4,14
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	10,14
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	14
Row address set-up time	t_{ASR}	0		0		ns	14
Row address hold time	t_{RAH}	10		10		ns	14
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	14
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8,14
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	14
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	0		0		ns	9,14
Data hold time	t_{DH}	8		10		ns	9,14
Refresh period(2K Ref.)	t_{REF}		32		32	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ dealy time	t_{CWD}	36		40		ns	7
$\overline{RAS}$ to $\overline{W}$ dealy time	t_{RWD}	73		85		ns	7,14

4

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.0/0.8V$, $V_{oh}/V_{ol}=2.0/0.8V$, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	48		55		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	
$\overline{CAS}$ set-up time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	14
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	14
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	14
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3,14
Hyper page cycle time	t_{HPC}	20		25		ns	12
Hyper page read-modify-write cycle time	t_{HPRWC}	68		77		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	14
$\overline{OE}$ access time	t_{OEA}		13		15	ns	14
$\overline{OE}$ to data delay	t_{OED}	13		15		ns	14
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	13	3	15	ns	6,11,14
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}		10		10	ns	14
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}		10		10	ns	14
Output data hold time	t_{DOH}	5		5		ns	14
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	6.11.12
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	6.11.14
$\overline{W}$ to data delay	t_{WED}	15		15		ns	14
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width(Hyper page cycle)	t_{WPE}	5		5		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF, Voh=2.0V and Vol=0.8V.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non-restrictive operating parameter. They are inclueded in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

   If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above contitions are satisfied, the conition of the data out is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-wirte cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

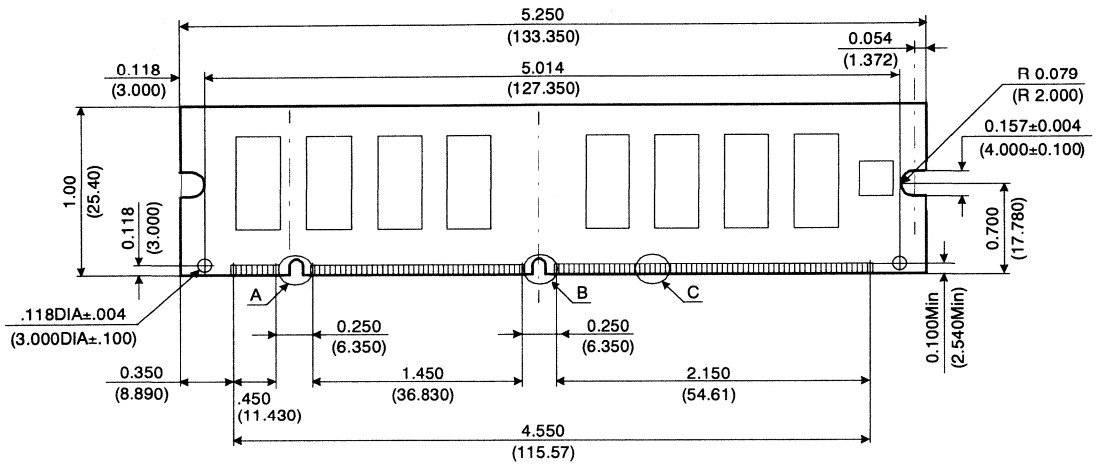
11. t_{CEZ}(max), t_{REZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

12. If $\overline{RAS}$goes to high before $\overline{CAS}$ high going, the open circuit condtion of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condtion of the output is achieved by $\overline{RAS}$ high going.

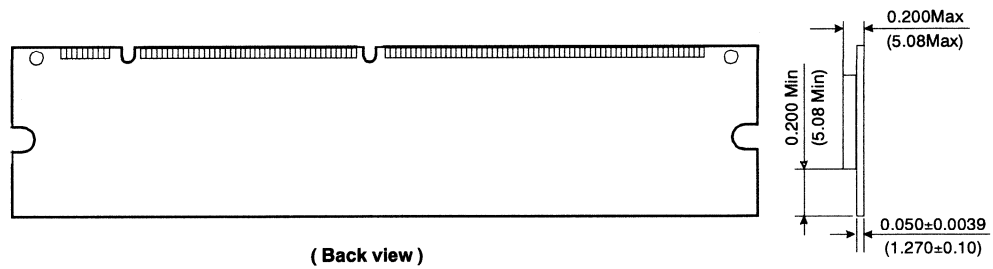
13. $t_{ASC} \geq 6ns$

PACKAGE DIMENSIONS

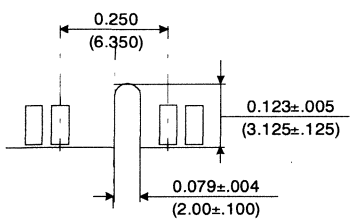
Units : Inches (millimeters)



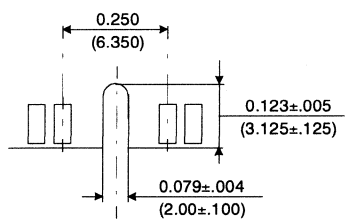
(Front view)



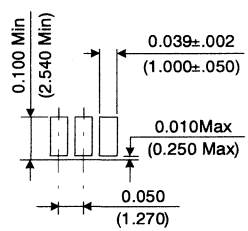
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 DRAM with EDO mode, SOJ
DRAM Part No. : KMM366F203CK - KM48V2004CK
KMM366F213CK - KM48V2104CK

KMM374F224CJ1 EDO Mode without buffer

2M x 72 DRAM DIMM with ECC using 1Mx16 & 1Mx4, Dual Bank, 3.3V

GENERAL DESCRIPTION

The Samsung KMM374F224CJ1 is a 2Mx72bits Dynamic RAM high density memory module. The Samsung KMM374F224CJ1 consists of eight CMOS 1Mx16bits DRAMs in SOJ 400mil package, four CMOS 1Mx4bit DRAMs in SOJ 300mil package and one 1K/2K EEPROM for SPD in 8-pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM374F224CJ1 is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

FEATURES

- Part Identification
  - KMM374F224CJ1(1024 cycles/16ms, SOJ)
- New JEDEC standard proposal without buffer
- Serial Presence Detect with EEPROM
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), Double sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-6	60ns	17ns	104ns	25ns

4

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS1}$	57	DQ18	85	Vss	113	$\overline{CAS5}$	141	DQ50
2	DQ0	30	$\overline{RAS0}$	58	DQ19	86	DQ32	114	$\overline{RAS1}$	142	DQ51
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ33	115	DU	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	DU	90	Vcc	118	A3	146	DU
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	*A10	66	DQ22	94	DQ39	122	*A11	150	DQ54
11	DQ8	39	*A12	67	DQ23	95	DQ40	123	*A13	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	DU	153	DQ56
14	DQ10	42	DU	70	DQ25	98	DQ42	126	DU	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	$\overline{OE2}$	72	DQ27	100	DQ44	128	DU	156	DQ59
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ45	129	$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS2}$	74	DQ28	102	Vcc	130	$\overline{CAS6}$	158	DQ60
19	DQ14	47	$\overline{CAS3}$	75	DQ29	103	DQ46	131	$\overline{CAS7}$	159	DQ61
20	DQ15	48	$\overline{W2}$	76	DQ30	104	DQ47	132	DU	160	DQ62
21	CB0	49	Vcc	77	DQ31	105	CB4	133	Vcc	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	NC	107	Vss	135	NC	163	NC
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	**SA0
26	Vcc	54	Vss	82	**SDA	110	Vcc	138	Vss	166	**SA1
27	$\overline{W0}$	55	DQ16	83	**SCL	111	DU	139	DQ48	167	**SA2
28	$\overline{CAS0}$	56	DQ17	84	Vcc	112	$\overline{CAS4}$	140	DQ49	168	Vcc

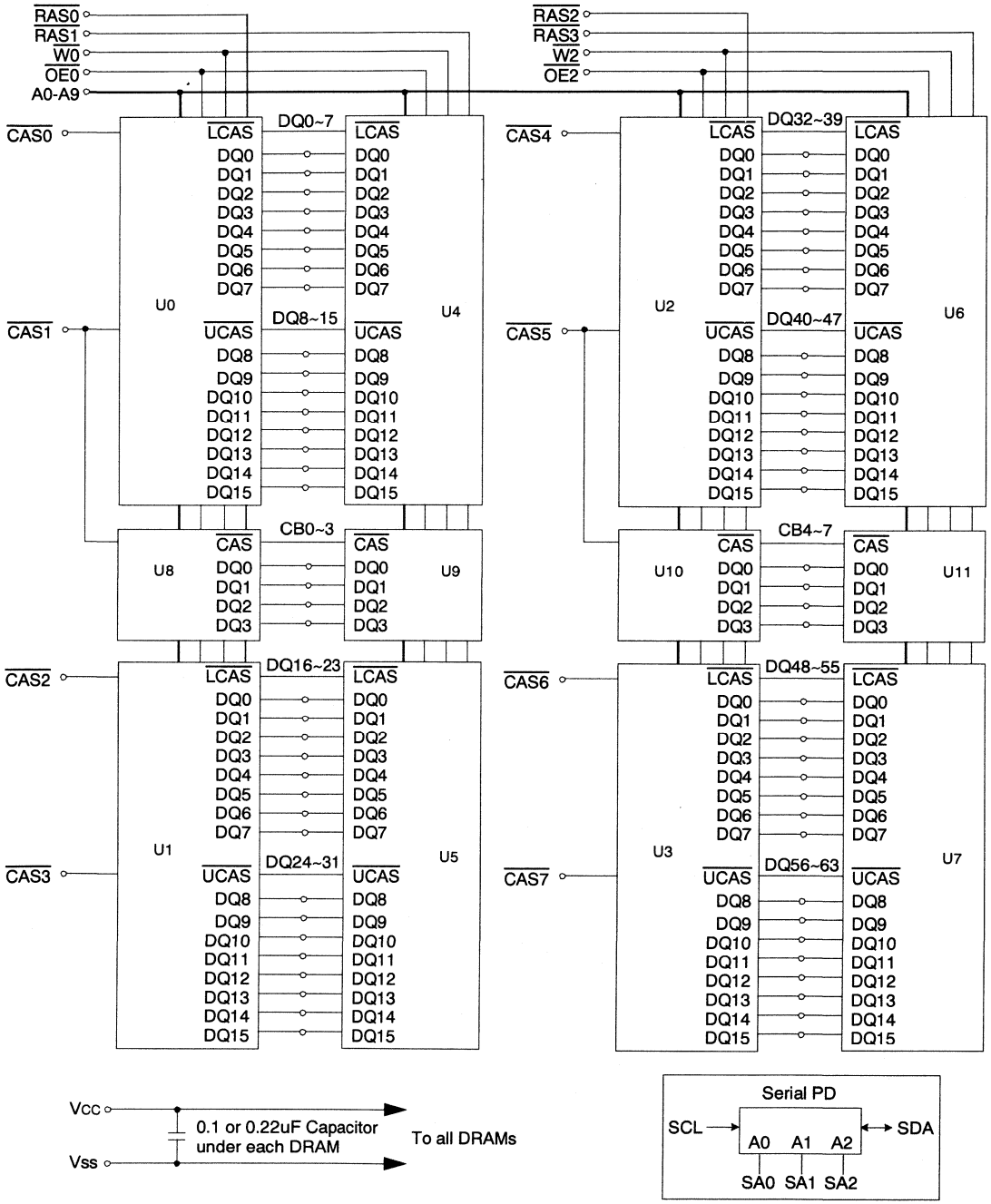
PIN NAMES

Pin Name	Function
A0 - A9	Address Input (1K Ref.)
DQ0 - DQ63	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Colume Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
DU	Don't use
**SDA	Serial Address /Data I/O
**SCL	Serial Clock
SA0 -SA2	Address in EEPROM
CB0 - CB7	Check Bit

* These pins are not used in this module.

** These pins should be NC in the system which does not support SPD.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_d	10.4	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for in tended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V/15ns, Pulse width is measured at V_{CC}.

*2 : -1.3V/15ns, Pulse width is measured at V_{SS}.

4

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM374F224CJ1		Unit
		Min	Max	
I_{CC1}	-6	-	660	mA
I_{CC2}	Don't care	-	20	mA
I_{CC3}	-6	-	660	mA
I_{CC4}	-6	-	500	mA
I_{CC5}	Don't care	-	10	mA
I_{CC6}	-6	-	660	mA
$I_{I(L)}$ $I_{O(L)}$	Don't care	-60 -10	60 10	uA uA
V_{OH} V_{OL}	Don't care	2.4 -	- 0.4	V V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{I(L)}$: Input Leakage Current (Any input 0≤ V_{IN}≤V_{CC}+0.3V, all other pins not under test=0 V)

$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V≤ V_{OUT}≤V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A9]	C_{IN1}	-	70	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	52	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	31	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	38	pF
Input/Output capacitance[DQ0-DQ63, CB0 - CB7]	C_{DQ1}	-	24	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, Output loading C_L=100pF

Parameter	Symbol	-6		Unit	Note
		Min	Max		
Random read or write cycle time	t_{RC}	104		ns	
Read-modify-write cycle time	t_{RWC}	155		ns	
Access time from $\overline{RAS}$	t_{RAC}		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		17	ns	3,4,5
Access time from column address	t_{AA}		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	15	ns	6
Transition time(rise and fall)	t_T	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	17		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	43	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		ns	
Row address set-up time	t_{ASR}	0		ns	
Row address hold time	t_{RAH}	10		ns	
Column address set-up time	t_{ASC}	0		ns	13
Column address hold time	t_{CAH}	10		ns	13
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		ns	
Read command set-up time	t_{RCS}	0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		ns	8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		ns	8
Write command hold time	t_{WCH}	10		ns	
Write command pulse width	t_{WP}	10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10		ns	16
Data set-up time	t_{DS}	0		ns	9,19
Data hold time	t_{DH}	10		ns	9,19
Refresh period (1K Ref.)	t_{REF}		16	ms	
Write command set-up time	t_{WCS}	0		ns	7
$\overline{CAS}$ to $\overline{W}$ dealy time	t_{CWD}	42		ns	7
$\overline{RAS}$ to $\overline{W}$ dealy time	t_{RWD}	85		ns	7

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.2/0.7V$, $V_{oh}/V_{ol}=2.0/0.8V$, Output loading $C_L=100pF$

Parameter	Symbol	-6		Unit	Note
		Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	55		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	60		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		ns	17
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		ns	18
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35	ns	3
Hyper page mode cycle time	t_{HPC}	25		ns	11
Hyper page mode read-modify write cycle time	t_{HPRWC}	77		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	10		ns	14
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		ns	
$\overline{OE}$ access time	t_{OEA}		15	ns	3
$\overline{OE}$ to data delay	t_{OED}	15		ns	
Output buffer turn off delay from $\overline{OE}$	t_{OEZ}	3	15	ns	6
$\overline{OE}$ command hold time	t_{OEH}	15		ns	
Output data hold time	t_{DOH}	5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	15	ns	6,12
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	15	ns	6
$\overline{W}$ to data delay	t_{WED}	15		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	t_{WPE}	5		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL} (max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF, Voh=2.0V and Vol=0.8V.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non-restrictive operating parameter. They are inclueded in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above contitions are satisfied, the condition of the data out is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. $t_{ASC} \geq 6ns$

12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condtion of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condtion of the output is achieved by $\overline{RAS}$ high going.

13. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.

14. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

15. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

16. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

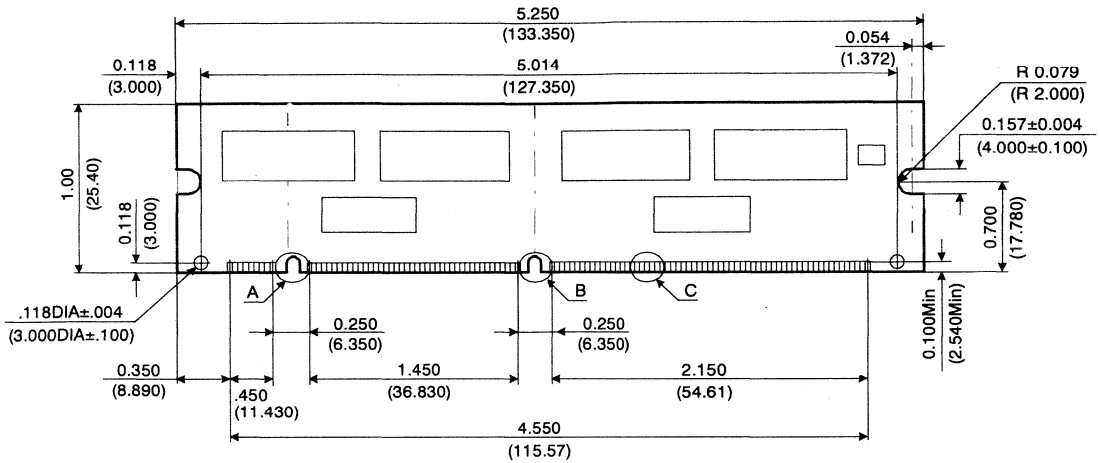
17. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.

18. t_{CHR} is referenced to later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.

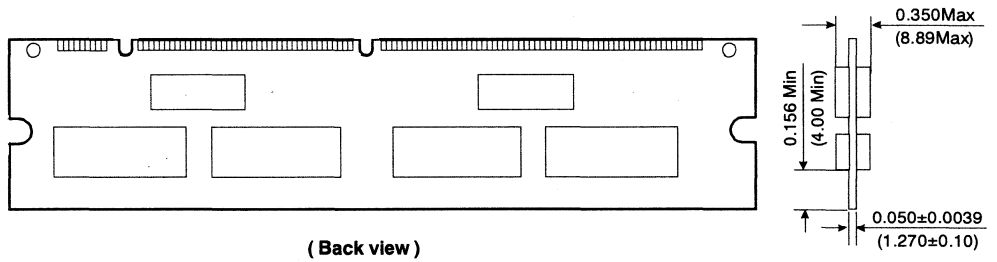
19. t_{DS}, t_{DH} is independently specified for lower byte DIN(0~7), upper byte DIN(8~15).

PACKAGE DIMENSIONS

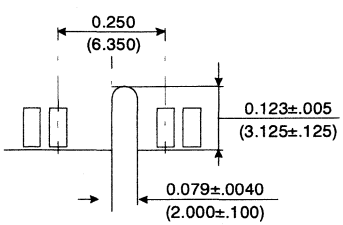
Units : Inches (millimeters)



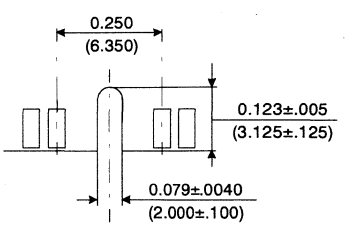
(Front view)



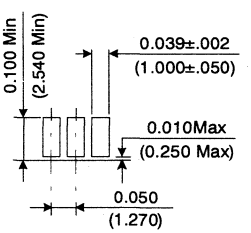
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 1Mx16 DRAM with EDO mode, SOJ and1Mx4 DRAM with EDO mode, SOJ.
DRAM Part No. : KMM374F224CJ1 -- KM416V1204CJ and KM44V1004DJ

KMM374F203CK & KMM374F213CK EDO Mode without buffer

2M x 72 DRAM DIMM with ECC based on 2Mx8, 4K & 2K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM374F20(1)3CK is a 2Mx72bits Dynamic RAM high density memory module. The Samsung KMM374F20(1)CK consists of nine CMOS 2Mx8bits DRAMs in SOJ 300mil package and one 1K/2K EEPROM for SPD in 8-pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM374F20(1)3CK is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

FEATURES

- Part Identification
  -KMM374F203CK (4096 cycles/64ms Ref. SOJ)
  -KMM374F213CK (2048 cycles/32ms Ref. SOJ)
- New JEDEC standard proposal without buffer
- Serial Presence Detect with EEPROM
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), single sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS1}$	57	DQ18	85	Vss	113	$\overline{CAS5}$	141	DQ50
2	DQ0	30	$\overline{RAS0}$	58	DQ19	86	DQ32	114	*$\overline{RAS1}$	142	DQ51
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ33	115	DU	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	DU	90	Vcc	118	A3	146	DU
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	A11	150	DQ54
11	DQ8	39	*A12	67	DQ23	95	DQ40	123	*A13	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	DU	153	DQ56
14	DQ10	42	DU	70	DQ25	98	DQ42	126	DU	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	$\overline{OE2}$	72	DQ27	100	DQ44	128	DU	156	DQ59
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ45	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS2}$	74	DQ28	102	Vcc	130	$\overline{CAS6}$	158	DQ60
19	DQ14	47	$\overline{CAS3}$	75	DQ29	103	DQ46	131	$\overline{CAS7}$	159	DQ61
20	DQ15	48	$\overline{W2}$	76	DQ30	104	DQ47	132	DU	160	DQ62
21	CB0	49	Vcc	77	DQ31	105	CB4	133	Vcc	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	NC	107	Vss	135	NC	163	NC
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	**SA0
26	Vcc	54	Vss	82	**SDA	110	Vcc	138	Vss	166	**SA1
27	$\overline{W0}$	55	DQ16	83	**SCL	111	DU	139	DQ48	167	**SA2
28	$\overline{CAS0}$	56	DQ17	84	Vcc	112	$\overline{CAS4}$	140	DQ49	168	Vcc

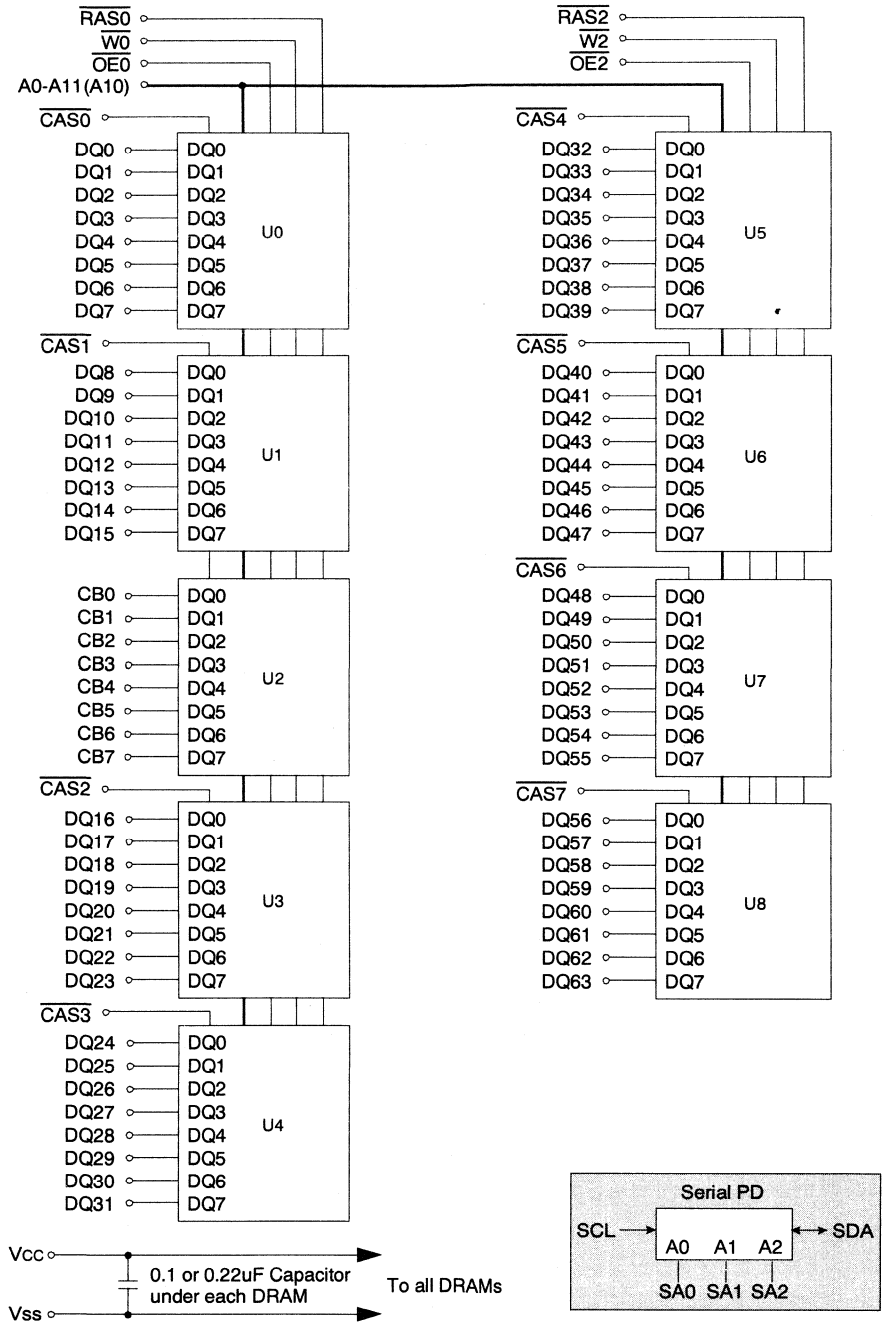
NOTE : A12 is used for only KMM374F203CK (4K ref.)

PIN NAMES

Pin Name	Function
A0 - A11	Address Input(4K ref.)
A0 - A10	Address Input(2K ref.)
DQ0 - DQ63	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Colume Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
DU	Don't use
**SDA	Serial Address /Data I/O
**SCL	Serial Clock
SA0 -SA2	Address in EEPROM
CB0 - CB7	Check Bit

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	9	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for in tended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V at pulse width≤15ns which is measured at V_{CC}.

*2 : -1.3V at pulse width≤15ns which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM374F203CK		KMM374F213CK		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	810	-	990	mA
	-6	-	720	-	900	mA
I_{CC2}	Don't care	-	9	-	9	mA
I_{CC3}	-5	-	810	-	990	mA
	-6	-	720	-	900	mA
I_{CC4}	-5	-	720	-	810	mA
	-6	-	630	-	720	mA
I_{CC5}	Don't care	-	4.5	-	4.5	mA
I_{CC6}	-5	-	810	-	990	mA
	-6	-	720	-	900	mA
$I_{I(L)}$	Don't care	-45	45	-45	45	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{I(L)}$: Input Leakage Current (Any input 0 ≤V_{IN}≤V_{CC}+0.3V, all other pins not under test=0 V)

$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V ≤V_{OUT}≤V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle, t_{HPC}.

CAPACITANCE (TA = 25°C, VCC=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11(A10)]	CIN1	-	55	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	CIN2	-	45	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	CIN3	-	45	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	CIN4	-	24	pF
Input/Output capacitance[DQ0-DQ63, CB0-CB7]	CDQ1	-	17	pF

AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=3.3V±0.3V. See notes 1,2.)

Test condition : Vih/Vil=2.0/0.8V, Voh/Vol=2.0/0.8V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		ns	
Read-modify-write cycle time	tRWC	131		155		ns	
Access time from $\overline{RAS}$	tRAC		50		60	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15	ns	3,4,5,14
Access time from column address	tAA		25		30	ns	3,10,14
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		ns	3,14
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		ns	3,14
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	ns	6,11,12,14
Transition time(rise and fall)	tT	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		ns	14
$\overline{CAS}$ hold time	tCSH	38		45		ns	14
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	ns	13
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	ns	4,14
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	ns	10,14
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		ns	14
Row address set-up time	tASR	0		0		ns	14
Row address hold time	tRAH	10		10		ns	14
Column address set-up time	tASC	0		0		ns	
Column address hold time	tCAH	8		10		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		ns	14
Read command set-up time	tRCS	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		ns	8,14
Write command hold time	tWCH	10		10		ns	
Write command pulse width	tWP	10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		ns	14
Write command to $\overline{CAS}$ lead time	tCWL	8		10		ns	
Data set-up time	tDS	0		0		ns	9,14
Data hold time	tDH	8		10		ns	9,14
Refresh period(2K Ref.)	tREF		32		32	ms	
Write command set-up time	tWCS	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ dealy time	tCWD	36		40		ns	7
$\overline{RAS}$ to $\overline{W}$ dealy time	tRWD	73		85		ns	7,14

4

AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=3.3V±0.3V. See notes 1,2.)

Test condition : Vih/Vil=2.0/0.8V, Voh/Vol=2.0/0.8V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	tAWD	48		55		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	tCPWD	53		60		ns	
$\overline{CAS}$ set-up time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		ns	14
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		ns	14
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		ns	14
Access time from $\overline{CAS}$ precharge	tCPA		28		35	ns	3,14
Hyper page cycle time	tHPC	20		25		ns	12
Hyper page read-modify-write cycle time	tHPRWC	68		77		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	tCP	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		ns	14
$\overline{OE}$ access time	tOEA		13		15	ns	14
$\overline{OE}$ to data delay	tOED	13		15		ns	14
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	ns	6,11,14
$\overline{OE}$ command hold time	tOEH	13		15		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	tWRP		10		10	ns	14
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	tWRH		10		10	ns	14
Output data hold time	tDOH	5		5		ns	14
Output buffer turn off delay time from $\overline{RAS}$	tREZ	3	13	3	15	ns	6.11.12
Output buffer turn off delay time from $\overline{W}$	tWEZ	3	13	3	15	ns	6.11.14
$\overline{W}$ to data delay	tWED	15		15		ns	14
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		ns	
$\overline{W}$ pulse width(Hyper page cycle)	tWPE	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	tPD		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	tPDOFF	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL} (max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF, Voh=2.0V and Vol=0.8V.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non-restrictive operating parameter. They are inclueded in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

   If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above contitions are satisfied, the conition of the data out is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-wirte cycles.

10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

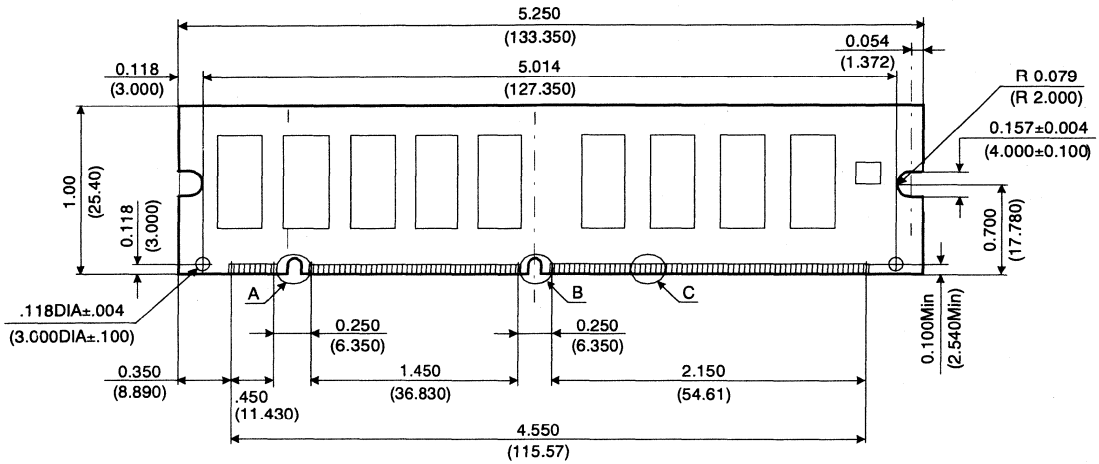
11. t_{CEZ}(max), t_{REZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

12. If $\overline{RAS}$goes to high before $\overline{CAS}$ high going, the open circuit condtion of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condtion of the output is achieved by $\overline{RAS}$ high going.

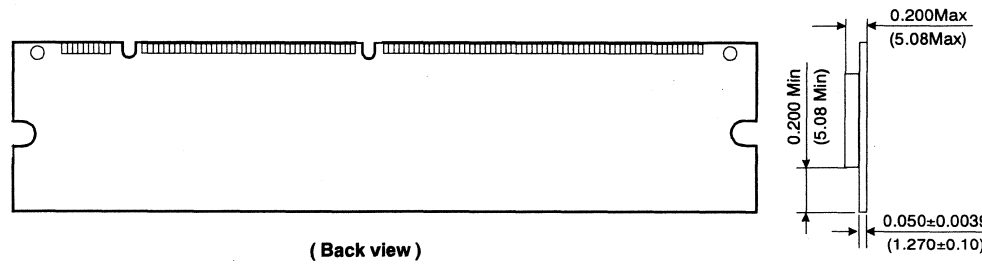
13. $t_{ASC} \geq 6$ns

PACKAGE DIMENSIONS

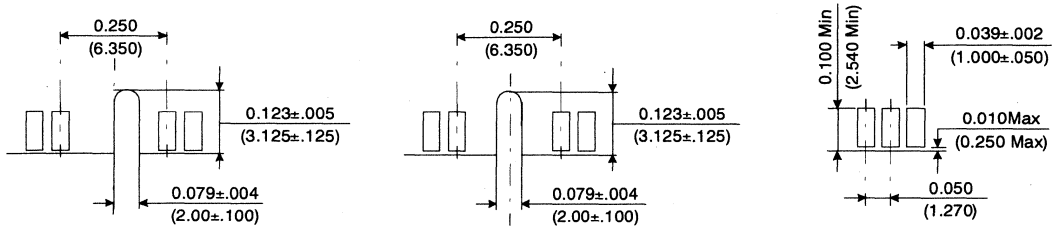
Units : Inches (millimeters)



(Front view)



(Back view)



Detail A **Detail B** **Detail C**

Tolerances : ±.005(.13) unless otherwise specified

The used device is 2Mx8 DRAM with EDO mode, SOJ
DRAM Part No. : KMM374F203CK - KM48V2004CK
KMM374F213CK - KM48V2104CK

KMM366F40(8)4CS1 EDO Mode without buffer

4M x 64 DRAM DIMM Using 4Mx16, 4K & 8K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM366F40(8)4CS1 is a 4Mx64bits Dynamic RAM high density memory module. The Samsung KMM366F40(8)4CS1 consists of four CMOS 4Mx16bits DRAMs in TSOP 400mil packages and one 2K EEPROM for SPD in 8-pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM366F40(8)4CS1 is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM366F404CS1	TSOP	4K	4K/64ms	
KMM366F484CS1	TSOP	8K	4K/64ms	8K/64ms

- New JEDEC standard proposal without buffer
- Serial Presence Detect with EEPROM
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), single sided component

4

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS1}$	57	DQ18	85	Vss	113	$\overline{CAS5}$	141	DQ50
2	DQ0	30	$\overline{RAS0}$	58	DQ19	86	DQ32	114	*$\overline{RAS1}$	142	DQ51
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ33	115	DU	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	DU	90	Vcc	118	A3	146	DU
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	A11	150	DQ54
11	DQ8	39	A12	67	DQ23	95	DQ40	123	*A13	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	DU	153	DQ56
14	DQ10	42	DU	70	DQ25	98	DQ42	126	DU	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	$\overline{OE2}$	72	DQ27	100	DQ44	128	DU	156	DQ59
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ45	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS2}$	74	DQ28	102	Vcc	130	$\overline{CAS6}$	158	DQ60
19	DQ14	47	$\overline{CAS3}$	75	DQ29	103	DQ46	131	$\overline{CAS7}$	159	DQ61
20	DQ15	48	$\overline{W2}$	76	DQ30	104	DQ47	132	DU	160	DQ62
21	*CB0	49	Vcc	77	DQ31	105	*CB4	133	Vcc	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	NC	107	Vss	135	NC	163	NC
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{W0}$	55	DQ16	83	SCL	111	DU	139	DQ48	167	SA2
28	$\overline{CAS0}$	56	DQ17	84	Vcc	112	$\overline{CAS4}$	140	DQ49	168	Vcc

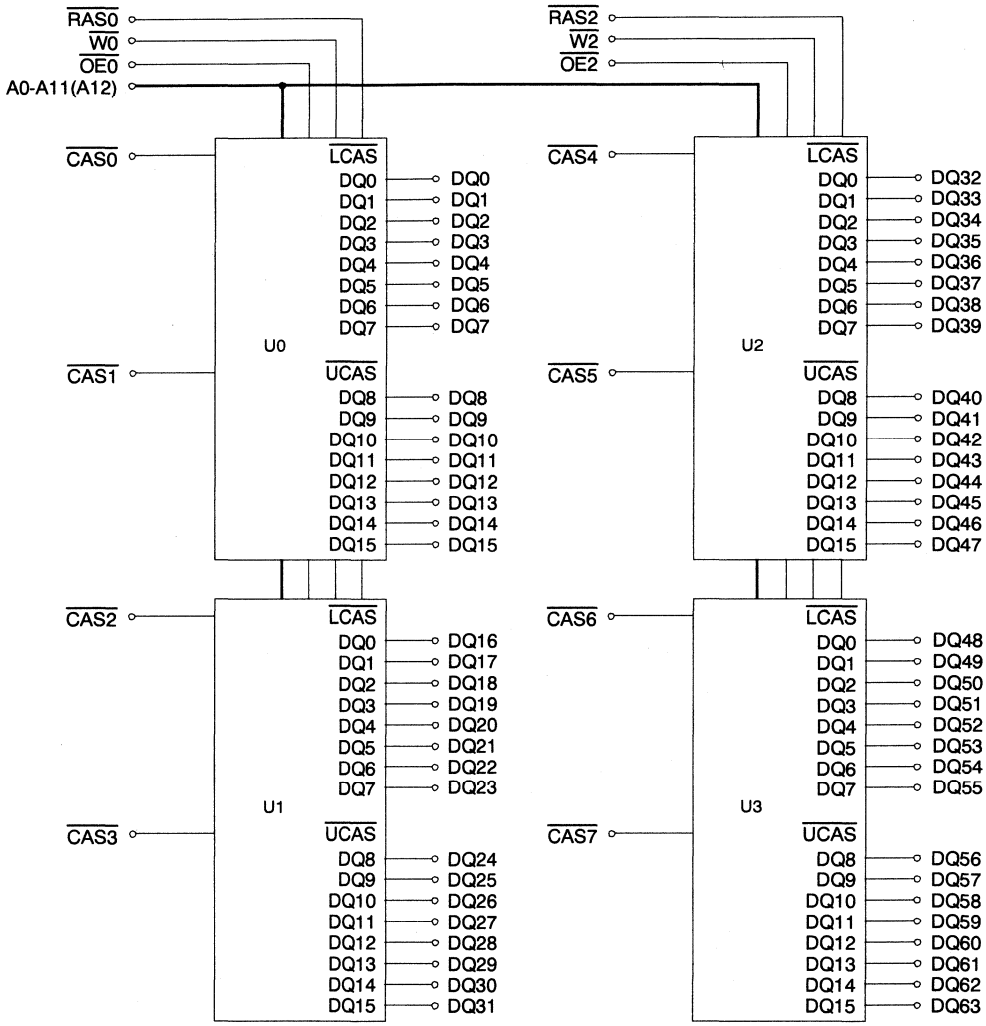
Note : A12 is used for only KMM366F484CS1 (8K ref.)

PIN NAMES

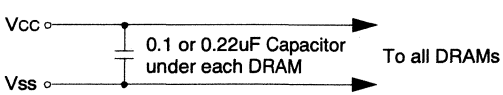
Pin Name	Function
A0 - A11	Address Input (4K ref.)
A0 - A12	Address Input (8K ref.)
DQ0 - DQ63	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
DU	Don't use
SDA	Serial Address /Data I/O
SCL	Serial Clock
SA0 -SA2	Address in EEPROM
*CB0 - CB7	Check Bit

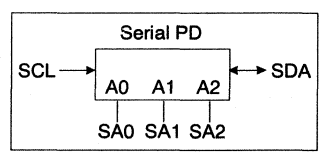
* These pins are not used in this module.

FUNCTIONAL BLOCK DIAGRAM



Note : A12 is used for only KMM366F484CS1 (8K ref.)





ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	4	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for in tended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0*2	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V

*1 : V_{CC}+1.3V at pulse width≤15ns which is measured at V_{CC}.

*2 : -1.3V at pulse width≤15ns which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM366F484CS1		KMM366F404CS1		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	320	-	480	mA
	-6	-	280	-	440	mA
I_{CC2}	Don't care	-	4	-	4	mA
I_{CC3}	-5	-	320	-	480	mA
	-6	-	280	-	440	mA
I_{CC4}	-5	-	360	-	360	mA
	-6	-	320	-	320	mA
I_{CC5}	Don't care	-	2	-	2	mA
I_{CC6}	-5	-	480	-	480	mA
	-6	-	440	-	440	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC} =min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤ V_{IN}≤V_{CC}+0.3V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤ V_{OUT}≤V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC} .

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A12]	C_{IN1}	-	30	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	24	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	24	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	17	pF
Input/Output capacitance[DQ0-DQ63]	CDQ	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading C_L=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	128		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,9
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,9
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	6,12
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	8		10		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		40		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	17	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	12	25	15	30	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	7		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	13
Column address hold time	t_{CAH}	7		10		ns	13
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	7		10		ns	
Write command pulse width	t_{WP}	7		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	8		10		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	7		10		ns	16
Data set-up time	t_{DS}	0		0		ns	
Data hold time	t_{DH}	7		10		ns	
Refresh period (4K & 8K Ref.)	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ dealy time	t_{CWD}	33		38		ns	7, 15
$\overline{RAS}$ to $\overline{W}$ dealy time	t_{RWD}	70		84		ns	7

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.2/0.7V$, $V_{oh}/V_{ol}=2.0/0.8V$, output loading $C_L=100pF$

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	45		53		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	47		58		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	17
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3
Hyper page mode cycle time	t_{HPC}	20		25		ns	10
Hyper page mode read-modify write cycle time	t_{HPRWC}	67		73		ns	10
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	7		10		ns	14
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{OE}$ access time	t_{OEA}		13		15	ns	
$\overline{OE}$ to data delay	t_{OED}	10		13		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	13	3	13	ns	6
$\overline{OE}$ command hold time	t_{OEH}	5		5		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	13	ns	6,12
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	13	ns	6
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non-restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above contitions are satisfied, The condition of the data out is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.

10. $t_{ASC} \geq 6$ns, Assume t_T = 2.0ns

11. For all of the refresh mode except distributed $\overline{CAS}$-before $\overline{RAS}$ refresh, 4096 cycle of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification.

12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condtion of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condtion of the output is achieved by $\overline{RAS}$ high going.

13. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.

14. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

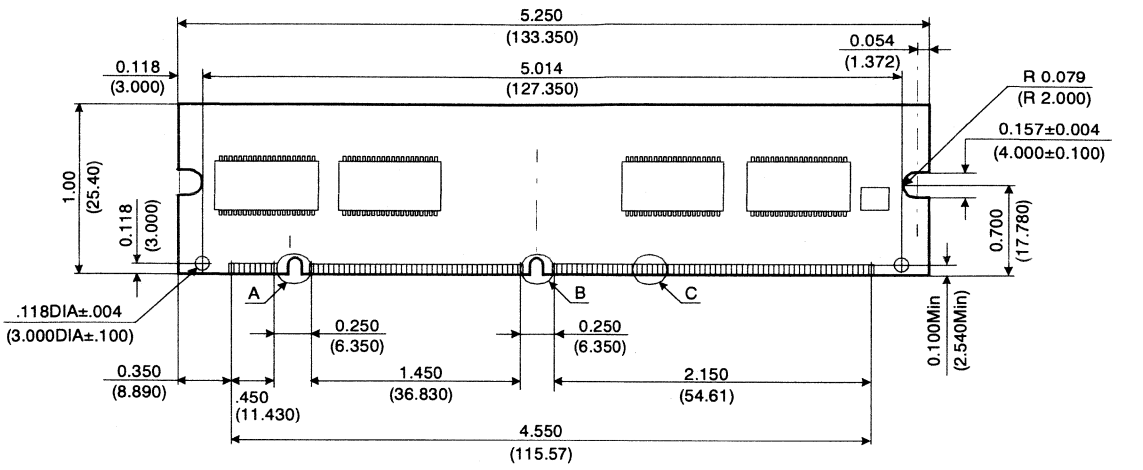
15. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

16. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

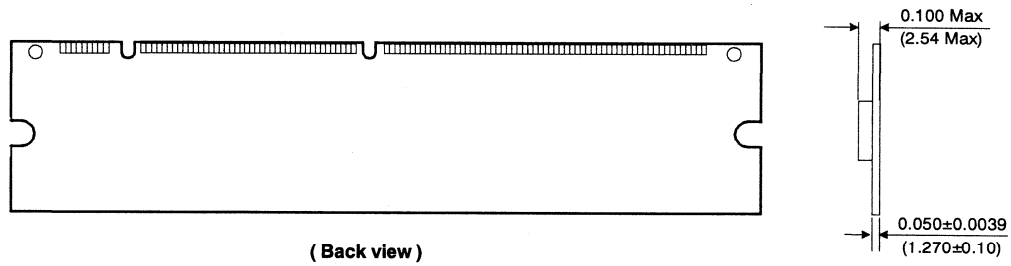
17. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.

PACKAGE DIMENSIONS

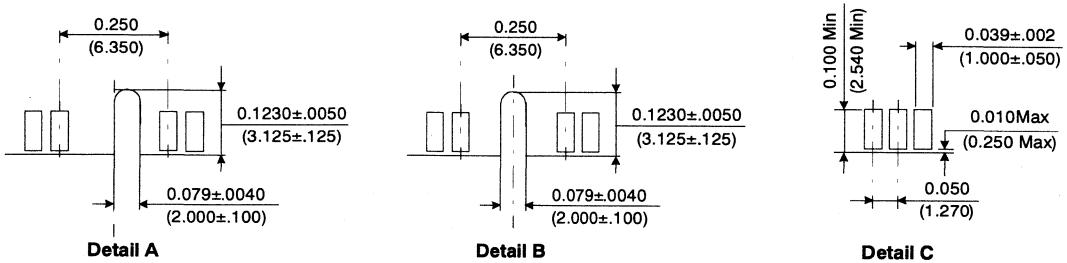
Units : Inches (millimeters)



(Front view)



(Back view)



Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 DRAM with EDO mode, TSOP II
DRAM Part No. : KMM366F404CS1 - KM416V4104CS
KMM366F484CS1 - KM416V4004CS

KMM374F404CS1 EDO Mode without buffer

4M x 72 DRAM DIMM with ECC Using 4Mx16 & 4Mx4, 4K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM374F404CS1 is a 4Mx72bits Dynamic RAM high density memory module. The Samsung KMM374F404CS1 consists of four CMOS 4Mx16bits DRAMs and two CMOS 4Mx4bits DRAMs in TSOP 300mil package and one 2K EEPROM for SPD in 8-pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM374F404CS1 is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

FEATURES

- Part Identification
  - KMM374F404CS1(4096 cycles/64ms, TSOP)
- New JEDEC standard proposal without buffer
- Serial Presence Detect with EEPROM
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), single sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

PIN CONFIGURATIONS

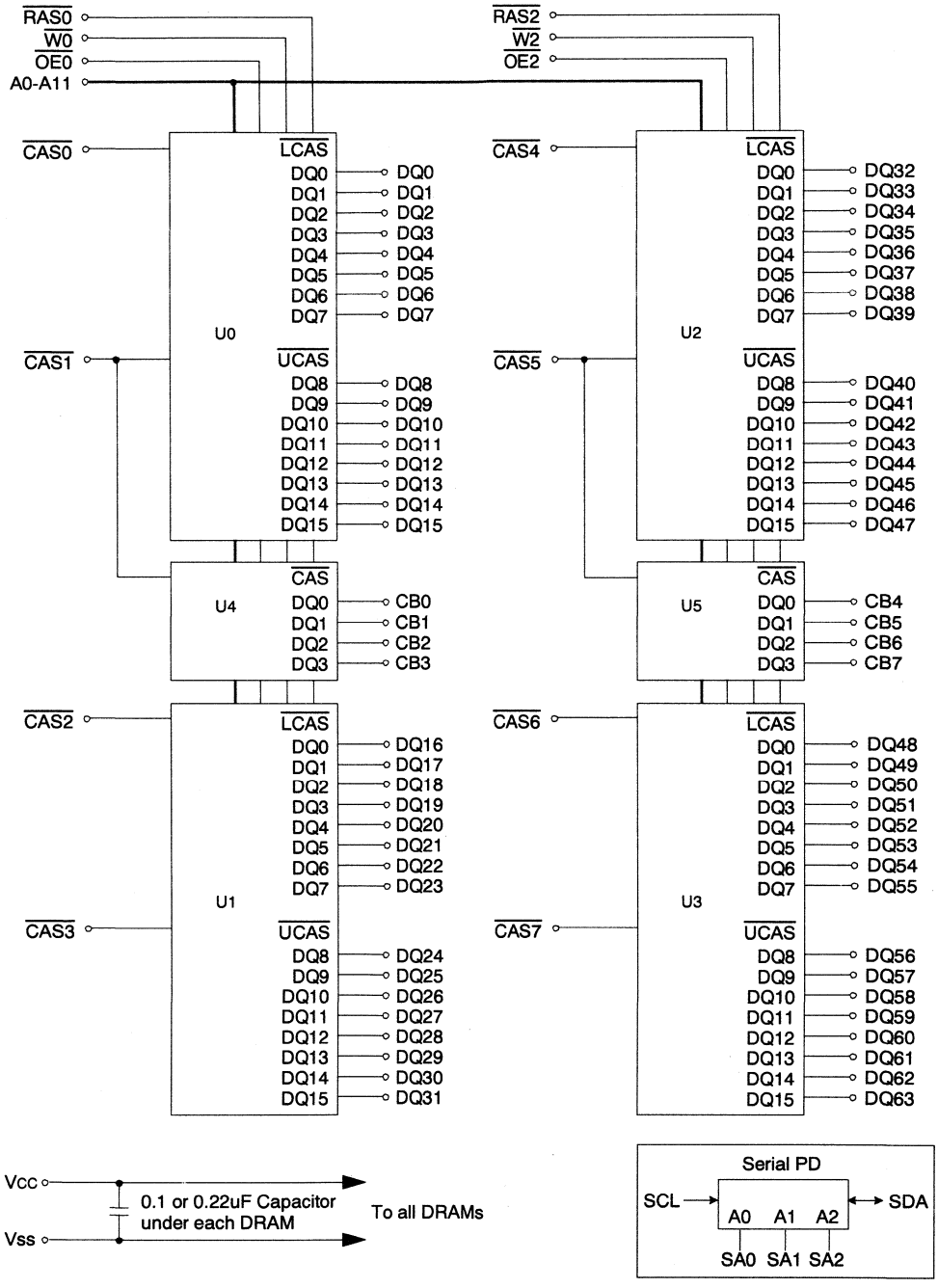
Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS1}$	57	DQ18	85	Vss	113	$\overline{CAS5}$	141	DQ50
2	DQ0	30	$\overline{RAS0}$	58	DQ19	86	DQ32	114	*$\overline{RAS1}$	142	DQ51
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ33	115	DU	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	DU	90	Vcc	118	A3	146	DU
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	A11	150	DQ54
11	DQ8	39	*A12	67	DQ23	95	DQ40	123	*A13	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	DU	153	DQ56
14	DQ10	42	DU	70	DQ25	98	DQ42	126	DU	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	$\overline{OE2}$	72	DQ27	100	DQ44	128	DU	156	DQ59
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ45	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS2}$	74	DQ28	102	Vcc	130	$\overline{CAS6}$	158	DQ60
19	DQ14	47	$\overline{CAS3}$	75	DQ29	103	DQ46	131	$\overline{CAS7}$	159	DQ61
20	DQ15	48	$\overline{W2}$	76	DQ30	104	DQ47	132	DU	160	DQ62
21	CB0	49	Vcc	77	DQ31	105	CB4	133	Vcc	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	NC	107	Vss	135	NC	163	NC
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{W0}$	55	DQ16	83	SCL	111	DU	139	DQ48	167	SA2
28	$\overline{CAS0}$	56	DQ17	84	Vcc	112	$\overline{CAS4}$	140	DQ49	168	Vcc

PIN NAMES

Pin Name	Function
A0 - A11	Address Input
DQ0 - DQ63	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
DU	Don't use
SDA	Serial Address /Data I/O
SCL	Serial Clock
SA0 -SA2	Address in EEPROM
CB0 - CB7	Check Bit

* These pins are not used in this module.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_d	6	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for in tended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V at pulse width ≤15ns which is measured at V_{CC}.

*2 : -1.3V at pulse width ≤ 15ns which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM374F404CS1		Unit
		Min	Max	
I_{CC1}	-5	-	660	mA
	-6	-	600	mA
I_{CC2}	Don't care	-	6	mA
I_{CC3}	-5	-	660	mA
	-6	-	600	mA
I_{CC4}	-5	-	520	mA
	-6	-	460	mA
I_{CC5}	Don't care	-	3	mA
I_{CC6}	-5	-	660	mA
	-6	-	600	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-5	5	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0 ≤V_{IN}≤V_{CC}+0.3V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V ≤V_{OUT}≤V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC} .

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	40	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	31	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	31	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	24	pF
Input/Output capacitance[DQ0-DQ63, CB0-CB7]	CDQ	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	128		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5,13
Access time from column address	t_{AA}		25		30	ns	3,10,13
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3,13
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		ns	3,13
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	6,11,13
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	8		10		ns	13
$\overline{CAS}$ hold time	t_{CSH}	38		40		ns	13
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	17	37	20	45	ns	4,13
$\overline{RAS}$ to column address delay time	t_{RAD}	12	25	15	30	ns	10,13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	13
Row address set-up time	t_{ASR}	0		0		ns	13
Row address hold time	t_{RAH}	7		10		ns	13
Column address set-up time	t_{ASC}	0		0		ns	14
Column address hold time	t_{CAH}	7		10		ns	14
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	13
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8,13
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	7		10		ns	
Write command pulse width	t_{WP}	7		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	8		10		ns	13
Write command to $\overline{CAS}$ lead time	t_{CWL}	7		10		ns	17
Data set-up time	t_{DS}	0		0		ns	9,13
Data hold time	t_{DH}	7		10		ns	9,13
Refresh period	t_{REF}		64		64	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	33		38		ns	7,16
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	70		84		ns	7,13

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=3.3V±0.3V. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	45		53		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	47		58		ns	
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	13,18
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	13
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3,13
Hyper page cycle time	t_{HPC}	20		25		ns	12
Hyper page read-modify-write cycle time	t_{HPRWC}	67		73		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	7		10		ns	15
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}		15		15	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}		25		30	ns	13
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	50	200K	60	200K	ns	13
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	30		35		ns	13
$\overline{OE}$ access time	t_{OEA}		13		15	ns	13
$\overline{OE}$ to data delay	t_{OED}	10		13		ns	13
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	13	3	13	ns	13
$\overline{OE}$ command hold time	t_{OEH}	5		5		ns	
Output data hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{DOH}	5		5		ns	13
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	13	3	13	ns	6,11
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	3	13	3	13	ns	6,13
$\overline{W}$ to data delay	t_{WED}	15		15		ns	13
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non-restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above contitions are satisfied, The condition of the data out is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.

10. $t_{ASC} \geq 6$ns, Assume t_T = 2.0ns.

11. For all of the refresh mode except distributed $\overline{CAS}$-before $\overline{RAS}$ refresh, 4096 cycle of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification.

12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condtion of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condtion of the output is achieved by $\overline{RAS}$ high going.

13. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.

14. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

15. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

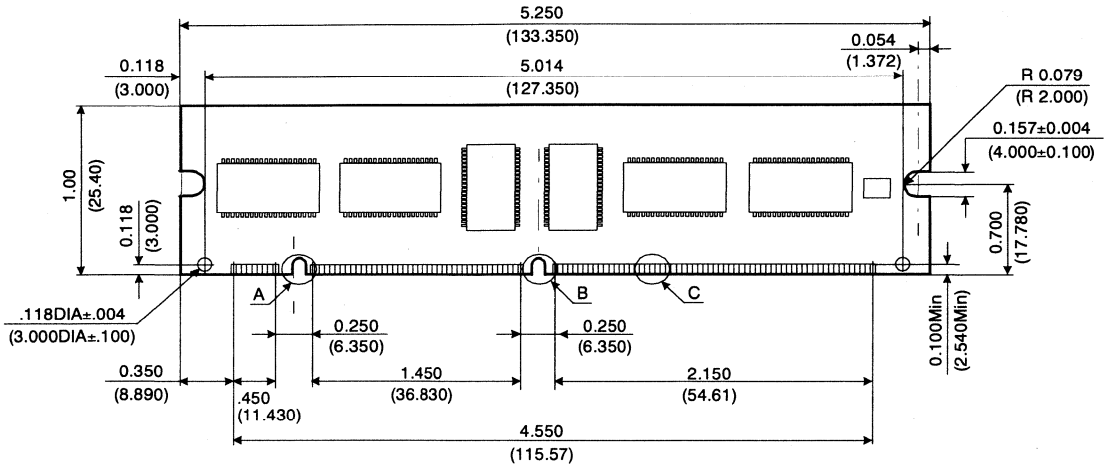
16. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

17. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.

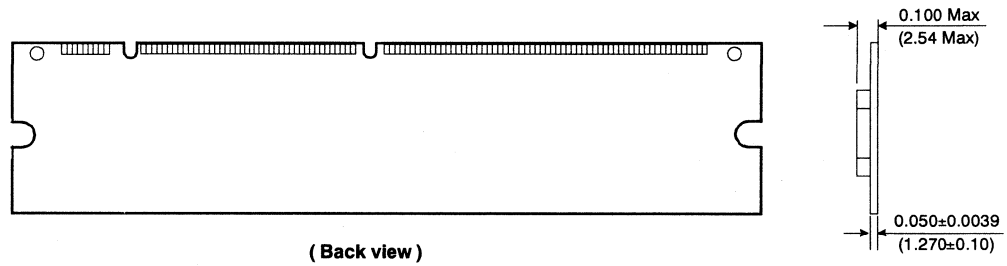
4

PACKAGE DIMENSIONS

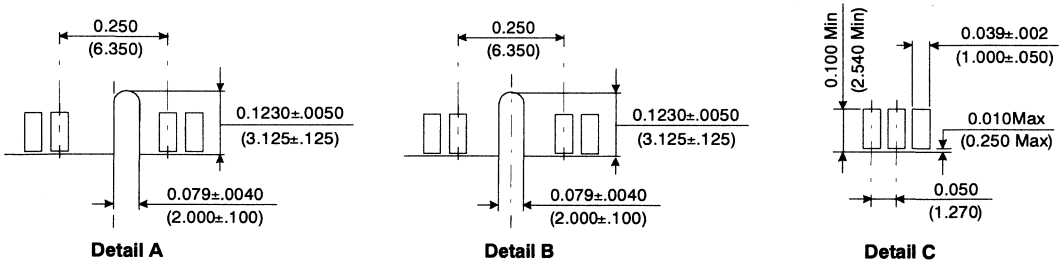
Units : Inches (millimeters)



(Front view)



(Back view)



Tolerances :±.005(.13) unless otherwise specified

The used device is 4Mx16 and 4Mx4 DRAM with EDO mode, TSOPII
DRAM Part No. : KMM374F404CS1 - KM416V4104CS
- KM44V4004CS

KMM366F80(8)3CK2 EDO Mode without buffer

8M x 64 DRAM DIMM Using 8Mx8, 8K & 4K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM366F80(8)3CK2 is a 8Mx64bits Dynamic RAM high density memory module. The Samsung KMM366F80(8)3CK2 consists of eight CMOS 8Mx8bits DRAMs in SOJ 400mil packages and one 2K EEPROM for SPD in 8-pin SOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM366F80(8)3CK2 is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	tRAC	tCAC	tRC	tHPC
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR ref.	ROR ref.
KMM366F803CK2	SOJ	4K	4K/64ms	
KMM366F883CK2	SOJ	8K	4K/64ms	8K/64ms

- New JEDEC standard proposal without buffer
- Serial Presence Detect with EEPROM
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), single sided component

4

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS1}$	57	DQ18	85	Vss	113	$\overline{CAS5}$	141	DQ50
2	DQ0	30	$\overline{RAS0}$	58	DQ19	86	DQ32	114	*$\overline{RAS1}$	142	DQ51
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ33	115	DU	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	DU	90	Vcc	118	A3	146	DU
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	A11	150	DQ54
11	DQ8	39	A12	67	DQ23	95	DQ40	123	*A13	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	DU	153	DQ56
14	DQ10	42	DU	70	DQ25	98	DQ42	126	DU	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	$\overline{OE2}$	72	DQ27	100	DQ44	128	DU	156	DQ59
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ45	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS2}$	74	DQ28	102	Vcc	130	$\overline{CAS6}$	158	DQ60
19	DQ14	47	$\overline{CAS3}$	75	DQ29	103	DQ46	131	$\overline{CAS7}$	159	DQ61
20	DQ15	48	$\overline{W2}$	76	DQ30	104	DQ47	132	DU	160	DQ62
21	*CB0	49	Vcc	77	DQ31	105	*CB4	133	Vcc	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	NC	107	Vss	135	NC	163	NC
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{W0}$	55	DQ16	83	SCL	111	$\overline{DU}$	139	DQ48	167	SA2
28	$\overline{CAS0}$	56	DQ17	84	Vcc	112	$\overline{CAS4}$	140	DQ49	168	Vcc

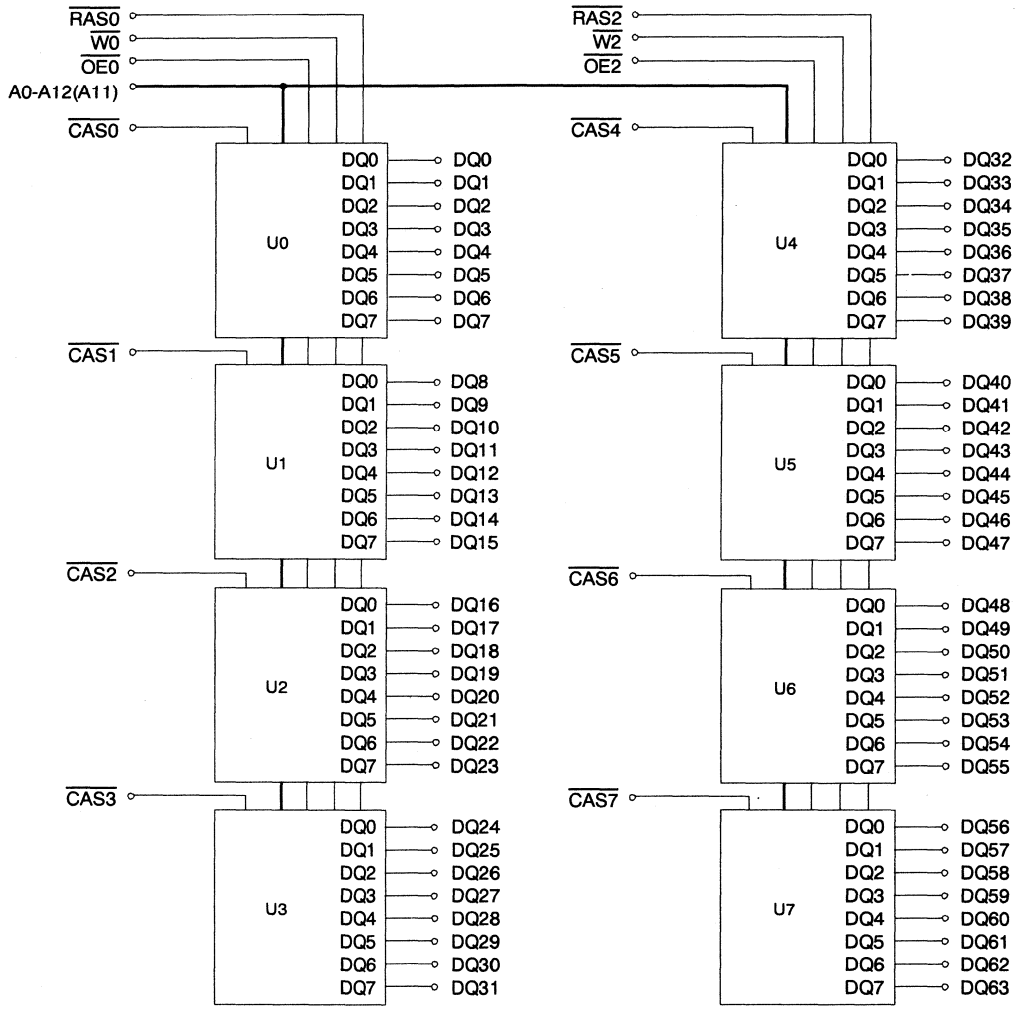
NOTE : A12 is used for only KMM366F883CK2 (8K ref.)

PIN NAMES

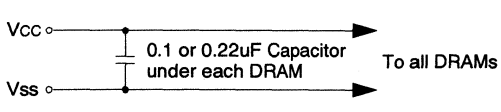
Pin Name	Function
A0 - A11	Address Input(4K ref.)
A0 - A12	Address Input(8K ref.)
DQ0 - DQ63	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
DU	Don't use
SDA	Serial Address /Data I/O
SCL	Serial Clock
SA0 -SA2	Address in EEPROM
*CB0 - CB7	Check Bit

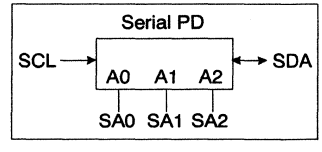
* These pins are not used in this module.

FUNCTIONAL BLOCK DIAGRAM



Note : A12 is used for only KMM366F883CK2 (8K ref.)





ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_d	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for in tended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V at pulse width≤15ns which is measured at V_{CC}.

*2 : -1.3V at pulse width≤15ns which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM366F883CK2		KMM366F803CK2		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	640	-	880	mA
	-6	-	560	-	800	mA
I_{CC2}	Don't care	-	8	-	8	mA
I_{CC3}	-5	-	640	-	880	mA
	-6	-	560	-	800	mA
I_{CC4}	-5	-	720	-	720	mA
	-6	-	640	-	640	mA
I_{CC5}	Don't care	-	4	-	4	mA
I_{CC6}	-5	-	880	-	880	mA
	-6	-	800	-	800	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.3V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC} .

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A12]	C_{IN1}	-	50	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	38	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	38	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	17	pF
Input/Output capacitance[DQ0-DQ63]	CDQ1	-	17	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	128		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5,13
Access time from column address	t_{AA}		25		30	ns	3,10,13
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3,13
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		ns	3,13
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	6,11,13
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	8		10		ns	13
$\overline{CAS}$ hold time	t_{CSH}	38		40		ns	13
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	17	37	20	45	ns	4,13
$\overline{RAS}$ to column address delay time	t_{RAD}	12	25	15	30	ns	10,13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	13
Row address set-up time	t_{ASR}	0		0		ns	13
Row address hold time	t_{RAH}	7		10		ns	13
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	7		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	13
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8,13
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	7		10		ns	
Write command pulse width	t_{WP}	7		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	8		10		ns	13
Write command to $\overline{CAS}$ lead time	t_{CWL}	7		10		ns	
Data set-up time	t_{DS}	0		0		ns	9,13
Data hold time	t_{DH}	7		10		ns	9,13
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	33		38		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	70		84		ns	7,13

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	45		53		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	47		58		ns	
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	13
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	13
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3,13
Hyper page cycle time	t_{HPC}	20		25		ns	12
Hyper page read-modify-write cycle time	t_{HPRWC}	67		73		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	7		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	13
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	13
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	13
$\overline{OE}$ access time	t_{OEA}		13		15	ns	13
$\overline{OE}$ to data delay	t_{OED}	10		13		ns	13
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	13	3	13	ns	13
$\overline{OE}$ command hold time	t_{OEH}	5		5		ns	
Output data hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{DOH}	5		5		ns	13
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	13	3	13	ns	6,11
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	3	13	3	13	ns	6,13
$\overline{W}$ to data delay	t_{WED}	15		15		ns	13
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non-restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above contitions are satisfied, The condition of the data out is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

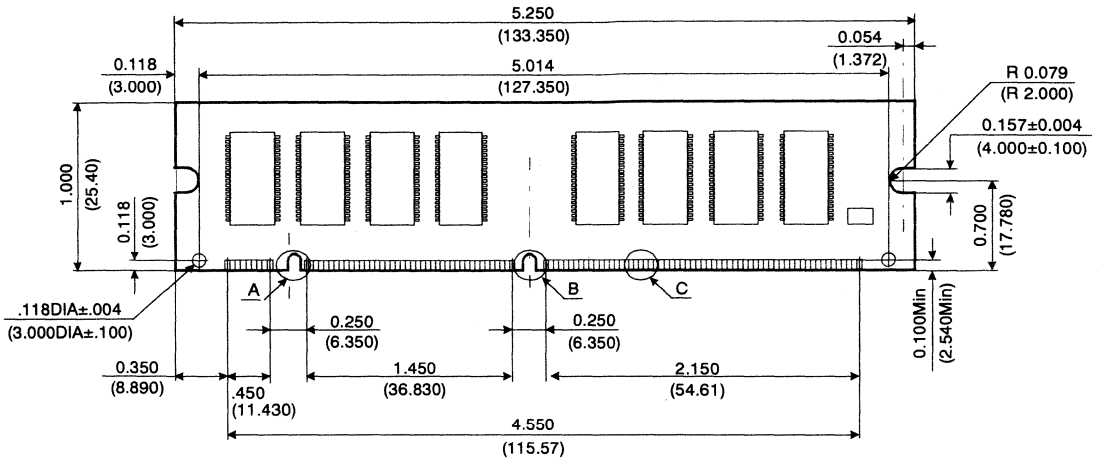
9. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.

10. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condtion of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condtion of the output is achieved by $\overline{RAS}$ high going.

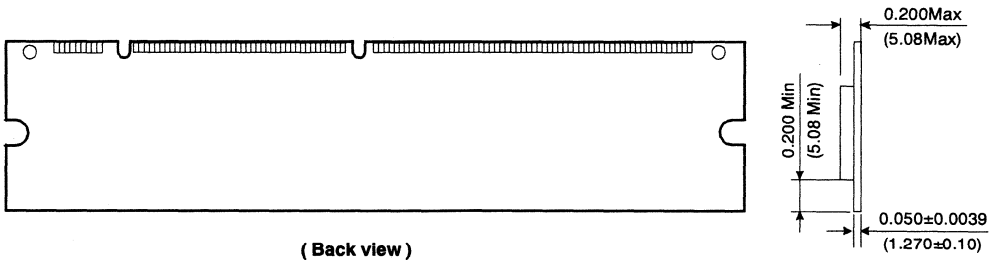
11. $t_{ASC} \geq 6ns$

PACKAGE DIMENSIONS

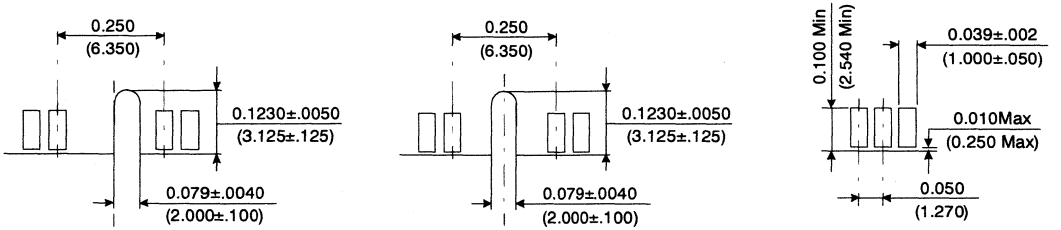
Units : Inches (millimeters)



(Front view)



(Back view)



Detail A **Detail B** **Detail C**

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 DRAM with EDO mode, SOJ
DRAM Part No. : KMM366F883CK2 - KM48V8004CK
KMM366F803CK2 - KM48V8104CK

KMM366F80(8)4CS1 EDO Mode without buffer

8M x 64 DRAM DIMM Using 4Mx16, 8K & 4K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM366F80(8)4CS1 is a 8Mx64bits Dynamic RAM high density memory module. The Samsung KMM366F80(8)4CS1 consists of eight CMOS 4Mx16bits DRAMs in TSOP 400mil packages and one 2K EEPROM for SPD in 8-pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM366F80(8)4CS1 is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	tRAC	tCAC	tRC	tHPC
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM366F804CS1	TSOP	4K	4K/64ms	
KMM366F884CS1	TSOP	8K	4K/64ms	8K/64ms

- New JEDEC standard proposal without buffer
- Serial Presence Detect with EEPROM
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS1}$	57	DQ18	85	Vss	113	$\overline{CAS5}$	141	DQ50
2	DQ0	30	$\overline{RAS0}$	58	DQ19	86	DQ32	114	$\overline{RAS1}$	142	DQ51
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ33	115	DU	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	DU	90	Vcc	118	A3	146	DU
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	A11	150	DQ54
11	DQ8	39	A12	67	DQ23	95	DQ40	123	*A13	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	DU	153	DQ56
14	DQ10	42	DU	70	DQ25	98	DQ42	126	DU	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	$\overline{OE2}$	72	DQ27	100	DQ44	128	DU	156	DQ59
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ45	129	$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS2}$	74	DQ28	102	Vcc	130	$\overline{CAS6}$	158	DQ60
19	DQ14	47	$\overline{CAS3}$	75	DQ29	103	DQ46	131	$\overline{CAS7}$	159	DQ61
20	DQ15	48	$\overline{W2}$	76	DQ30	104	DQ47	132	DU	160	DQ62
21	*CB0	49	Vcc	77	DQ31	105	*CB4	133	Vcc	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	NC	107	Vss	135	NC	163	NC
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{W0}$	55	DQ16	83	SCL	111	DU	139	DQ48	167	SA2
28	$\overline{CAS0}$	56	DQ17	84	Vcc	112	$\overline{CAS4}$	140	DQ49	168	Vcc

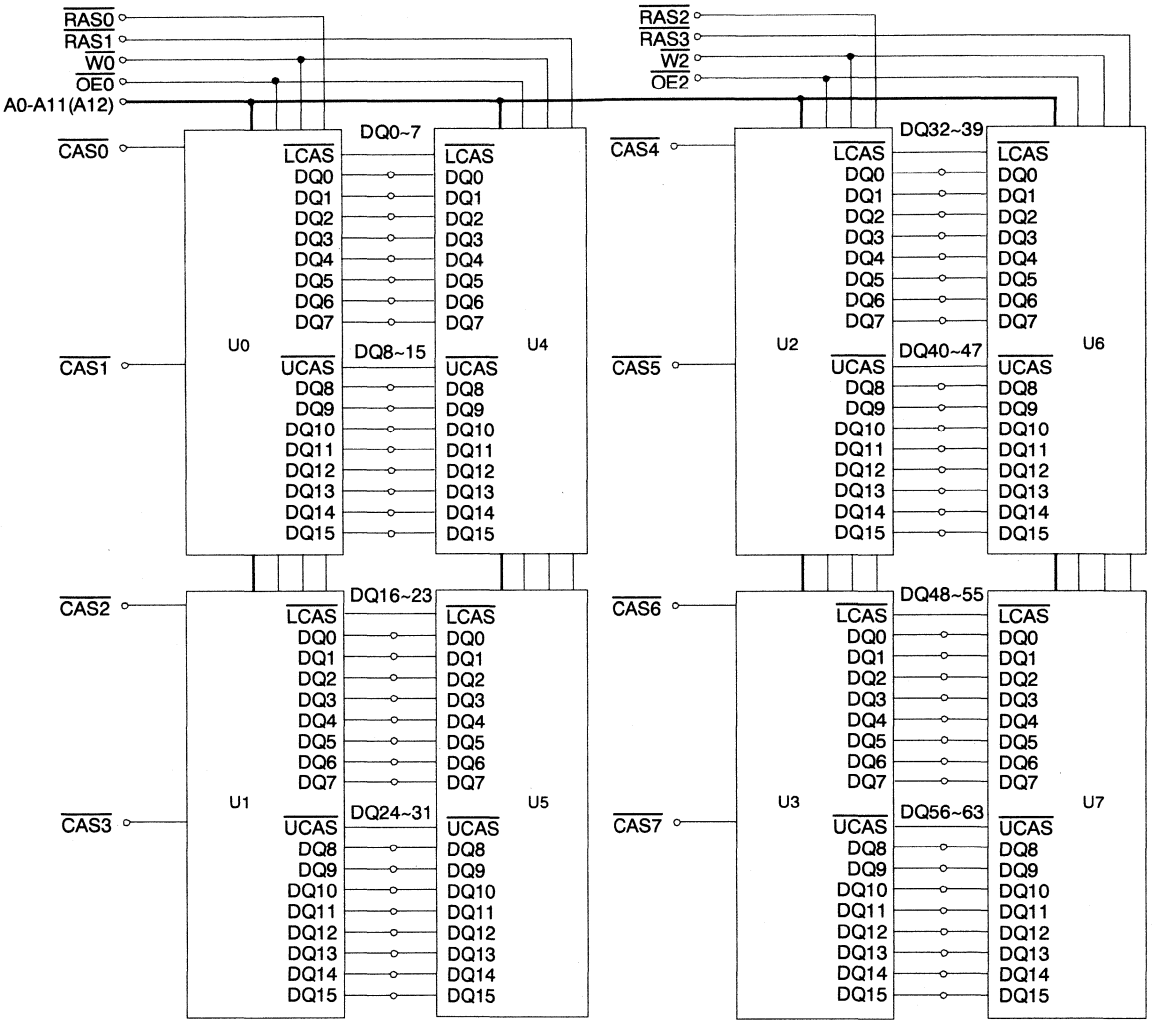
Note : A12 is used for only KMM366F884CS1 (8K ref.)

PIN NAMES

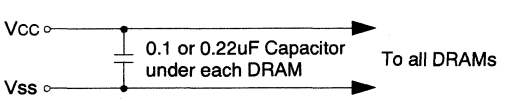
Pin Name	Function
A0 - A11	Address Input (4K ref.)
A0 - A12	Address Input (8K ref.)
DQ0 - DQ63	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
DU	Don't use
SDA	Serial Address /Data I/O
SCL	Serial Clock
SA0 -SA2	Address in EEPROM
*CB0 - CB7	Check Bit

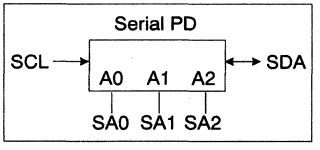
* These pins are not used in this module.

FUNCTIONAL BLOCK DIAGRAM



Note : A12 is used for only KMM366F884CS1 (8K ref.)





ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_d	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V at pulse width≤15ns which is measured at V_{CC}.

*2 : -1.3V at pulse width≤15ns which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM366F884CS1		KMM366F804CS1		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	324	-	484	mA
	-6	-	284	-	444	mA
I_{CC2}	Don't care	-	8	-	8	mA
I_{CC3}	-5	-	324	-	484	mA
	-6	-	284	-	444	mA
I_{CC4}	-5	-	364	-	364	mA
	-6	-	324	-	324	mA
I_{CC5}	Don't care	-	4	-	4	mA
I_{CC6}	-5	-	484	-	484	mA
	-6	-	444	-	444	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-10	10	-10	10	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤ V_{IN}≤V_{CC}+0.3V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤ V_{OUT}≤V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A12]	C_{IN1}	-	50	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	38	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	24	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	24	pF
Input/Output capacitance[DQ0-DQ63]	CDQ	-	24	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading C_L=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	128		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,9
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,9
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	6,12
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	8		10		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		40		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	17	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	12	25	15	30	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	7		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	13
Column address hold time	t_{CAH}	7		10		ns	13
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	7		10		ns	
Write command pulse width	t_{WP}	7		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	8		10		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	7		10		ns	16
Data set-up time	t_{DS}	0		0		ns	
Data hold time	t_{DH}	7		10		ns	
Refresh period (4K & 8K Ref.)	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	33		38		ns	7, 15
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	70		84		ns	7

4

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.2/0.7V$, $V_{oh}/V_{ol}=2.0/0.8V$, output loading $C_L=100pF$

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	45		53		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	47		58		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	17
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3
Hyper page mode cycle time	t_{HPC}	20		25		ns	10
Hyper page mode read-modify write cycle time	t_{HPRWC}	67		73		ns	10
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	7		10		ns	14
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{OE}$ access time	t_{OEA}		13		15	ns	
$\overline{OE}$ to data delay	t_{OED}	10		13		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	13	3	13	ns	6
$\overline{OE}$ command hold time	t_{OEH}	5		5		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	13	ns	6,12
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	13	ns	6
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC} (max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non-restrictive operating parameter. They are inclueded in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above contitions are satisfied, The condition of the data out is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. Operation within the t_{RAD} (max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.

10. $t_{ASC} \geq 6$ns, Assume t_T = 2.0ns.

11. For all of the refresh mode except distributed $\overline{CAS}$-before $\overline{RAS}$ refresh, 4096 cycle of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification.

12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condtion of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condtion of the output is achieved by $\overline{RAS}$ high going.

13. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.

14. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

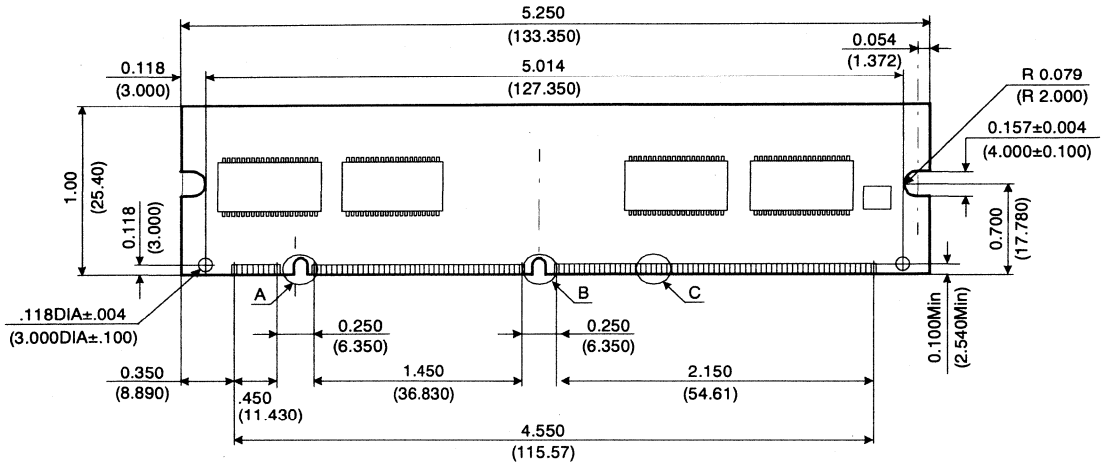
15. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

16. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

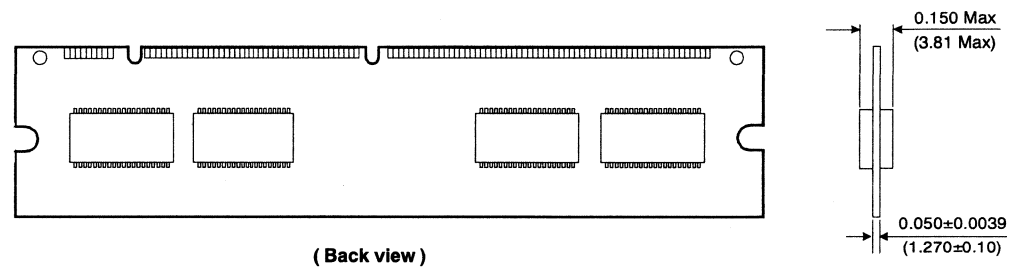
17. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.

PACKAGE DIMENSIONS

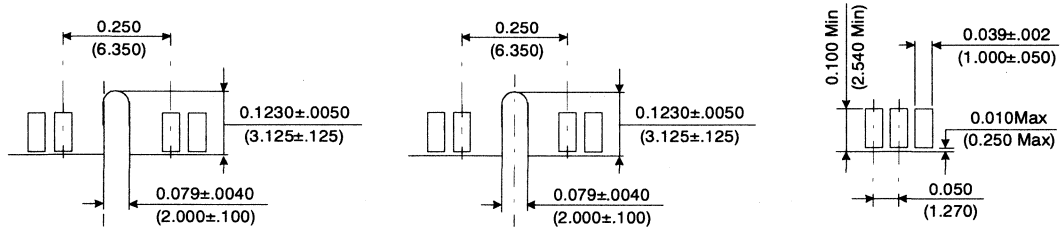
Units : Inches (millimeters)



(Front view)



(Back view)



Detail A **Detail B** **Detail C**

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 DRAM with EDO mode, TSOP II
DRAM Part No. : KMM366F884CS1 - KM416V4004CS
KMM366F804CS1 - KM416V4104CS

KMM374F80(8)3CK1 EDO Mode without buffer

8M x 72 DRAM DIMM with ECC Using 8Mx8, 8K & 4K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM374F80(8)3CK1 is a 8Mx72bits Dynamic RAM high density memory module. The Samsung KMM374F80(8)3CK1 consists of nine CMOS 8Mx8bits DRAMs in SOJ 400mil packages and one 2K EEPROM for SPD in 8-pin SOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM374F80(8)3CK1 is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

FEATURES

- Part Identification

Part number	PKG	Ref	CBR ref.	ROR ref.
KMM374F803CK1	SOJ	4K	4K/64ms	
KMM374F883CK1	SOJ	8K	4K/64ms	8K/64ms

- New JEDEC standard proposal without buffer
- Serial Presence Detect with EEPROM
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), single sided component

4

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS1}$	57	DQ18	85	Vss	113	$\overline{CAS5}$	141	DQ50
2	DQ0	30	$\overline{RAS0}$	58	DQ19	86	DQ32	114	*$\overline{RAS1}$	142	DQ51
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ33	115	DU	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	DU	90	Vcc	118	A3	146	DU
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	A11	150	DQ54
11	DQ8	39	A12	67	DQ23	95	DQ40	123	*A13	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	DU	153	DQ56
14	DQ10	42	DU	70	DQ25	98	DQ42	126	DU	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	$\overline{OE2}$	72	DQ27	100	DQ44	128	DU	156	DQ59
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ45	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS2}$	74	DQ28	102	Vcc	130	$\overline{CAS6}$	158	DQ60
19	DQ14	47	$\overline{CAS3}$	75	DQ29	103	DQ46	131	$\overline{CAS7}$	159	DQ61
20	DQ15	48	$\overline{W2}$	76	DQ30	104	DQ47	132	DU	160	DQ62
21	CB0	49	Vcc	77	DQ31	105	CB4	133	Vcc	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	NC	107	Vss	135	NC	163	NC
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{W0}$	55	DQ16	83	SCL	111	DU	139	DQ48	167	SA2
28	$\overline{CAS0}$	56	DQ17	84	Vcc	112	$\overline{CAS4}$	140	DQ49	168	Vcc

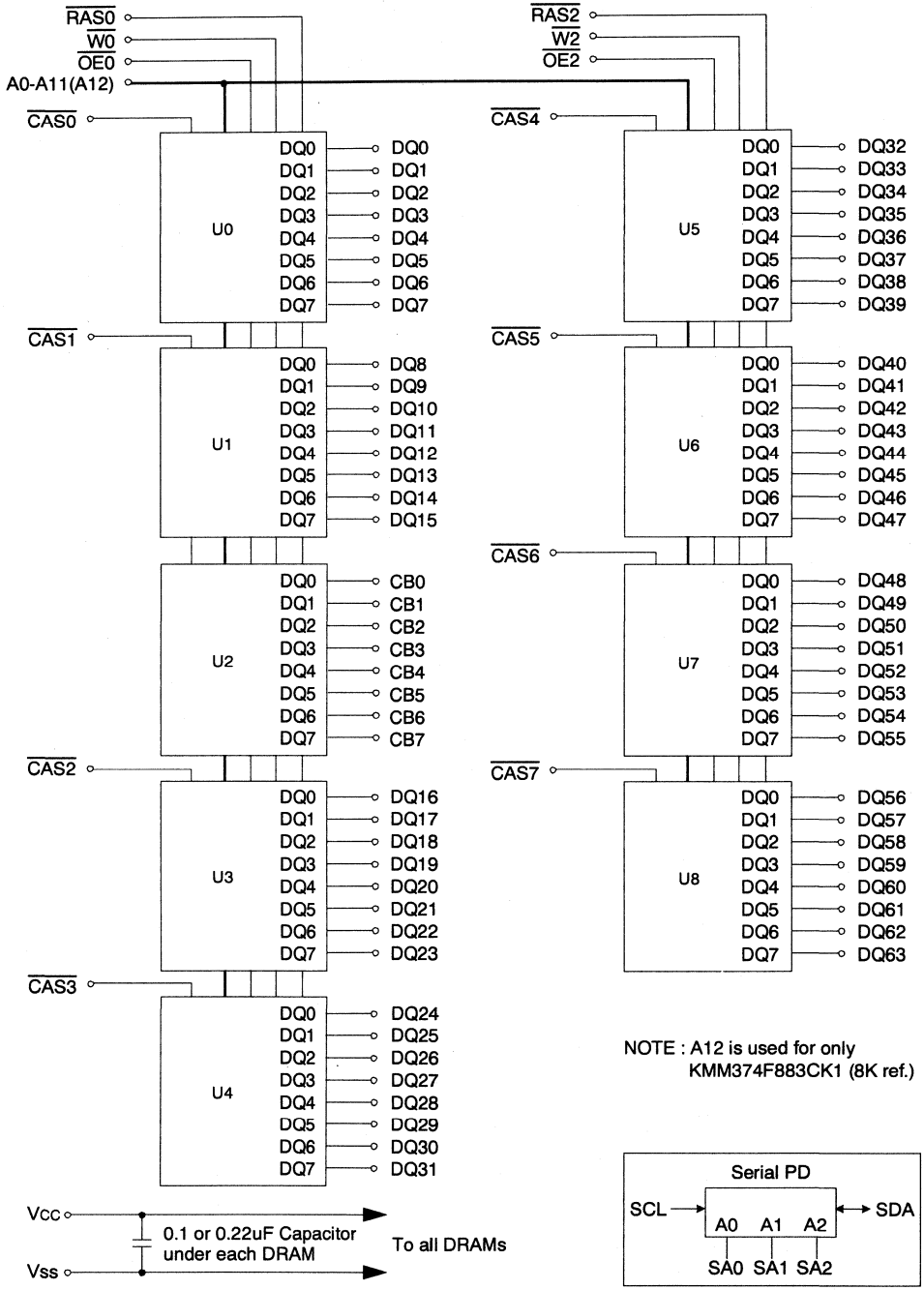
NOTE : A12 is used for only KMM374F883CK1 (8K ref.)

PIN NAMES

Pin Name	Function
A0 - A11	Address Input(4K ref.)
A0 - A12	Address Input(8K ref.)
DQ0 - DQ63	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
DU	Don't use
SDA	Serial Address /Data I/O
SCL	Serial Clock
SA0 -SA2	Address in EEPROM
CB0 - CB7	Check Bit

* These pins are not used in this module.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	9	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V at pulse width≤15ns which is measured at V_{CC}.

*2 : -1.3V at pulse width≤15ns which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM374F883CK1		KMM374F803CK1		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	720	-	990	mA
	-6	-	630	-	900	mA
I_{CC2}	Don't care	-	9	-	9	mA
I_{CC3}	-5	-	720	-	990	mA
	-6	-	630	-	900	mA
I_{CC4}	-5	-	810	-	810	mA
	-6	-	720	-	720	mA
I_{CC5}	Don't care	-	4.5	-	4.5	mA
I_{CC6}	-5	-	990	-	990	mA
	-6	-	900	-	900	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @ t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.3V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤ V_{OUT}≤V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC} .

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A12]	C_{IN1}	-	55	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	45	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	45	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	24	pF
Input/Output capacitance[DQ0-DQ63, CB0-CB7]	CDQ	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading C_L=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	128		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,9
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,9
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	6,10
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	8		10		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		40		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	17	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	12	25	15	30	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	7		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	7		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	7		10		ns	
Write command pulse width	t_{WP}	7		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	8		10		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	7		10		ns	
Data set-up time	t_{DS}	0		0		ns	
Data hold time	t_{DH}	7		10		ns	
Refresh period (4K & 8K Ref.)	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	33		38		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	70		84		ns	7

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.2/0.7V$, $V_{oh}/V_{ol}=2.0/0.8V$, output loading $C_L=100pF$

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	45		53		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	47		58		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3
Hyper page mode cycle time	t_{HPC}	20		25		ns	11
Hyper page mode read-modify write cycle time	t_{HPRWC}	67		73		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	7		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{OE}$ access time	t_{OEA}		13		15	ns	
$\overline{OE}$ to data delay	t_{OED}	10		13		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	13	3	13	ns	6
$\overline{OE}$ command hold time	t_{OEH}	5		5		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	13	ns	6,10
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	13	ns	6
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	

4

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non-restrictive operating parameter. They are inclueded in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above contitions are satisfied, The condition of the data out is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

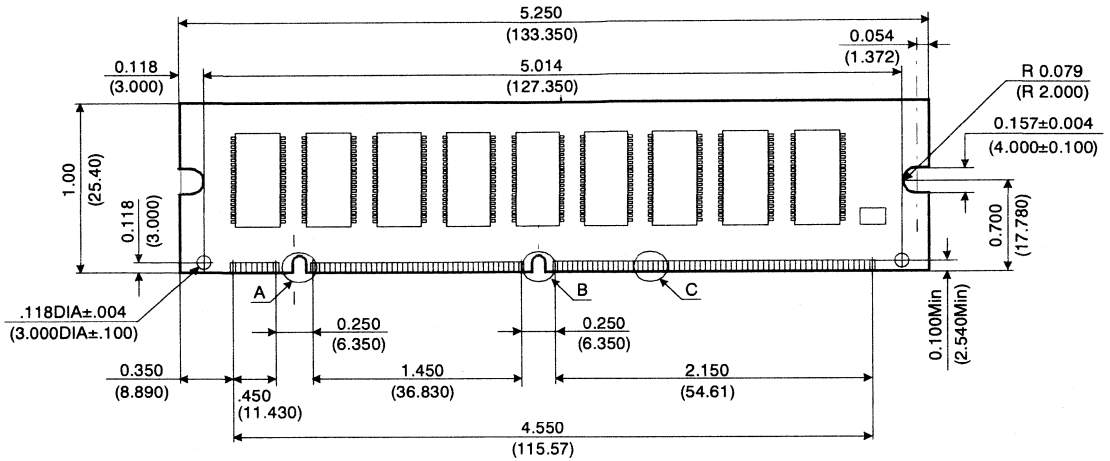
9. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.

10. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condtion of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condtion of the output is achieved by $\overline{RAS}$ high going.

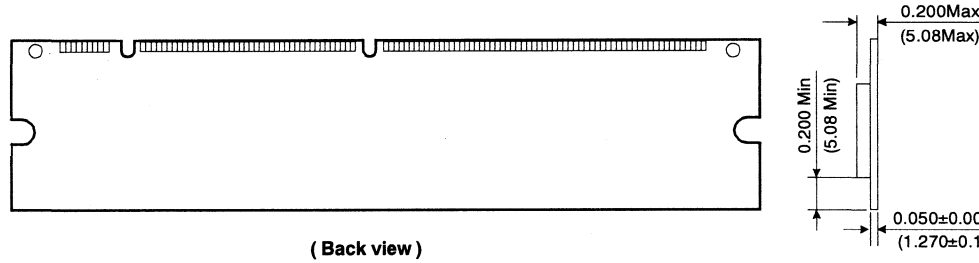
11. $t_{ASC} \geq 6ns$

PACKAGE DIMENSIONS

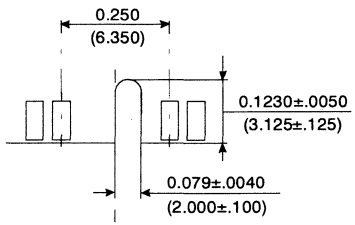
Units : Inches (millimeters)



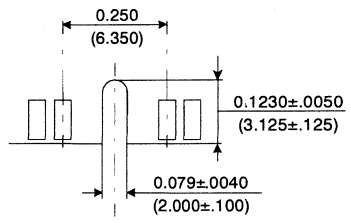
(Front view)



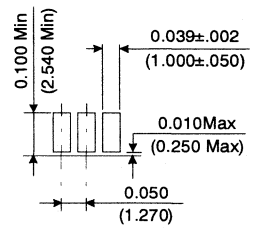
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 DRAM with EDO mode, SOJ
DRAM Part No. : KMM374F883CK1 - KM48V8004CK
KMM374F803CK1 - KM48V8104CK

KMM374F804CS1 Fast EDO Mode without buffer

8M x 72 DRAM DIMM with ECC Using 4Mx16 & 4Mx4, 4K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM374F804CS1 is a 8Mx72bits Dynamic RAM high density memory module. The Samsung KMM374F804CS1 consists of eight CMOS 4Mx16bits DRAMs in TSOP 400mil packages and four CMOS 4Mx4bits DRAMs in TSOP 300mil package and one 2K EEPROM for SPD in 8-pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM374F804CS1 is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

FEATURES

- Part Identification
  - KMM374F804CS1(4096 cycles/64ms, TSOP II)
- New JEDEC standard proposal without buffer
- Serial Presence Detect with EEPROM
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), double sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

PIN CONFIGURATIONS

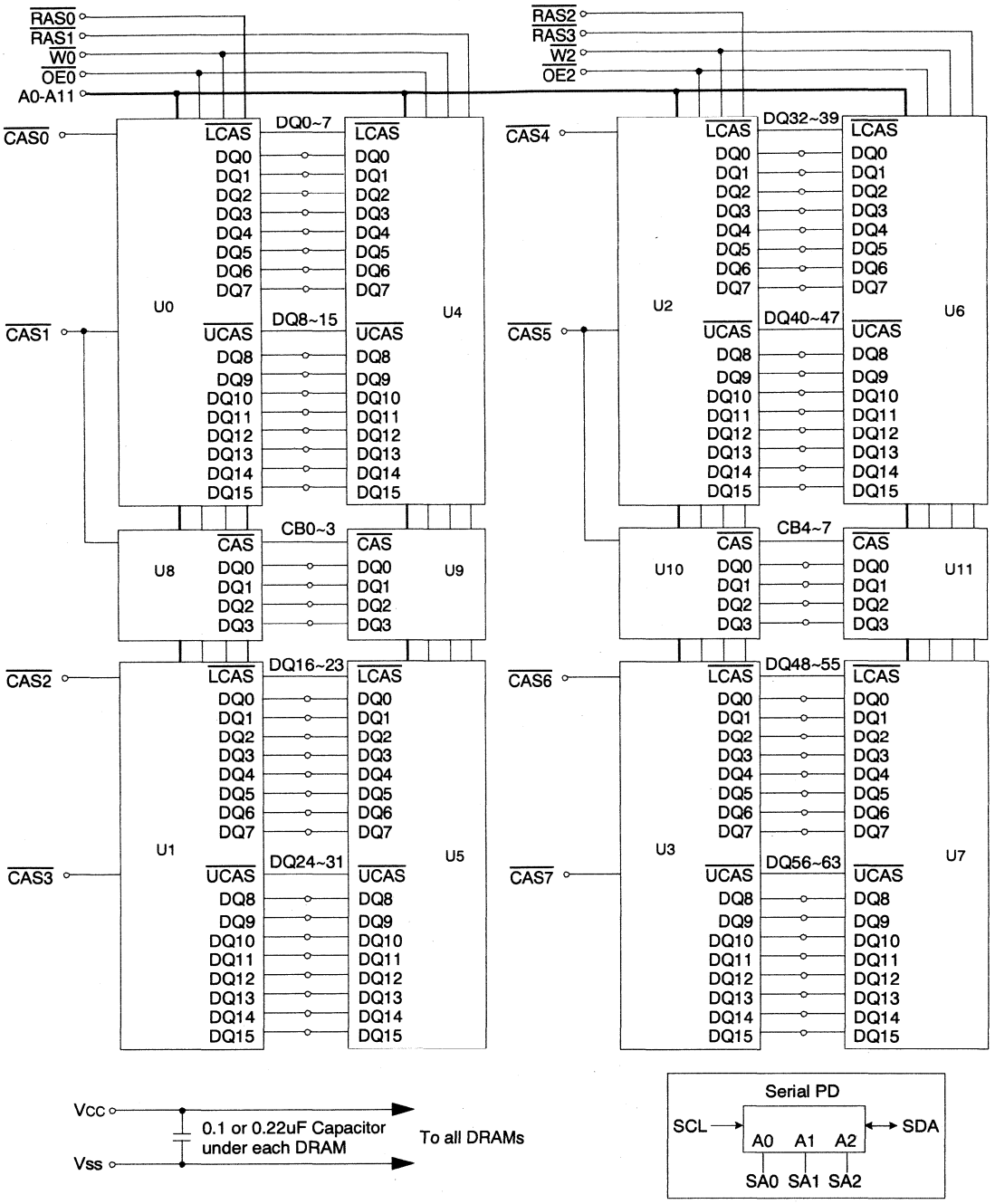
Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS1}$	57	DQ18	85	Vss	113	$\overline{CAS5}$	141	DQ50
2	DQ0	30	$\overline{RAS0}$	58	DQ19	86	DQ32	114	$\overline{RAS1}$	142	DQ51
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ33	115	DU	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	DU	90	Vcc	118	A3	146	DU
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	A11	150	DQ54
11	DQ8	39	*A12	67	DQ23	95	DQ40	123	*A13	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	DU	153	DQ56
14	DQ10	42	DU	70	DQ25	98	DQ42	126	DU	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	$\overline{OE2}$	72	DQ27	100	DQ44	128	DU	156	DQ59
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ45	129	$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS2}$	74	DQ28	102	Vcc	130	$\overline{CAS6}$	158	DQ60
19	DQ14	47	$\overline{CAS3}$	75	DQ29	103	DQ46	131	$\overline{CAS7}$	159	DQ61
20	DQ15	48	$\overline{W2}$	76	DQ30	104	DQ47	132	DU	160	DQ62
21	CB0	49	Vcc	77	DQ31	105	CB4	133	Vcc	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	NC	107	Vss	135	NC	163	NC
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{W0}$	55	DQ16	83	SCL	111	DU	139	DQ48	167	SA2
28	$\overline{CAS0}$	56	DQ17	84	Vcc	112	$\overline{CAS4}$	140	DQ49	168	Vcc

PIN NAMES

Pin Name	Function
A0 - A11	Address Input
DQ0 - DQ63	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
DU	Don't use
SDA	Serial Address /Data I/O
SCL	Serial Clock
SA0 -SA2	Address in EEPROM
CB0 - CB7	Check Bit

* These pins are not used in this module.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_d	12	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V at pulse width≤15ns which is measured at V_{CC}.

*2 : -1.3V at pulse width≤15ns which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM374F804CS1		Unit
		Min	Max	
I_{CC1}	-5	-	666	mA
	-6	-	606	mA
I_{CC2}	Don't care	-	12	mA
I_{CC3}	-5	-	666	mA
	-6	-	606	mA
I_{CC4}	-5	-	526	mA
	-6	-	466	mA
I_{CC5}	Don't care	-	6	mA
I_{CC6}	-5	-	666	mA
	-6	-	606	mA
$I_{I(L)}$	Don't care	-10	10	uA
$I_{O(L)}$		-10	10	uA
V_{OH}	Don't care	2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @ t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.3V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V ≤V_{OUT}≤V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	70	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	52	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	31	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	38	pF
Input/Output capacitance[DQ0-DQ63, CB0-CB7]	C_{DQ}	-	24	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading C_L=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	128		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,9
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,9
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	6,12
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	8		10		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		40		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	17	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	12	25	15	30	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	7		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	13
Column address hold time	t_{CAH}	7		10		ns	13
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	7		10		ns	
Write command pulse width	t_{WP}	7		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	8		10		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	7		10		ns	16
Data set-up time	t_{DS}	0		0		ns	
Data hold time	t_{DH}	7		10		ns	
Refresh period (4K Ref.)	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	33		38		ns	7, 15
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	70		84		ns	7

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.2/0.7V$, $V_{oh}/V_{ol}=2.0/0.8V$, output loading $C_L=100pF$

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	45		53		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	47		58		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	17
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3
Hyper page mode cycle time	t_{HPC}	20		25		ns	10
Hyper page mode read-modify write cycle time	t_{HPRWC}	67		73		ns	10
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	7		10		ns	14
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{OE}$ access time	t_{OEA}		13		15	ns	
$\overline{OE}$ to data delay	t_{OED}	10		13		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	13	3	13	ns	6
$\overline{OE}$ command hold time	t_{OEH}	5		5		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	13	ns	6,12
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	13	ns	6
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non-restrictive operating parameter. They are inclueded in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above contitions are satisfied, The condition of the data out is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.

10. $t_{ASC} \geq 6$ns, Assume t_T = 2.0ns

11. For all of the refresh mode except distributed $\overline{CAS}$-before $\overline{RAS}$ refresh, 4096 cycle of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification.

12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condtion of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condtion of the output is achieved by $\overline{RAS}$ high going.

13. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.

14. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

15. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

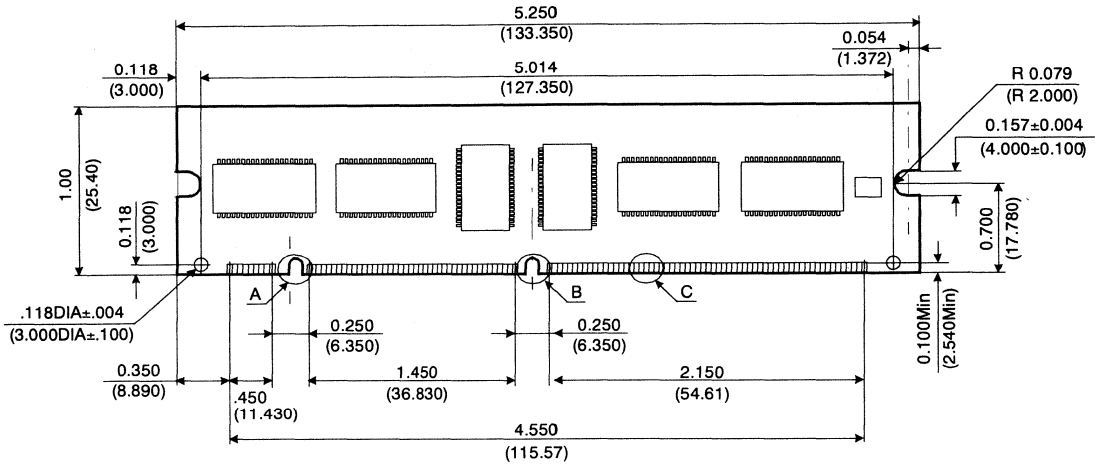
16. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

17. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.

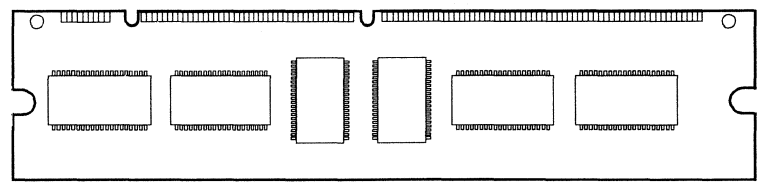
4

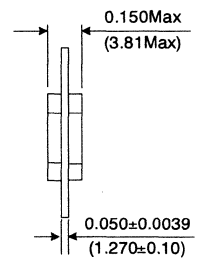
PACKAGE DIMENSIONS

Units : Inches (millimeters)

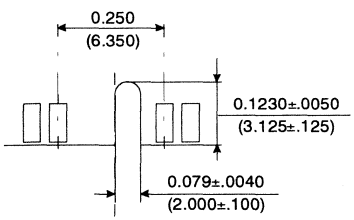


(Front view)

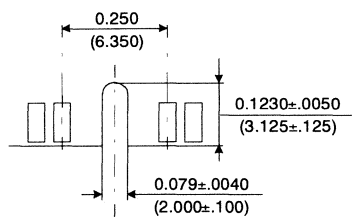




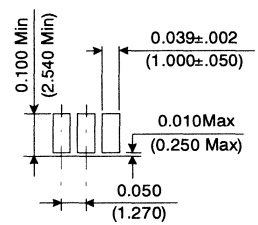
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 and 4Mx4 DRAM with EDO mode, TSOP II
DRAM Part No. : KMM374F804CS1 - KM416V4104CS
- KM44V4004CS

KMM366F160(8)0CK2 EDO Mode without buffer

16M x 64 DRAM DIMM Using 16Mx4, 4K & 8K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM366F160(8)0CK2 is a 16Mx64bits Dynamic RAM high density memory module. The Samsung KMM366F160(8)0CK2 consists of sixteen CMOS 16Mx4bits DRAMs in SOJ 400mil packages and one 2K EEPROM for SPD in 8-pin SOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM366F160(8)0CK2 is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	tRAC	tCAC	tRC	tHPC
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM366F1600CK2	SOJ	4K	4K/64ms	
KMM366F1680CK2	SOJ	8K	4K/64ms	8K/64ms

- New JEDEC standard proposal without buffer
- Serial Presence Detect with EEPROM
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), double sided component

4

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS1}$	57	DQ18	85	Vss	113	$\overline{CAS5}$	141	DQ50
2	DQ0	30	$\overline{RAS0}$	58	DQ19	86	DQ32	114	*$\overline{RAS1}$	142	DQ51
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ33	115	DU	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	DU	90	Vcc	118	A3	146	DU
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	A11	150	DQ54
11	DQ8	39	A12	67	DQ23	95	DQ40	123	*A13	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	DU	153	DQ56
14	DQ10	42	DU	70	DQ25	98	DQ42	126	DU	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	$\overline{OE2}$	72	DQ27	100	DQ44	128	DU	156	DQ59
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ45	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS2}$	74	DQ28	102	Vcc	130	$\overline{CAS6}$	158	DQ60
19	DQ14	47	$\overline{CAS3}$	75	DQ29	103	DQ46	131	$\overline{CAS7}$	159	DQ61
20	DQ15	48	$\overline{W2}$	76	DQ30	104	DQ47	132	DU	160	DQ62
21	*CB0	49	Vcc	77	DQ31	105	*CB4	133	Vcc	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	NC	107	Vss	135	NC	163	NC
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{W0}$	55	DQ16	83	SCL	111	DU	139	DQ48	167	SA2
28	$\overline{CAS0}$	56	DQ17	84	Vcc	112	$\overline{CAS4}$	140	DQ49	168	Vcc

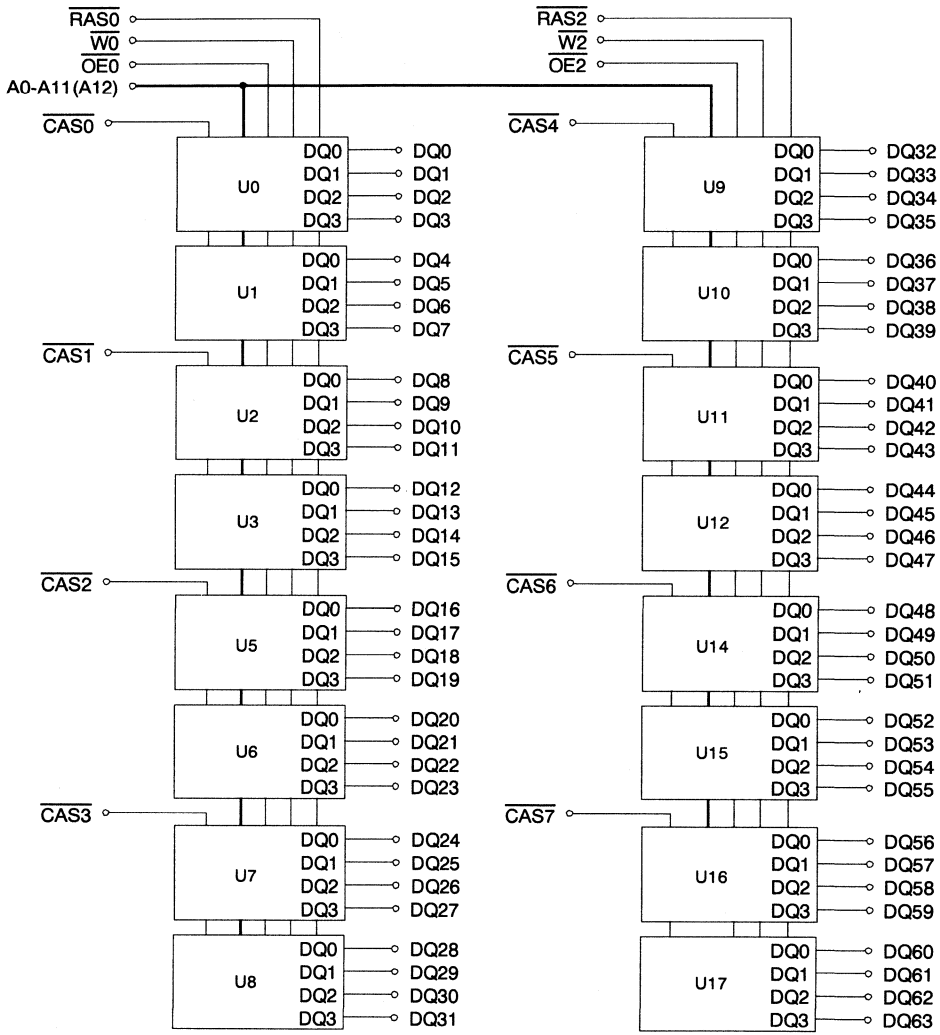
NOTE : A12 is used for only KMM366F1680CK2 (8K ref.)

PIN NAMES

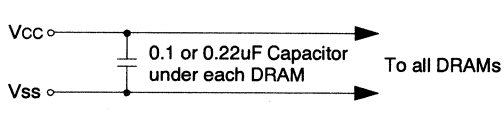
Pin Name	Function
A0 - A11	Address Input(4K ref.)
A0 - A12	Address Input(8K ref.)
DQ0 - DQ63	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
DU	Don't use
SDA	Serial Address /Data I/O
SCL	Serial Clock
SA0 -SA2	Address in EEPROM
*CB0 - CB7	Check Bit

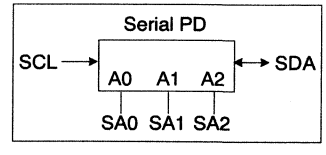
* These pins are not used in this module.

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM366F1680CK2 (8K ref.)





ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	16	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V at pulse width≤15ns which is measured at V_{CC}.

*2 : -1.3V at pulse width≤15ns which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM366F1680CK2		KMM366F1600CK2		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	1280	-	1760	mA
	-6	-	1120	-	1600	mA
I_{CC2}	Don't care	-	16	-	16	mA
I_{CC3}	-5	-	1280	-	1760	mA
	-6	-	1120	-	1600	mA
I_{CC4}	-5	-	1440	-	1440	mA
	-6	-	1280	-	1280	mA
I_{CC5}	Don't care	-	8	-	8	mA
I_{CC6}	-5	-	1760	-	1760	mA
	-6	-	1600	-	1600	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤ V_{OUT}≤V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A12]	C_{IN1}	-	90	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	66	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	66	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	24	pF
Input/Output capacitance[DQ0-DQ63]	CDQ	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading C_L=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	128		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,9
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,9
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	6,10
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	8		10		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		40		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	17	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	12	25	15	30	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	7		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	7		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	7		10		ns	
Write command pulse width	t_{WP}	7		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	8		10		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	7		10		ns	
Data set-up time	t_{DS}	0		0		ns	
Data hold time	t_{DH}	7		10		ns	
Refresh period (4K & 8K Ref.)	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	33		38		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	70		84		ns	7

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.2/0.7V$, $V_{oh}/V_{ol}=2.0/0.8V$, output loading $C_L=100pF$

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	45		53		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	47		58		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3
Hyper page mode cycle time	t_{HPC}	20		25		ns	11
Hyper page mode read-modify write cycle time	t_{HPRWC}	67		73		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	7		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{OE}$ access time	t_{OEA}		13		15	ns	
$\overline{OE}$ to data delay	t_{OED}	10		13		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	13	3	13	ns	6
$\overline{OE}$ command hold time	t_{OEH}	5		5		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	13	ns	6,10
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	13	ns	6
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC} (max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non-restrictive operating parameter. They are inclueded in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above contitions are satisfied, The condition of the data out is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

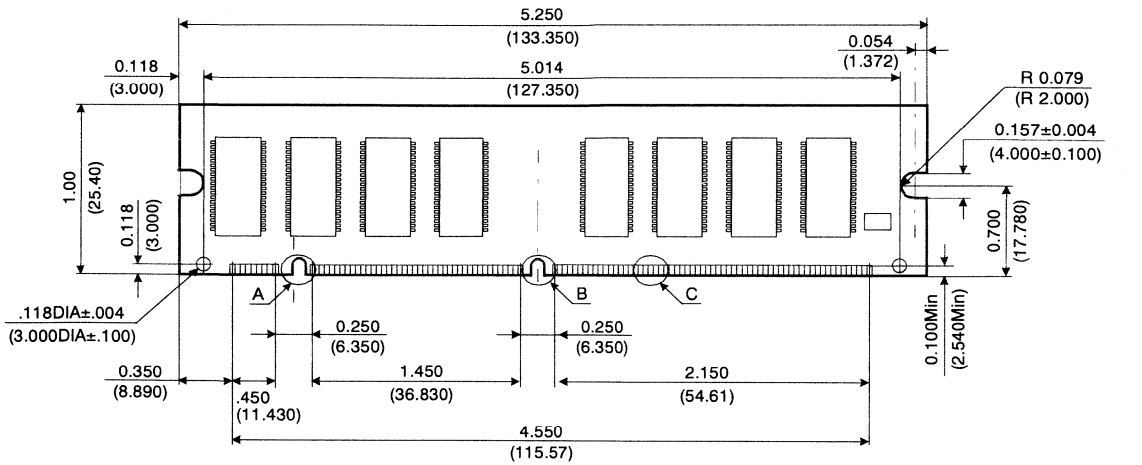
9. Operation within the t_{RAD} (max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.

10. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condtion of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condtion of the output is achieved by $\overline{RAS}$ high going.

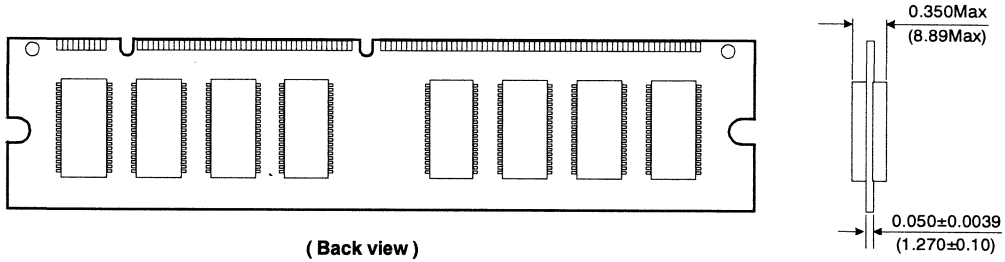
11. $t_{ASC} \geq 6$ns

PACKAGE DIMENSIONS

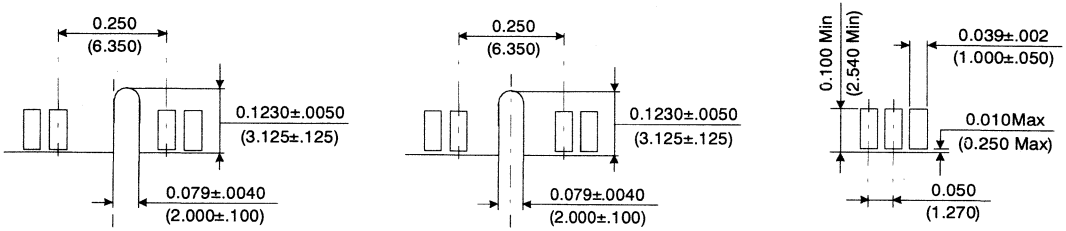
Units : Inches (millimeters)



(Front view)



(Back view)



Detail A **Detail B** **Detail C**

Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx4 DRAM with EDO mode, SOJ
DRAM Part No. : KMM366F1600CK2 - KM44V16104CK
KMM366F1680CK2 - KM44V16004CK

KMM374F160(8)0CK1 EDO Mode without buffer

16M x 72 DRAM DIMM with ECC Using 16Mx4, 4K & 8K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM374F160(8)0CK1 is a 16Mx72bits Dynamic RAM high density memory module. The Samsung KMM374F160(8)0CK1 consists of eighteen CMOS 16Mx4bits DRAMs in SOJ 400mil packages and one 1K/2K EEPROM for SPD in 8-pin SOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM374F160(8)0CK1 is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

FEATURES

- Part Identification

Part number	PK	Ref.	CBR	ROR
KMM374F1600CK1	SOJ	4K	4K/64ms	
KMM374F1680CK1	SOJ	8K	4K/64ms	8K/64ms

- New JEDEC standard proposal without buffer
- Serial Presence Detect with EEPROM
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS1}$	57	DQ18	85	Vss	113	$\overline{CAS5}$	141	DQ50
2	DQ0	30	$\overline{RAS0}$	58	DQ19	86	DQ32	114	*$\overline{RAS1}$	142	DQ51
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ33	115	DU	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	DU	90	Vcc	118	A3	146	DU
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	A11	150	DQ54
11	DQ8	39	A12	67	DQ23	95	DQ40	123	*A13	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	DU	153	DQ56
14	DQ10	42	DU	70	DQ25	98	DQ42	126	DU	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	$\overline{OE2}$	72	DQ27	100	DQ44	128	DU	156	DQ59
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ45	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS2}$	74	DQ28	102	Vcc	130	$\overline{CAS6}$	158	DQ60
19	DQ14	47	$\overline{CAS3}$	75	DQ29	103	DQ46	131	$\overline{CAS7}$	159	DQ61
20	DQ15	48	$\overline{W2}$	76	DQ30	104	DQ47	132	DU	160	DQ62
21	CB0	49	Vcc	77	DQ31	105	CB4	133	Vcc	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	NC	107	Vss	135	NC	163	NC
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{W0}$	55	DQ16	83	SCL	111	DU	139	DQ48	167	SA2
28	$\overline{CAS0}$	56	DQ17	84	Vcc	112	$\overline{CAS4}$	140	DQ49	168	Vcc

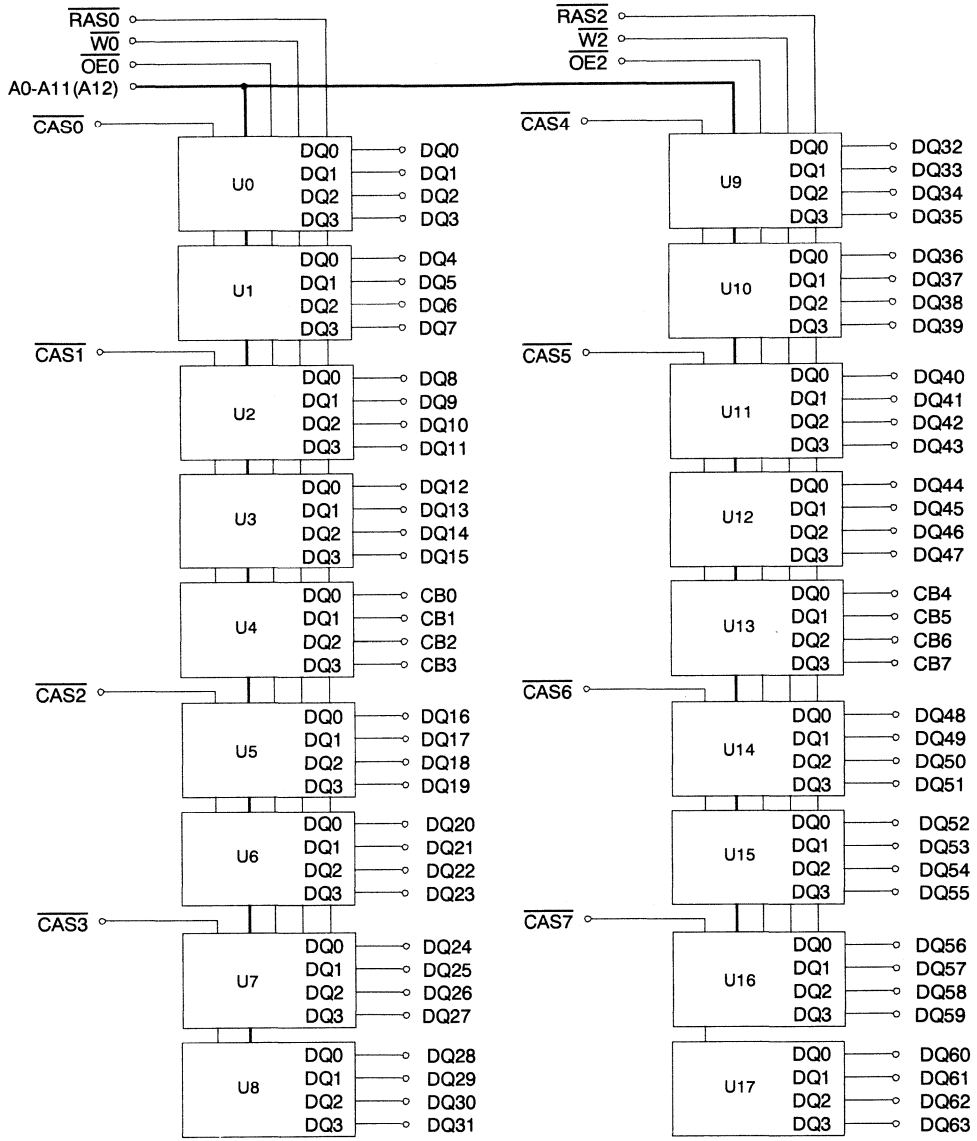
NOTE : A12 is used for only KMM374F1680CK1 (8K ref.)

PIN NAMES

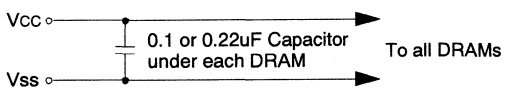
Pin Name	Function
A0 - A11	Address Input(4K ref.)
A0 - A12	Address Input(8K ref.)
DQ0 - DQ63	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
DU	Don't use
SDA	Serial Address/Data I/O
SCL	Serial Clock
SA0 - SA2	Address in EEPROM
CB0 - CB7	Check Bit

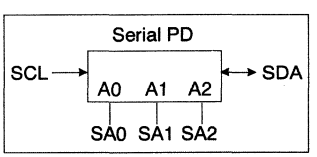
* These pins are not used in this module.

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM374F1680CK1 (8K ref.)





ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	18	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for in tended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V at pulse width≤15ns which is measured at V_{CC}.

*2 : -1.3V at pulse width≤15ns which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM374F1680CK1		KMM374F1600CK1		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	1440	-	1980	mA
	-6	-	1260	-	1800	mA
I_{CC2}	Don't care	-	18	-	18	mA
I_{CC3}	-5	-	1440	-	1980	mA
	-6	-	1260	-	1800	mA
I_{CC4}	-5	-	1620	-	1620	mA
	-6	-	1440	-	1440	mA
I_{CC5}	Don't care	-	9	-	9	mA
I_{CC6}	-5	-	1980	-	1980	mA
	-6	-	1800	-	1800	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @ t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL} , $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤ V_{IN}≤V_{CC}+0.3V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC} .

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A12]	C_{IN1}	-	100	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	73	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	73	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	31	pF
Input/Output capacitance[DQ0-DQ63, CB0-CB7]	CDQ	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading C_L=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	128		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,9
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,9
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	6,10
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	8		10		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		40		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	17	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	12	25	15	30	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	7		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	7		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	7		10		ns	
Write command pulse width	t_{WP}	7		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	8		10		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	7		10		ns	
Data set-up time	t_{DS}	0		0		ns	
Data hold time	t_{DH}	7		10		ns	
Refresh period (4K & 8K Ref.)	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	33		38		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	70		84		ns	7

4

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.2/0.7V$, $V_{oh}/V_{ol}=2.0/0.8V$, output loading $C_L=100pF$

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	45		53		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	47		58		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3
Hyper page mode cycle time	t_{HPC}	20		25		ns	11
Hyper page mode read-modify write cycle time	t_{HPRWC}	67		73		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	7		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{OE}$ access time	t_{OEA}		13		15	ns	
$\overline{OE}$ to data delay	t_{OED}	10		13		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	13	3	13	ns	6
$\overline{OE}$ command hold time	t_{OEH}	5		5		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	13	ns	6,10
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	13	ns	6
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non-restrictive operating parameter. They are inclueded in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above contitions are satisfied, The condition of the data out is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.

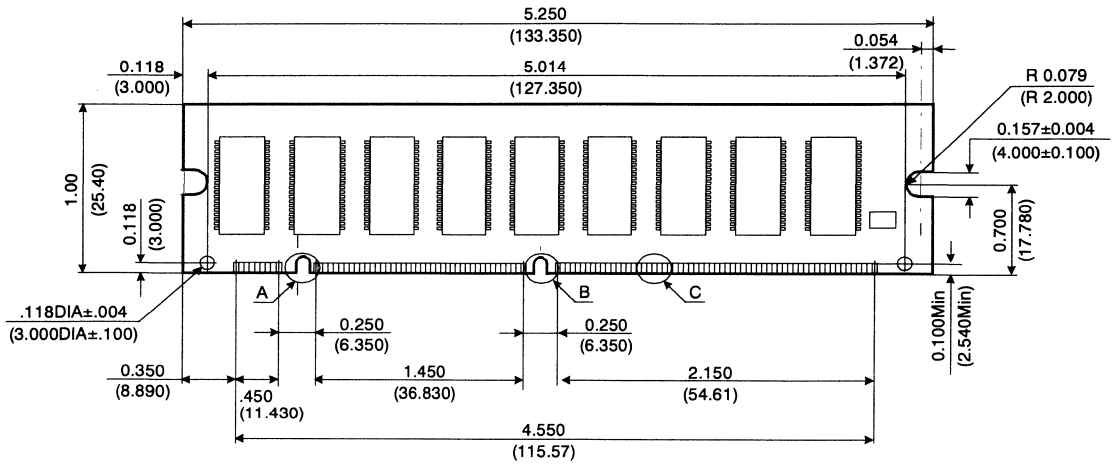
10. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condtion of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condtion of the output is achieved by $\overline{RAS}$ high going.

11. $t_{ASC} \geq 6$ns.

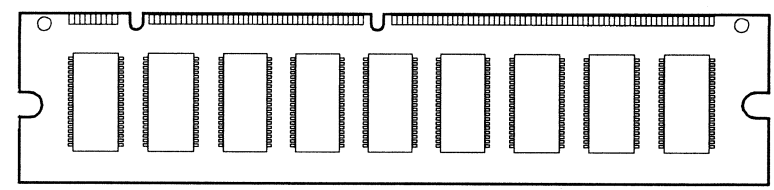
4

PACKAGE DIMENSIONS

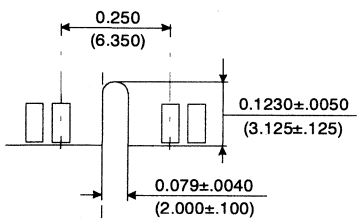
Units : Inches (millimeters)



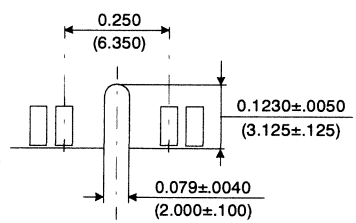
(Front view)



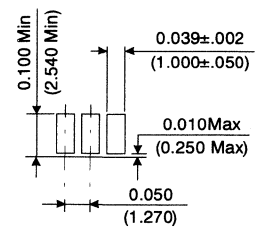
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx4 DRAM with EDO mode, SOJ
DRAM Part No. : KMM374F1680CK1 - KM44V16004CK
KMM374F1600CK1 - KM44V16104CK

KMM374F320(8)0CK1 EDO Mode without buffer

32M x 72 DRAM DIMM with ECC Using 16Mx4, 4K & 8K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM374F320(8)0CK1 is a 32Mx72bits Dynamic RAM high density memory module. The Samsung KMM374F320(8)0CK1 consists of thirty-six CMOS 16Mx4bits DRAMs in SOJ 400mil packages and one 1K/2K EEPROM for SPD in 8-pin SOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM374F320(8)0CK1 is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-5	50ns	13ns	84ns	20ns
-6	60ns	15ns	104ns	25ns

FEATURES

- Part Identification

Part number	PK	Ref	CBR ref.	ROR ref.
KMM374F3200CK1	SOJ	4K	4K/64ms	
KMM374F3280CK1	SOJ	8K	4K/64ms	8K/64ms

- New JEDEC standard proposal without buffer
- Serial Presence Detect with EEPROM
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1625mil), double sided component

4

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS1}$	57	DQ18	85	Vss	113	$\overline{CAS5}$	141	DQ50
2	DQ0	30	$\overline{RAS0}$	58	DQ19	86	DQ32	114	$\overline{RAS1}$	142	DQ51
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ33	115	DU	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	DU	90	Vcc	118	A3	146	DU
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	A11	150	DQ54
11	DQ8	39	A12	67	DQ23	95	DQ40	123	*A13	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	DU	153	DQ56
14	DQ10	42	DU	70	DQ25	98	DQ42	126	DU	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	$\overline{OE2}$	72	DQ27	100	DQ44	128	DU	156	DQ59
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ45	129	$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS2}$	74	DQ28	102	Vcc	130	$\overline{CAS6}$	158	DQ60
19	DQ14	47	$\overline{CAS3}$	75	DQ29	103	DQ46	131	$\overline{CAS7}$	159	DQ61
20	DQ15	48	$\overline{W2}$	76	DQ30	104	DQ47	132	DU	160	DQ62
21	CB0	49	Vcc	77	DQ31	105	CB4	133	Vcc	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	NC	107	Vss	135	NC	163	NC
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{W0}$	55	DQ16	83	SCL	111	DU	139	DQ48	167	SA2
28	$\overline{CAS0}$	56	DQ17	84	Vcc	112	$\overline{CAS4}$	140	DQ49	168	Vcc

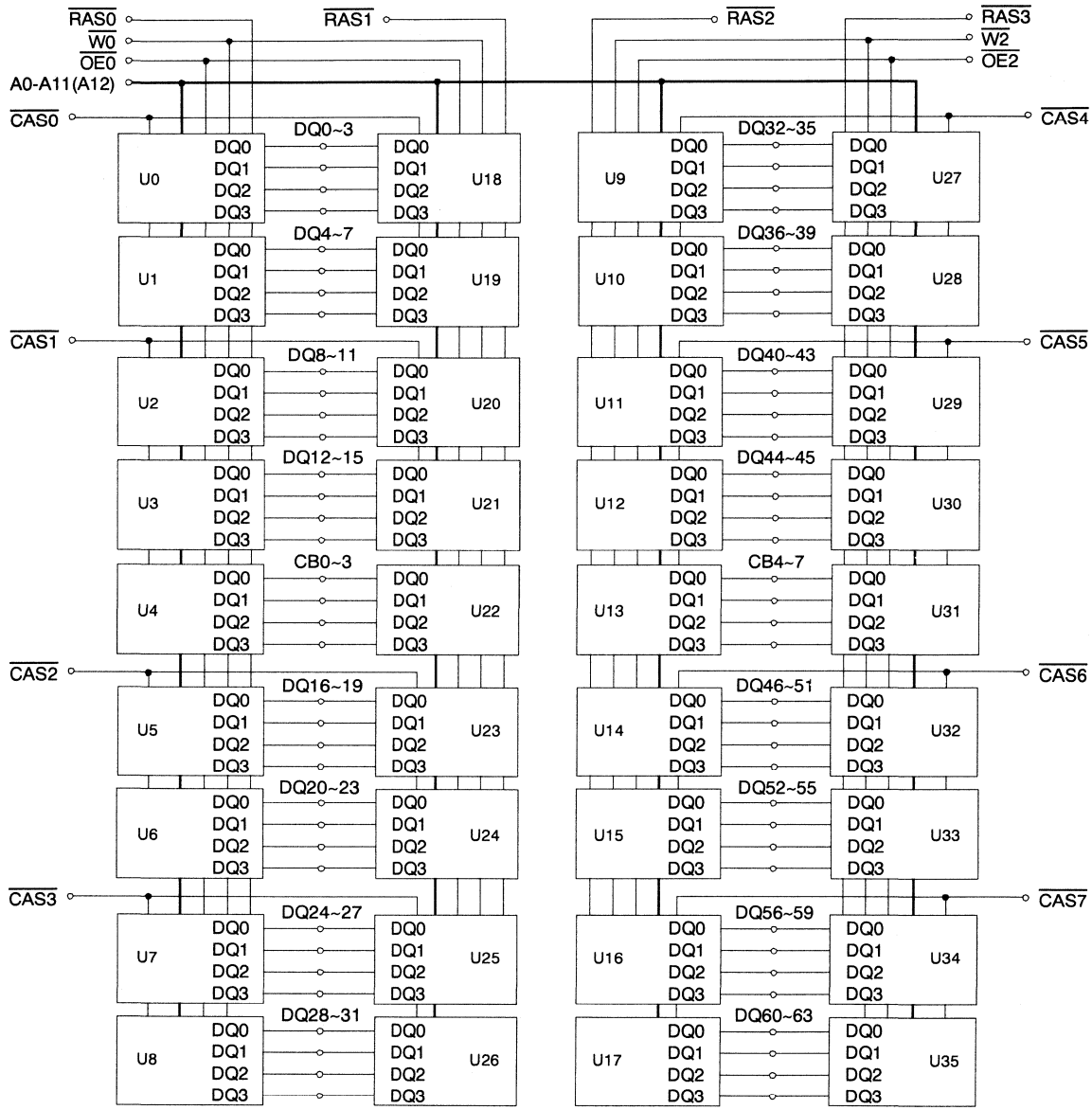
NOTE : A12 is used for only KMM374F3280CK1 (8K ref.)

PIN NAMES

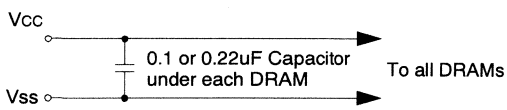
Pin Name	Function
A0 - A11	Address Input(4K ref.)
A0 - A12	Address Input(8K ref.)
DQ0 - DQ63	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
DU	Don't use
SDA	Serial Address /Data I/O
SCL	Serial Clock
SA0 -SA2	Address in EEPROM
CB0 - CB7	Check Bit

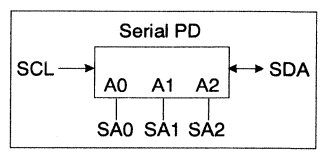
* These pins are not used in this module.

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM374F3280CK1 (8K ref.)





ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	Pd	36	W
Short Circuit Output Current	Ios	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for in tended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V at pulse width≤15ns which is measured at V_{CC}.

*2 : -1.3V at pulse width≤15ns which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM374F3280CK1		KMM374F3200CK1		Unit
		Min	Max	Min	Max	
I_{CC1}	-5	-	1458	-	1998	mA
	-6	-	1278	-	1818	mA
I_{CC2}	Don't care	-	36	-	36	mA
I_{CC3}	-5	-	1458	-	1998	mA
	-6	-	1278	-	1818	mA
I_{CC4}	-5	-	1638	-	1638	mA
	-6	-	1458	-	1458	mA
I_{CC5}	Don't care	-	18	-	18	mA
I_{CC6}	-5	-	1998	-	1998	mA
	-6	-	1818	-	1818	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-10	10	-10	10	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC} =min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤ V_{IN}≤V_{CC}+0.3V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤ V_{OUT}≤V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC} .

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A12]	C_{IN1}	-	190	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	136	pF
Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$]	C_{IN3}	-	73	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	52	pF
Input/Output capacitance[DQ0-DQ63, CB0-CB7]	C_{DQ}	-	27	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading C_L=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	128		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,9
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,9
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	6,10
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	8		10		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		40		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	17	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	12	25	15	30	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	7		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	7		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	7		10		ns	
Write command pulse width	t_{WP}	7		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	8		10		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	7		10		ns	
Data set-up time	t_{DS}	0		0		ns	
Data hold time	t_{DH}	7		10		ns	
Refresh period (4K & 8K Ref.)	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	33		38		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	70		84		ns	7

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=3.3V \pm 0.3V$. See notes 1,2.)

Test condition : $V_{ih}/V_{il}=2.2/0.7V$, $V_{oh}/V_{ol}=2.0/0.8V$, output loading $C_L=100pF$

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	45		53		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	47		58		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3
Hyper page mode cycle time	t_{HPC}	20		25		ns	11
Hyper page mode read-modify write cycle time	t_{HPRWC}	67		73		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	7		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{OE}$ access time	t_{OEA}		13		15	ns	
$\overline{OE}$ to data delay	t_{OED}	10		13		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	13	3	13	ns	6
$\overline{OE}$ command hold time	t_{OEH}	5		5		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	13	ns	6,10
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	13	ns	6
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non-restrictive operating parameter. They are inclueded in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above contitions are satisfied, The condition of the data out is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

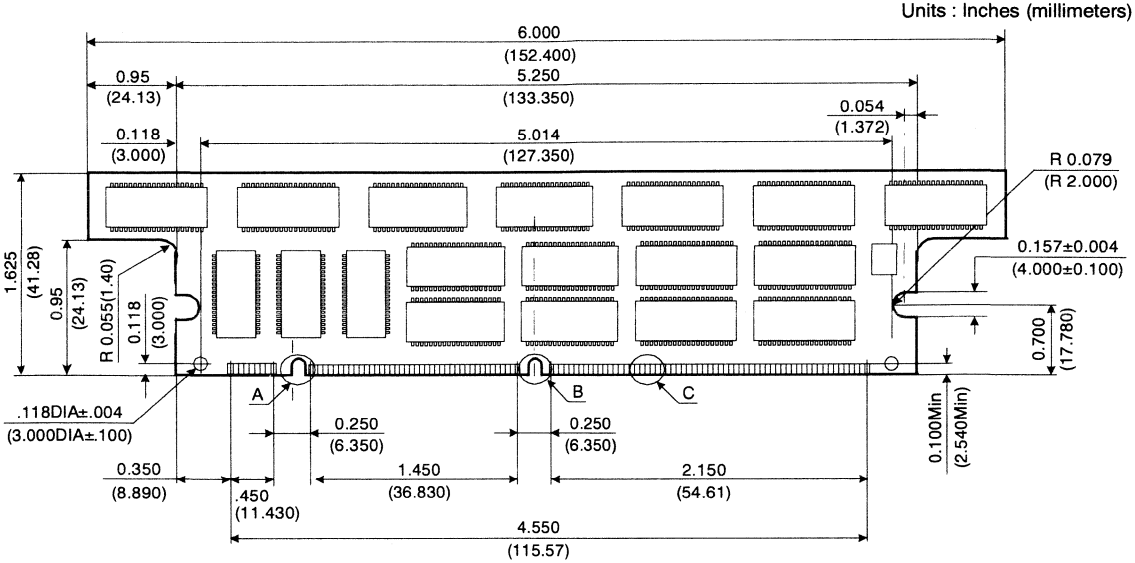
9. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.

10. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condtion of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condtion of the output is achieved by $\overline{RAS}$ high going.

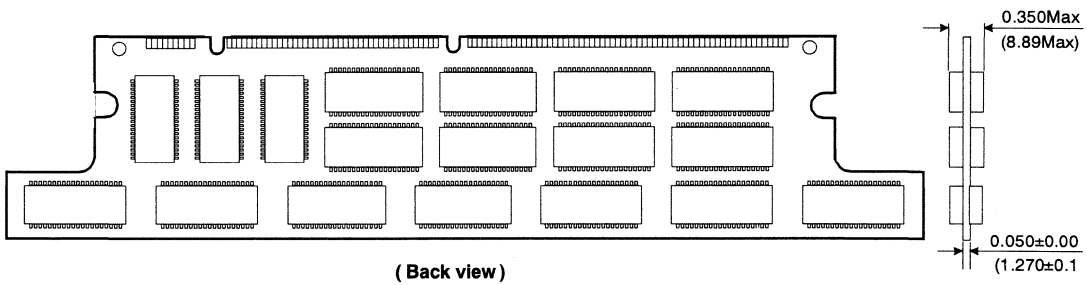
11. $t_{ASC} \geq 6$ns.

PACKAGE DIMENSIONS

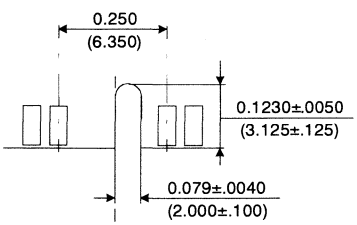
Units : Inches (millimeters)



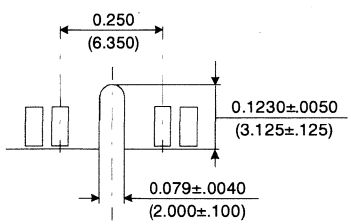
(Front view)



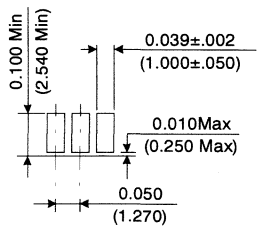
(Back view)



Detail A



Detail B

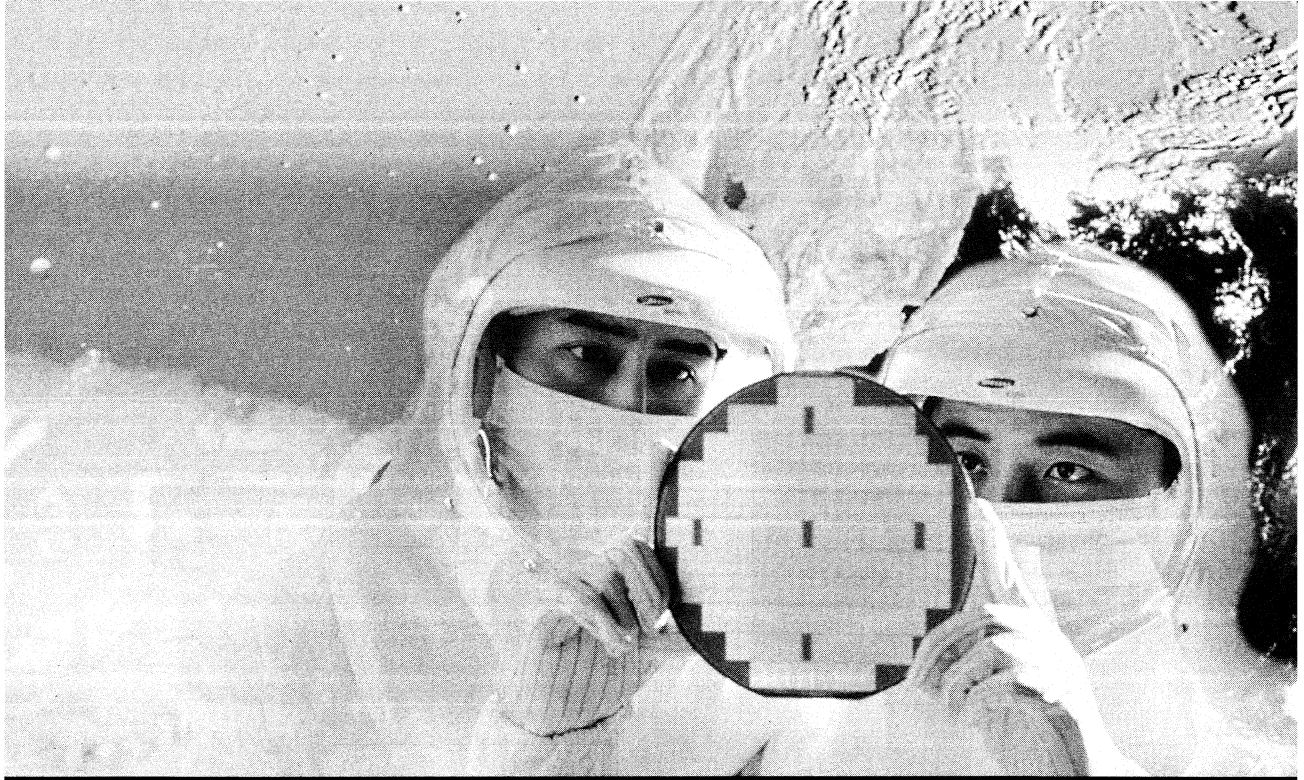


Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx4 DRAM with EDO mode, SOJ
DRAM Part No. : KMM374F3280CK1-KM44V16004CK
KMM374F3200CK1-KM44V16104CK

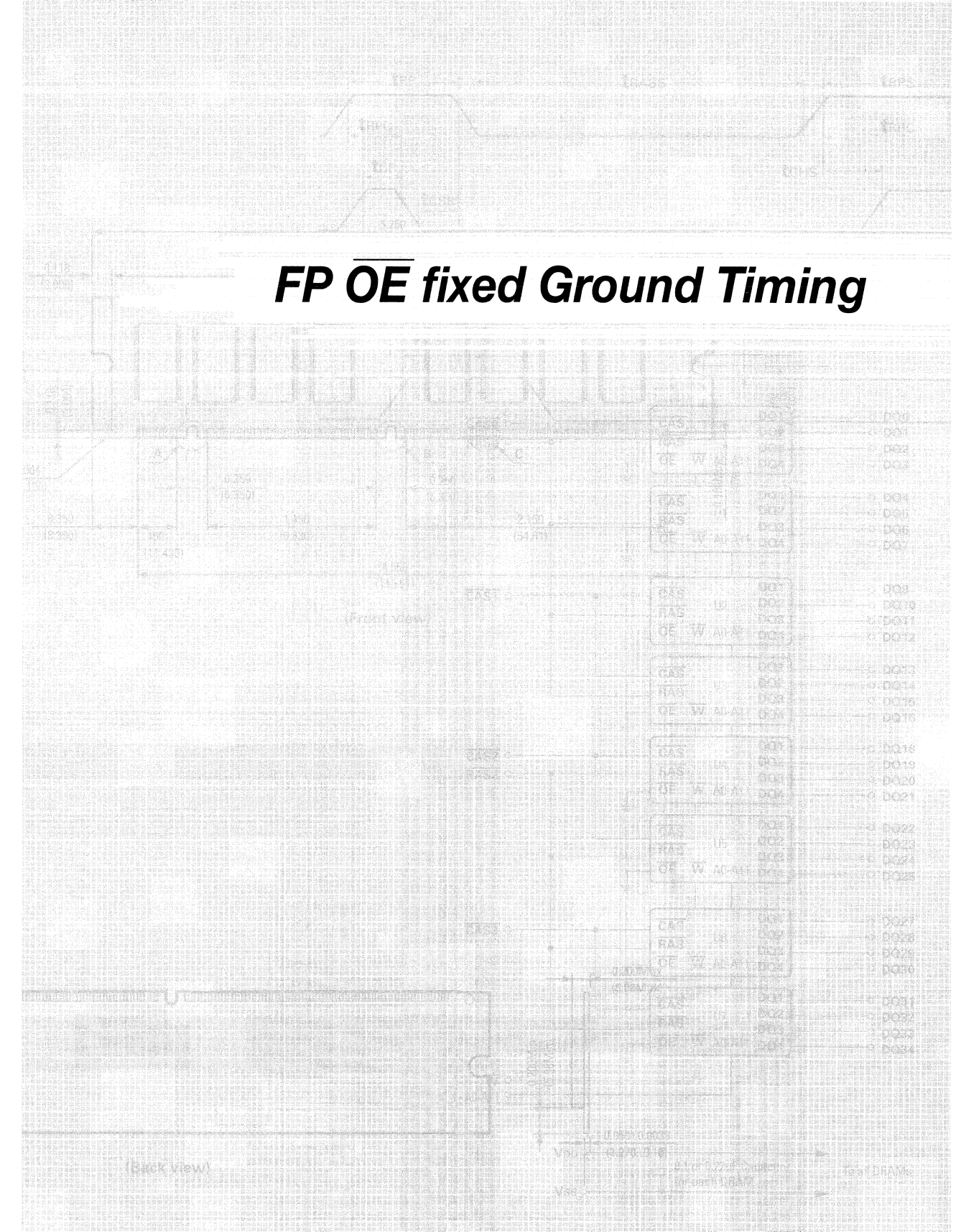
NOTES



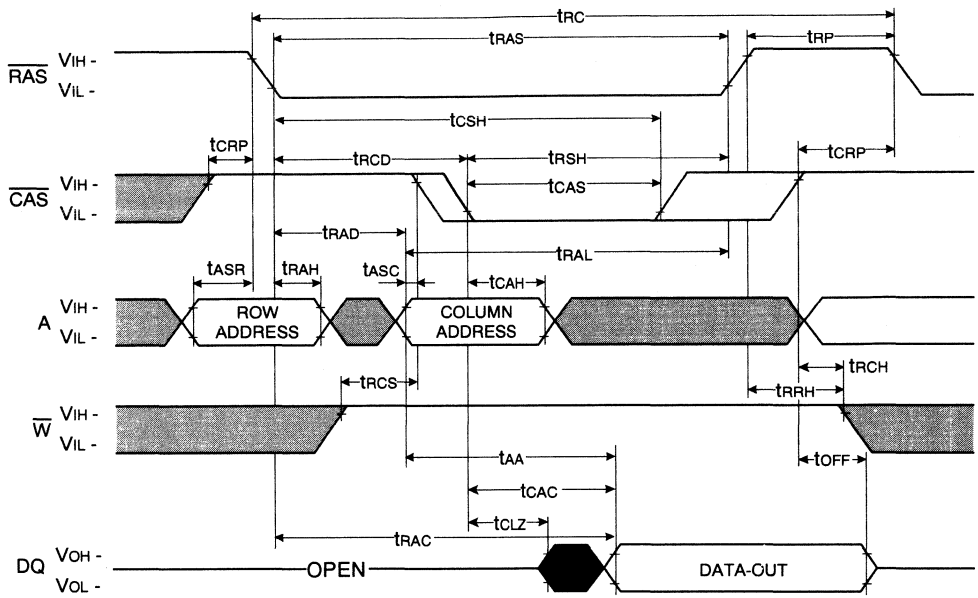
Timing Diagram 5

1. FP, $\overline{OE}$ fixed ground Timing
2. FP, $\overline{OE}$ controlled Timing
3. EDO, $\overline{OE}$ fixed ground Timing
4. EDO, $\overline{OE}$ controlled Timing

FP $\overline{OE}$ fixed Ground Timing



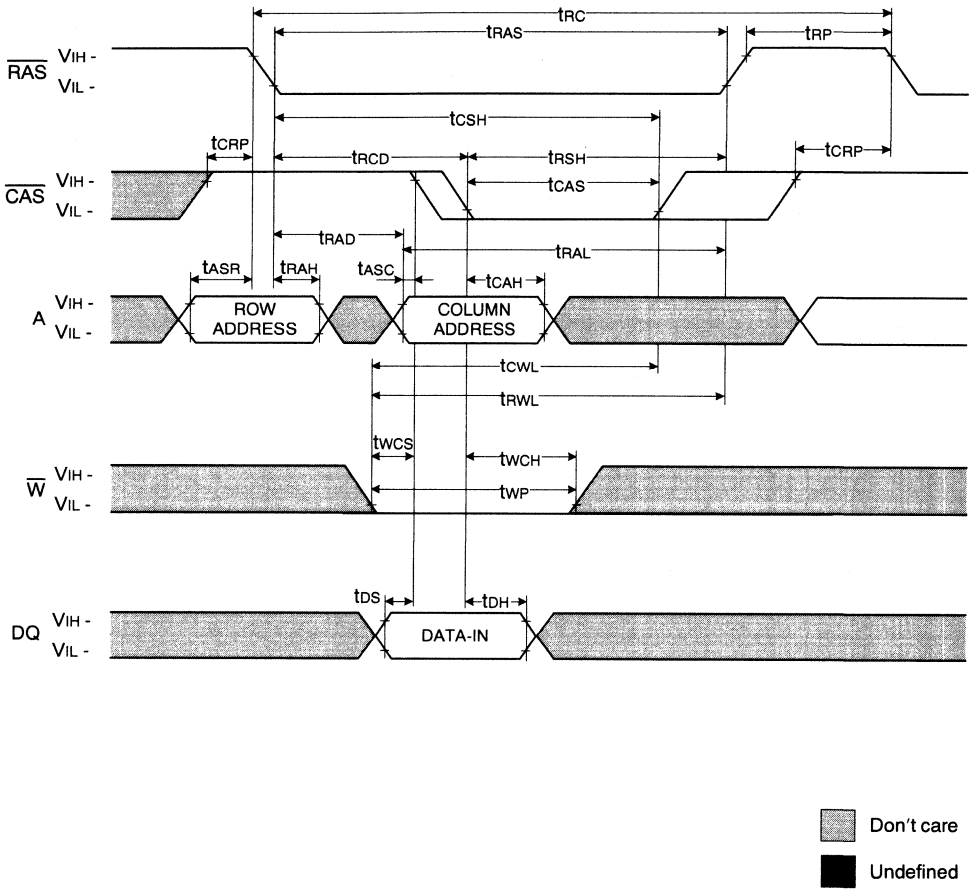
READ CYCLE


tRC
tRAS
tRP
RAS VIH - VIL -
tCSH
tCRP
tRCD
tRSH
tCRP
CAS VIH - VIL -
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A VIH - VIL -
ROW ADDRESS
COLUMN ADDRESS
tRCH
tRCS
tRRH
W VIH - VIL -
tAA
tOFF
tCAC
tCLZ
tRAC
DQ VOH - VOL -
OPEN
DATA-OUT
Don't care
Undefined

5

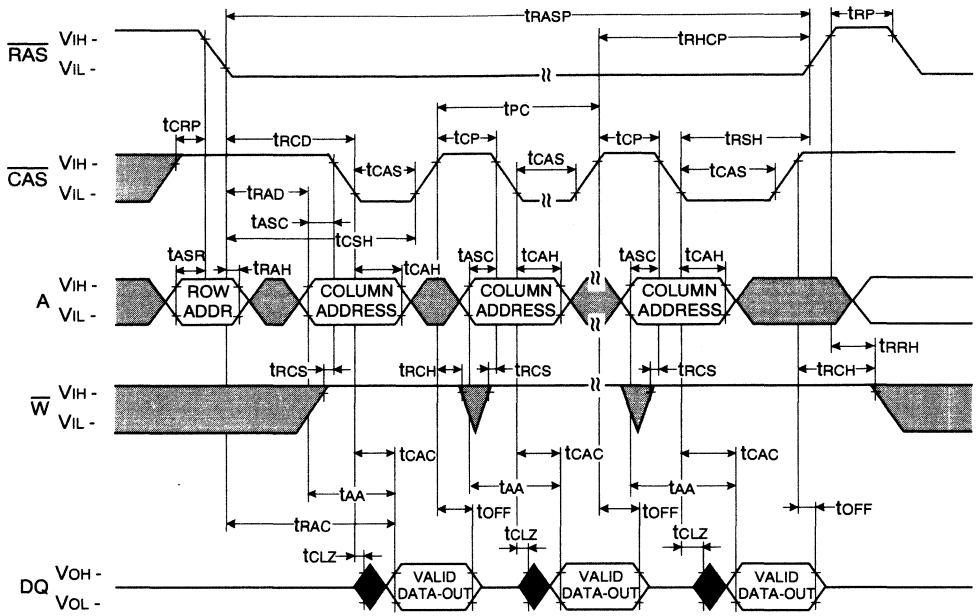
WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



FAST PAGE READ CYCLE

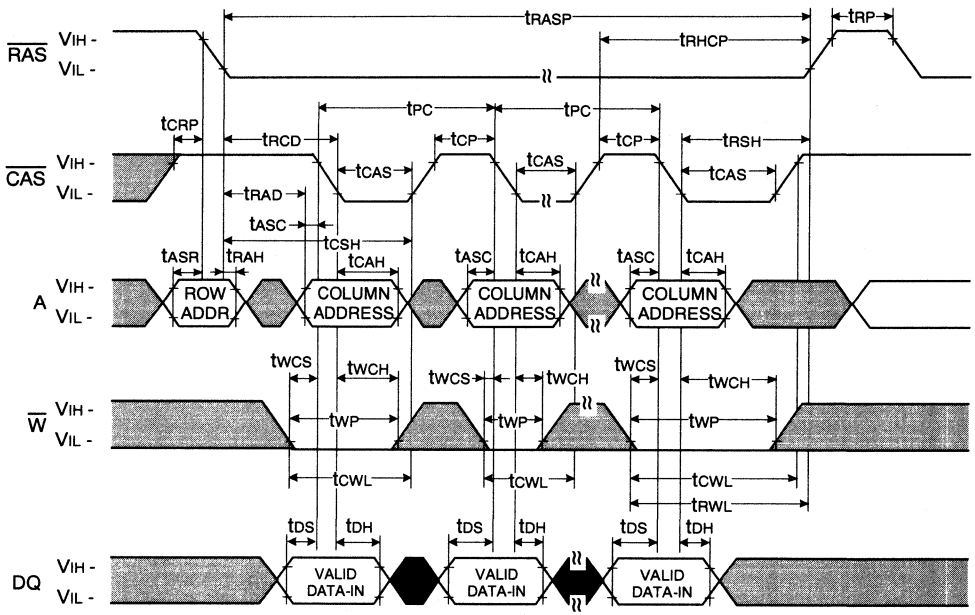
NOTE : DOUT = OPEN



5

FAST PAGE WRITE CYCLE (EARLY WRITE)

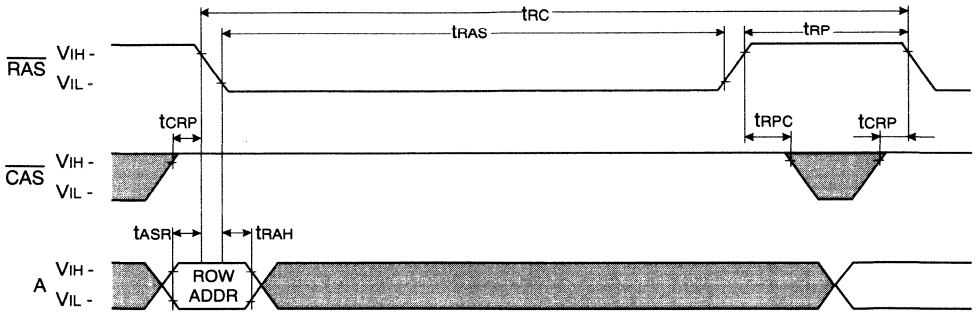
NOTE : DOUT = OPEN



$\overline{RAS}$ - ONLY REFRESH CYCLE

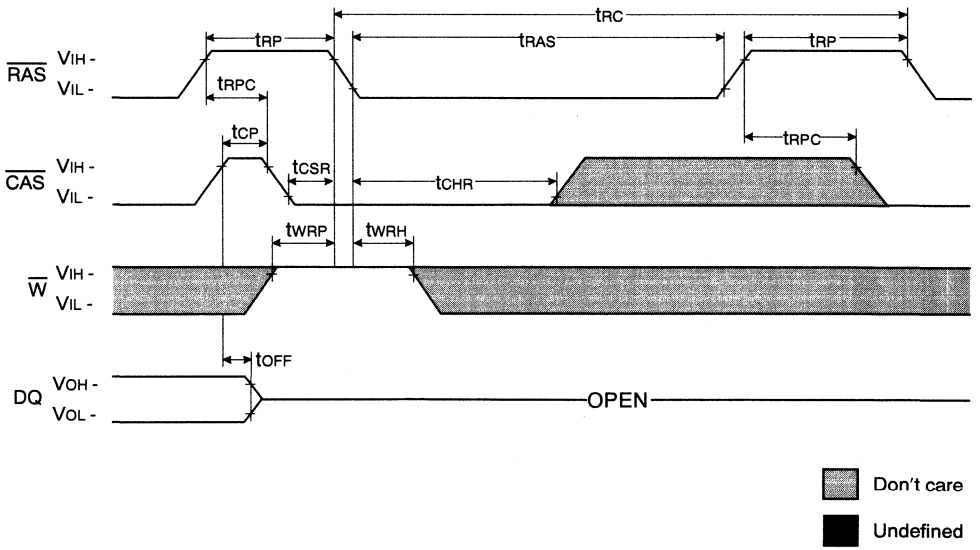
NOTE : $\overline{W}$, $\overline{OE}$, DIN = Don't care

DOUT = OPEN



$\overline{CAS}$ - BEFORE - $\overline{RAS}$ REFRESH CYCLE

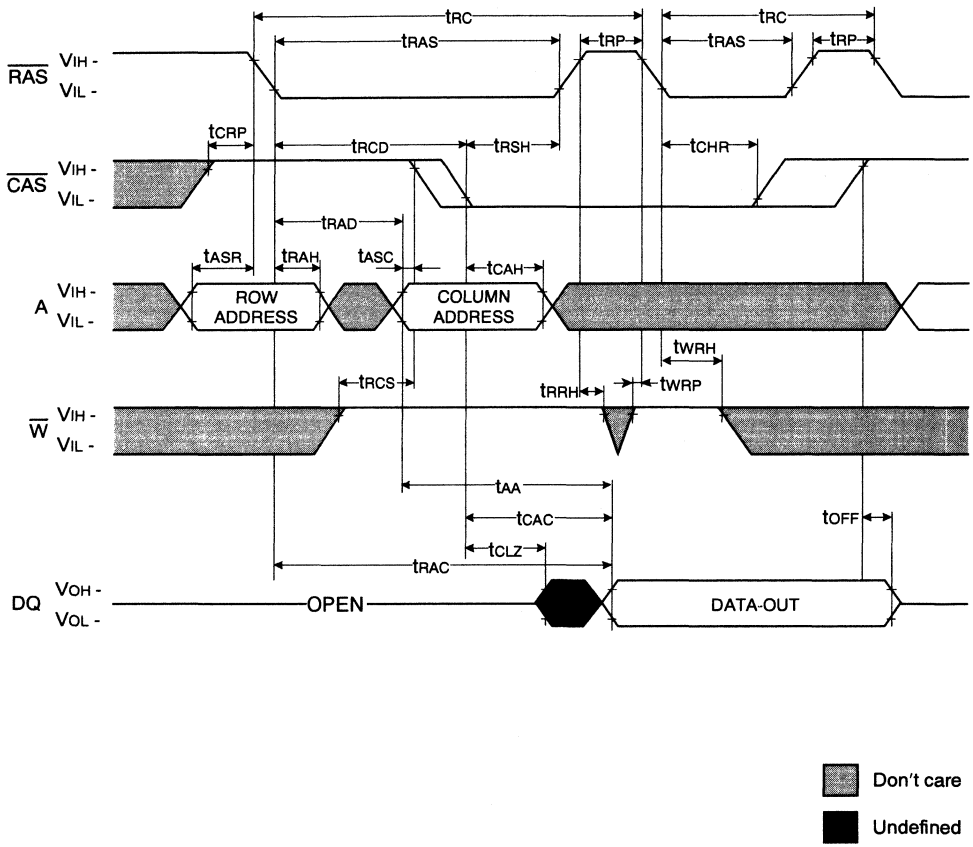
NOTE : $\overline{OE}$, A = Don't care



5

SAMSUNG ELECTRONICS

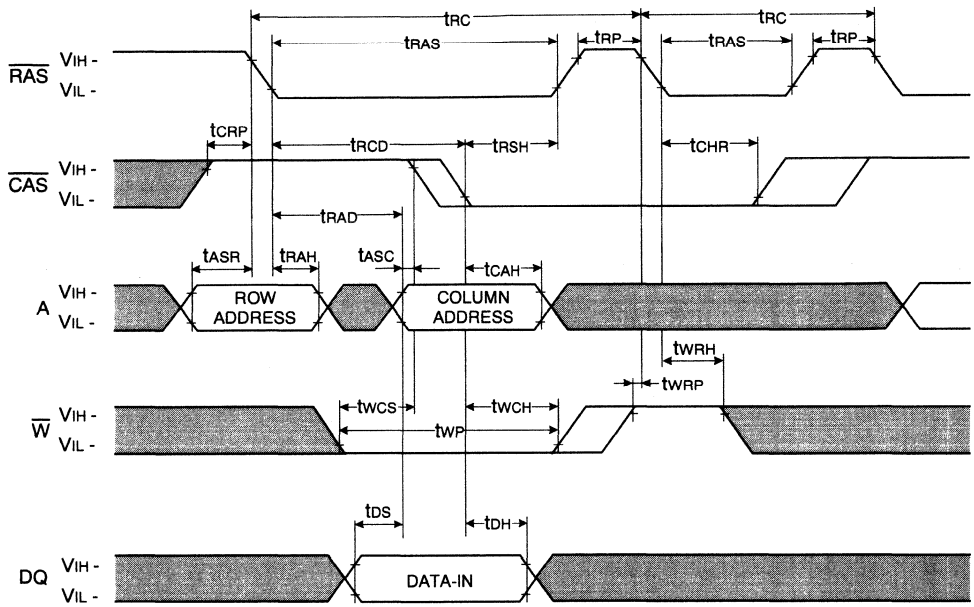
HIDDEN REFRESH CYCLE (READ)



SAMSUNG ELECTRONICS

HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN

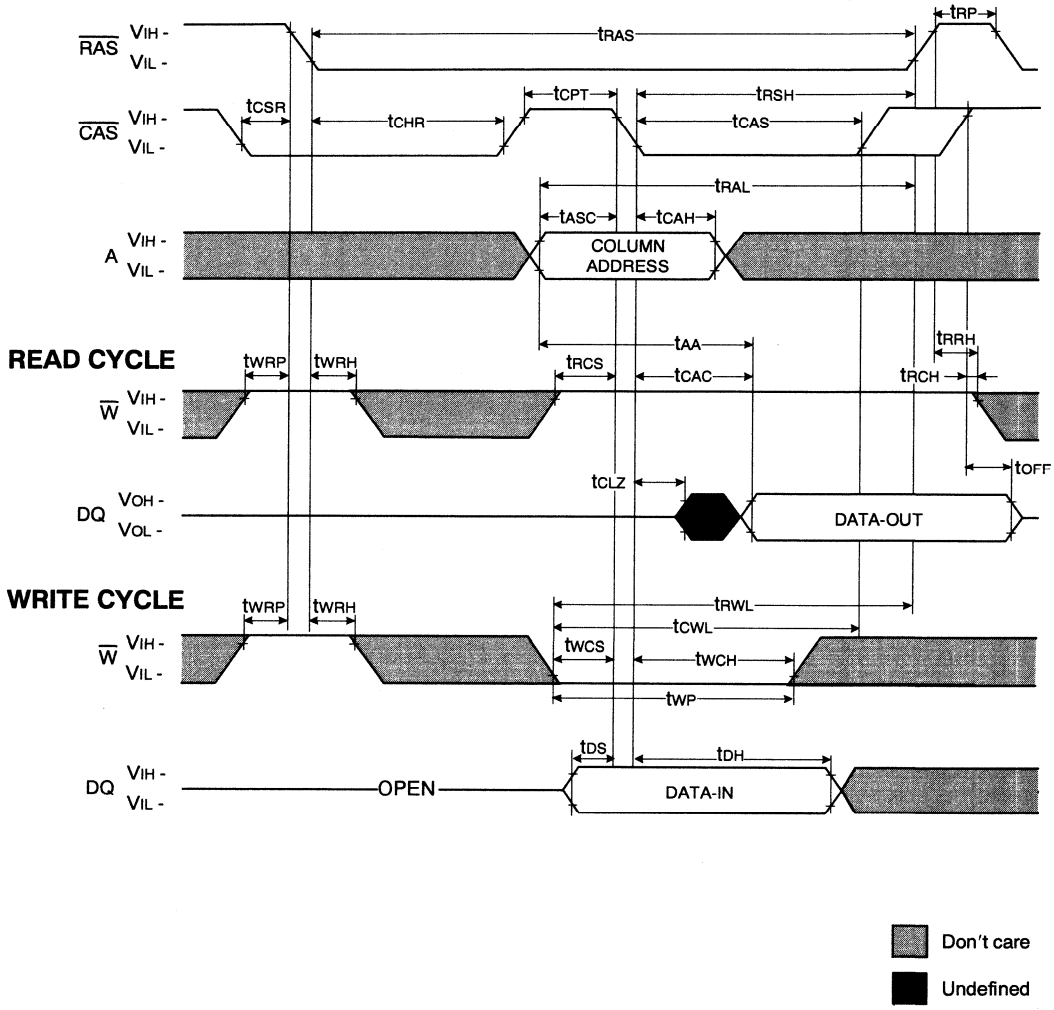


Don't care

Undefined

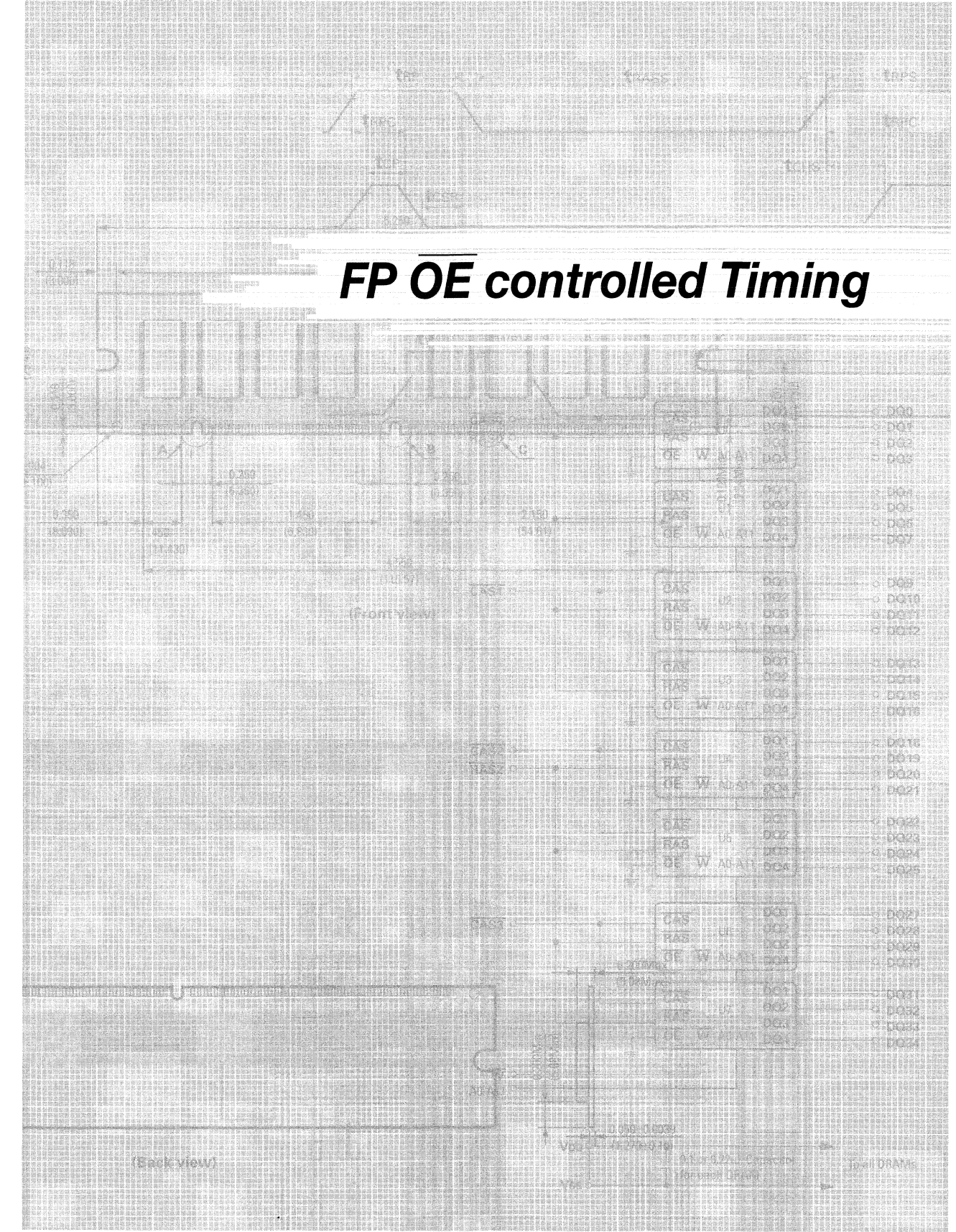
5

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

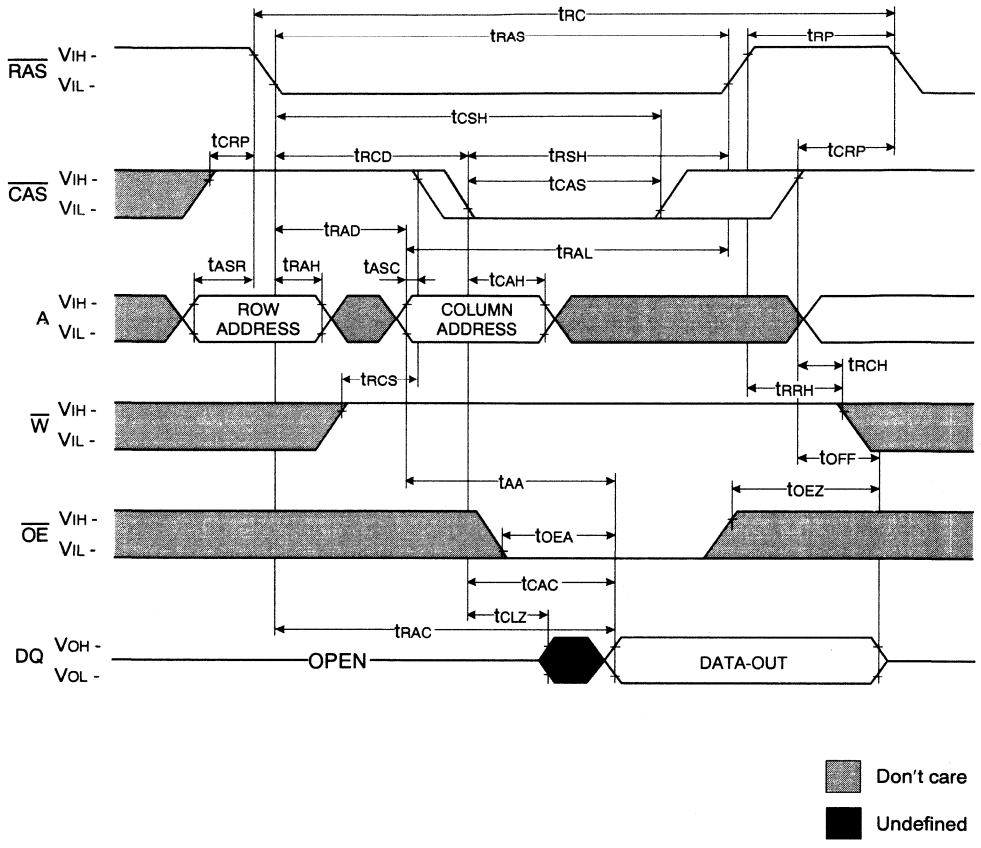


NOTE : This timing diagram is applied to all devices besides 16M DRAM 4th & 64M DRAM.

FP $\overline{OE}$ controlled Timing



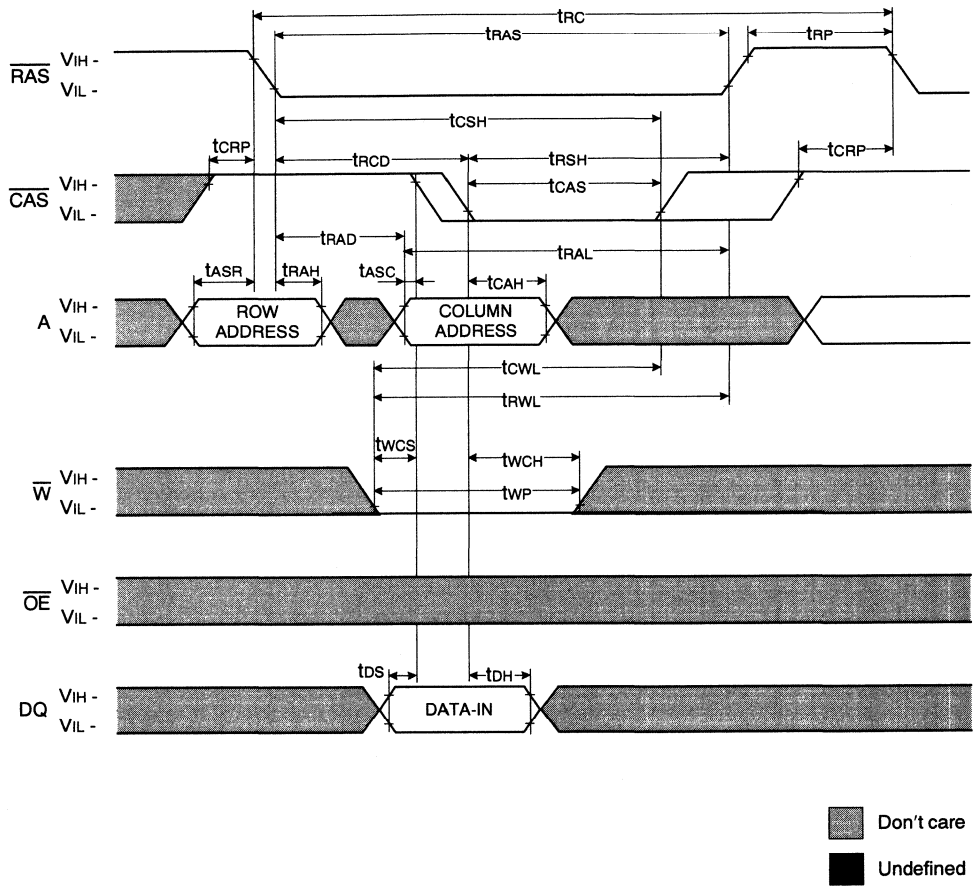
READ CYCLE



SAMSUNG ELECTRONICS

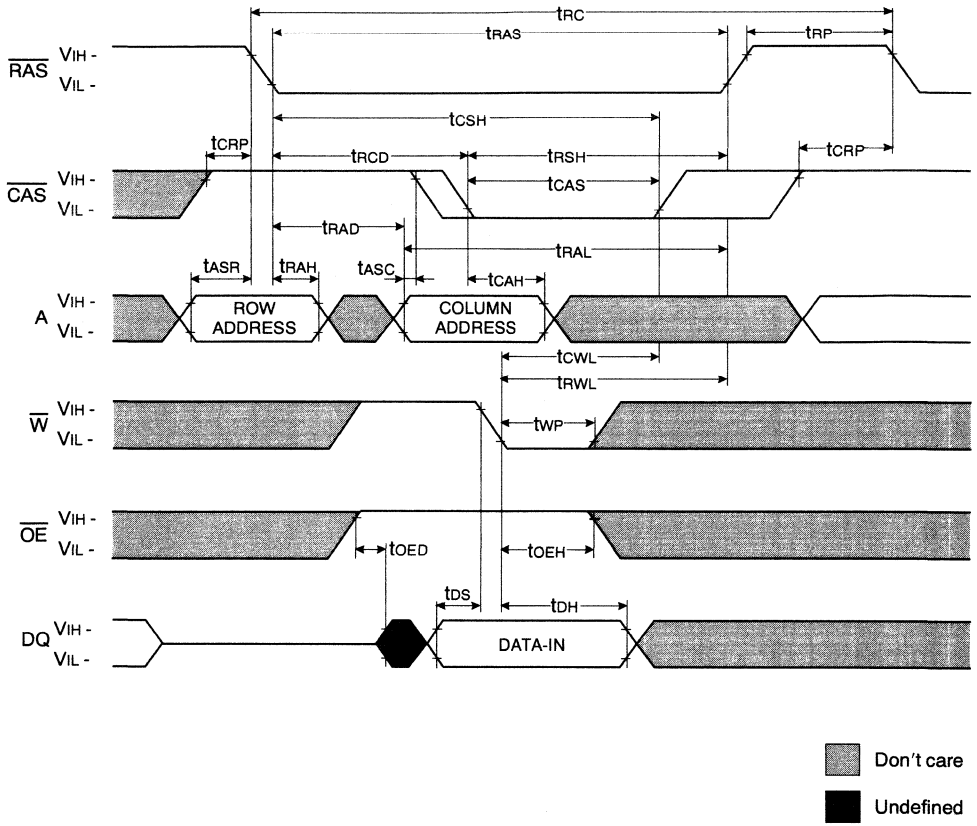
WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



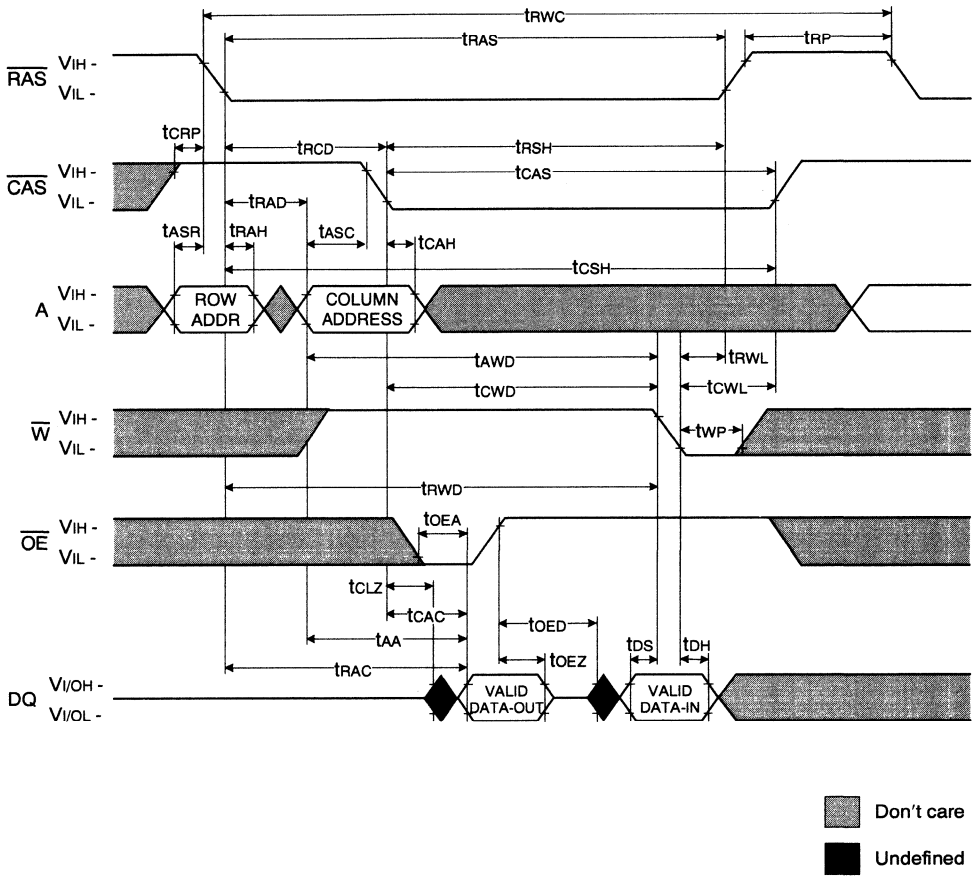
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : DOUT = OPEN



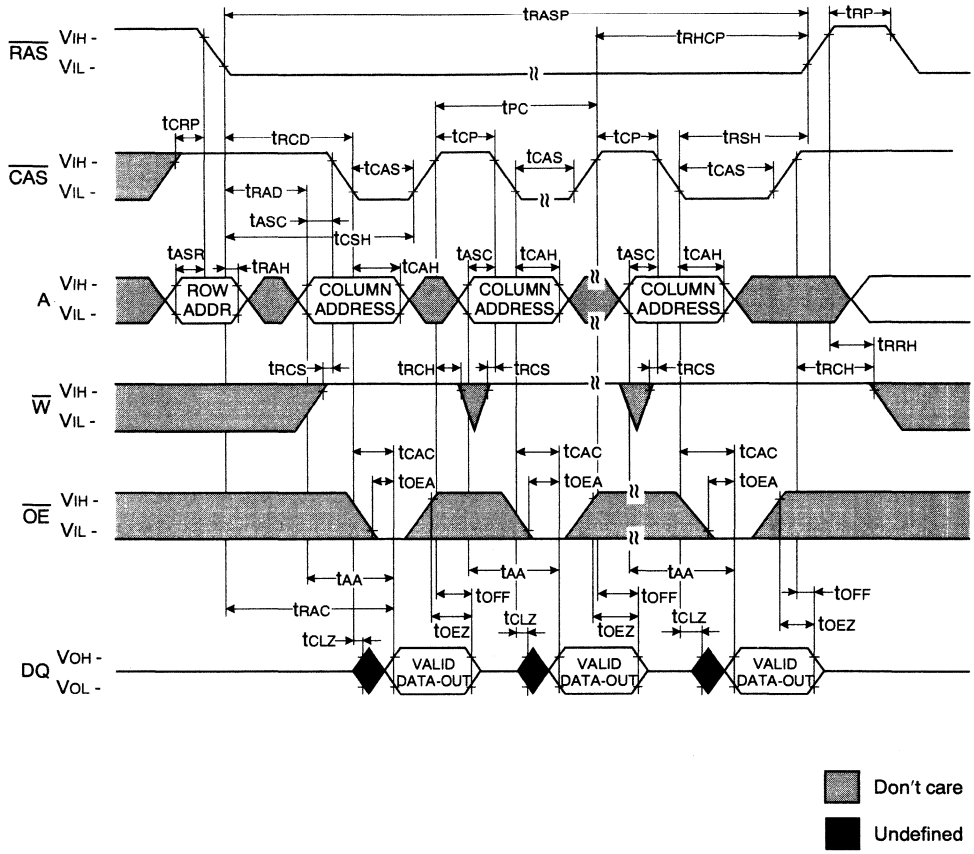
5

READ - MODIFY - WRTIE CYCLE



FAST PAGE READ CYCLE

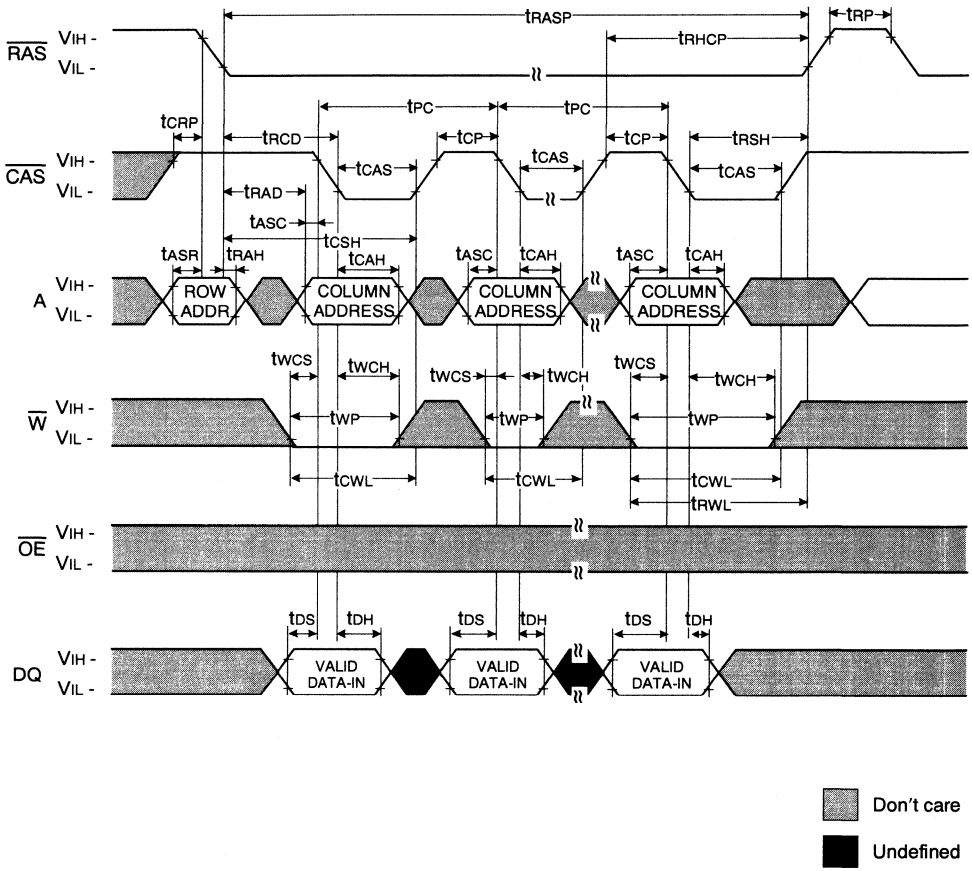
NOTE : DOUT = OPEN



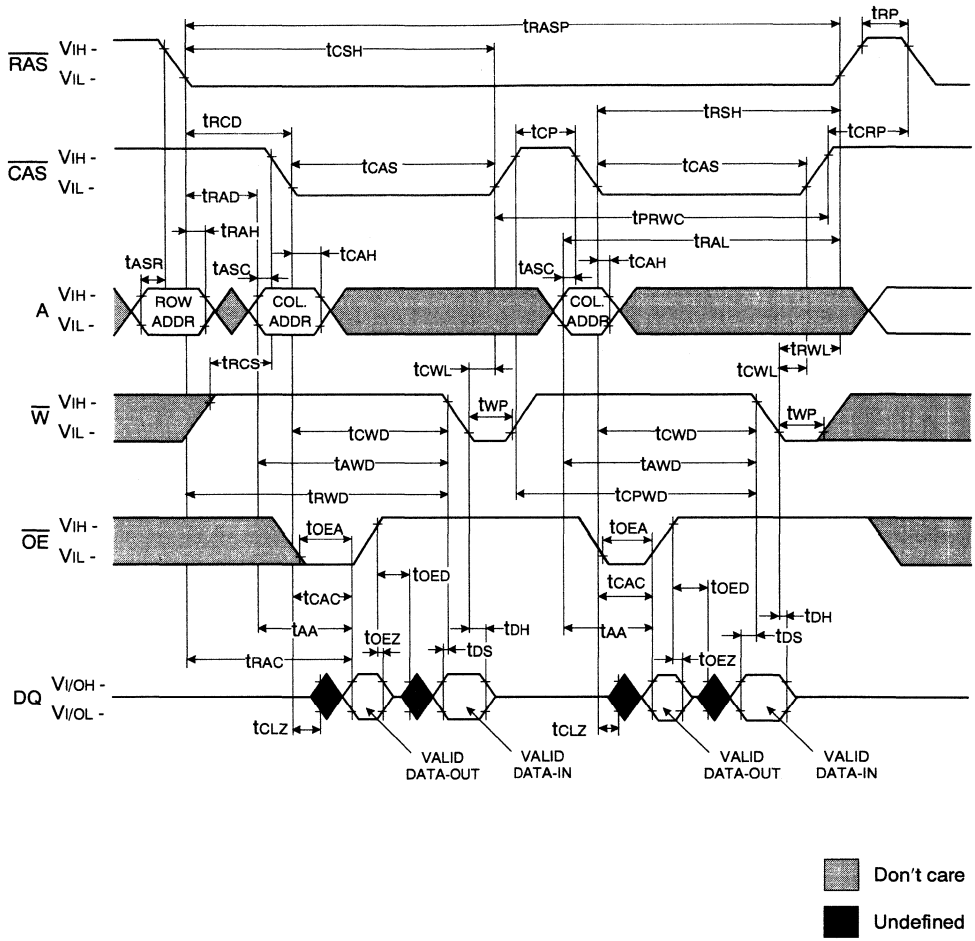
5

FAST PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

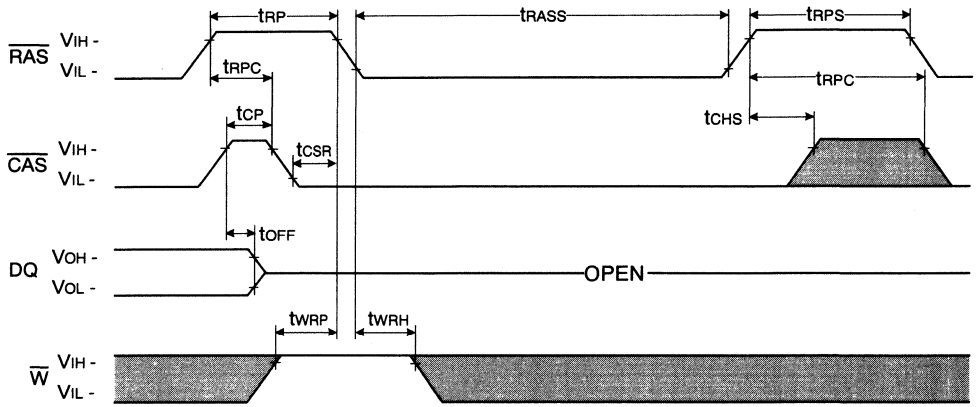


FAST PAGE READ - MODIFY - WRITE CYCLE



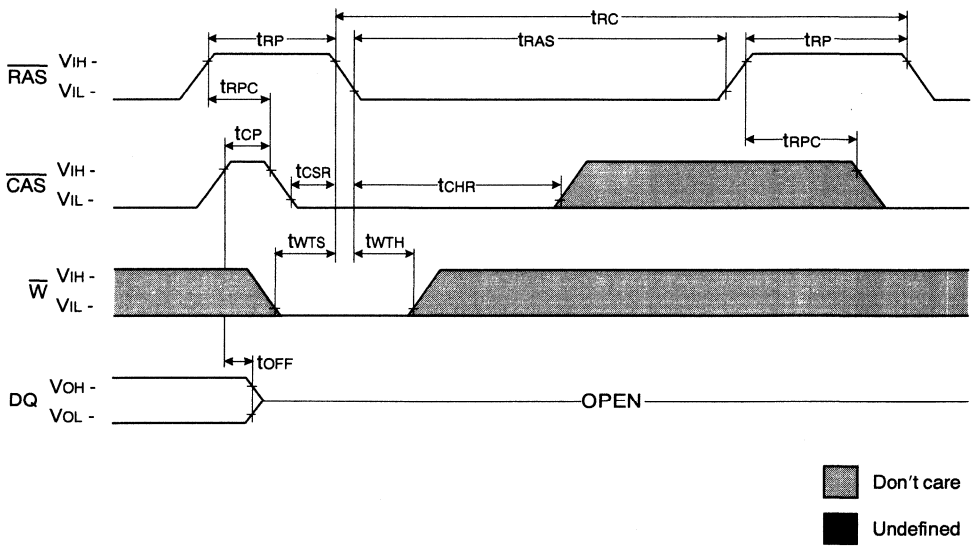
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



TEST MODE IN CYCLE

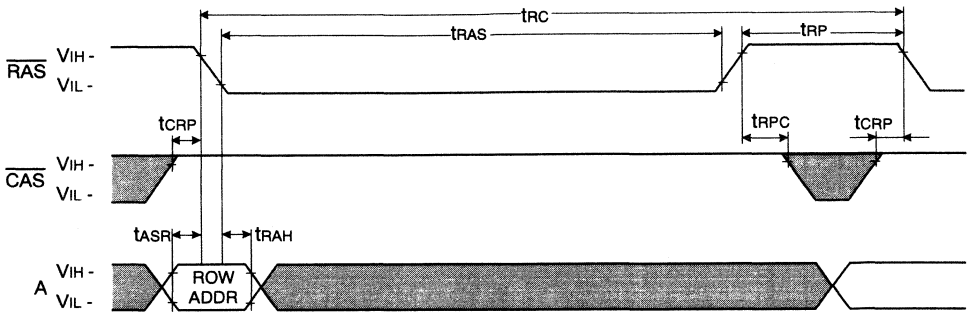
NOTE : $\overline{OE}$, A = Don't care



$\overline{RAS}$ - ONLY REFRESH CYCLE

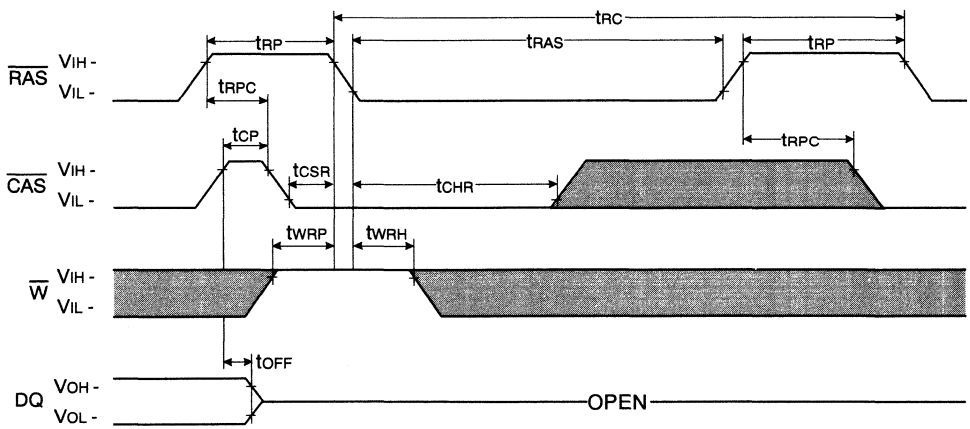
NOTE : $\overline{W}$, $\overline{OE}$, DIN = Don't care

DOUT = OPEN



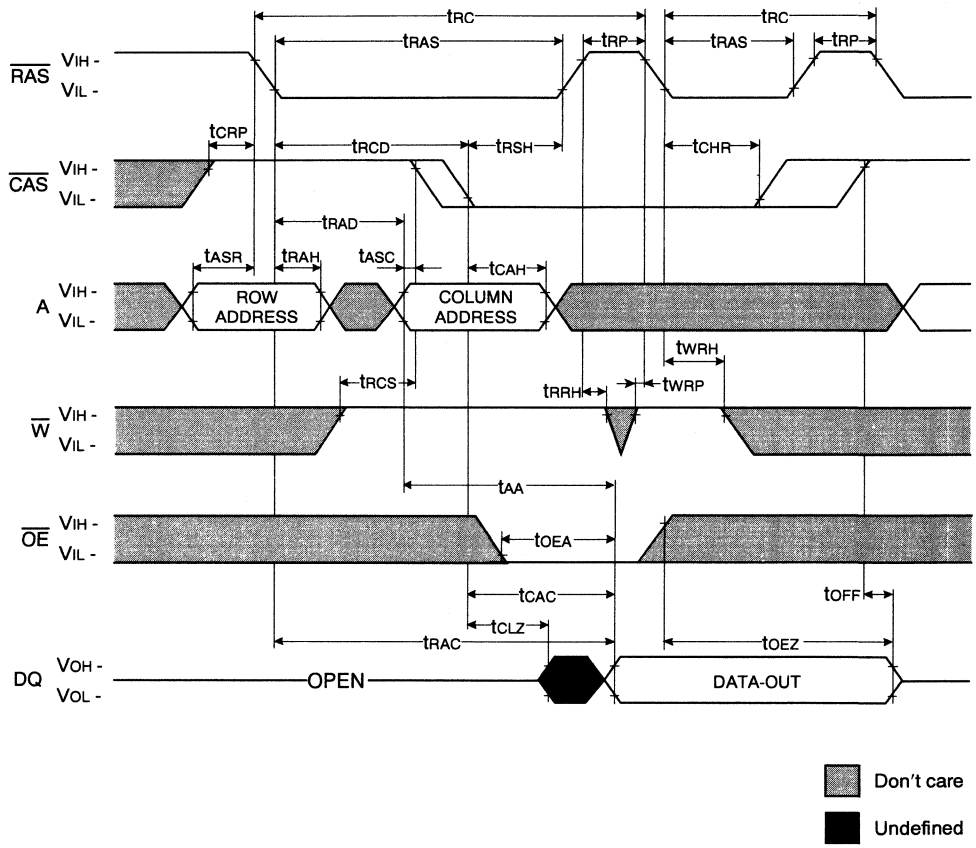
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



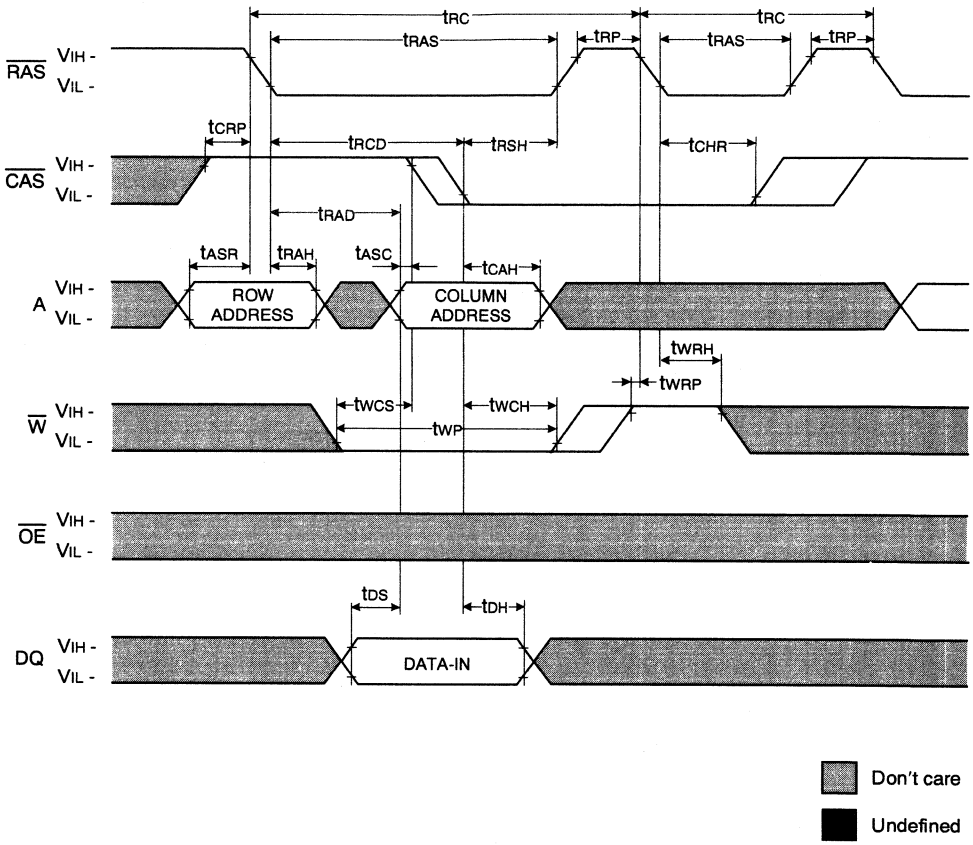
5

HIDDEN REFRESH CYCLE (READ)



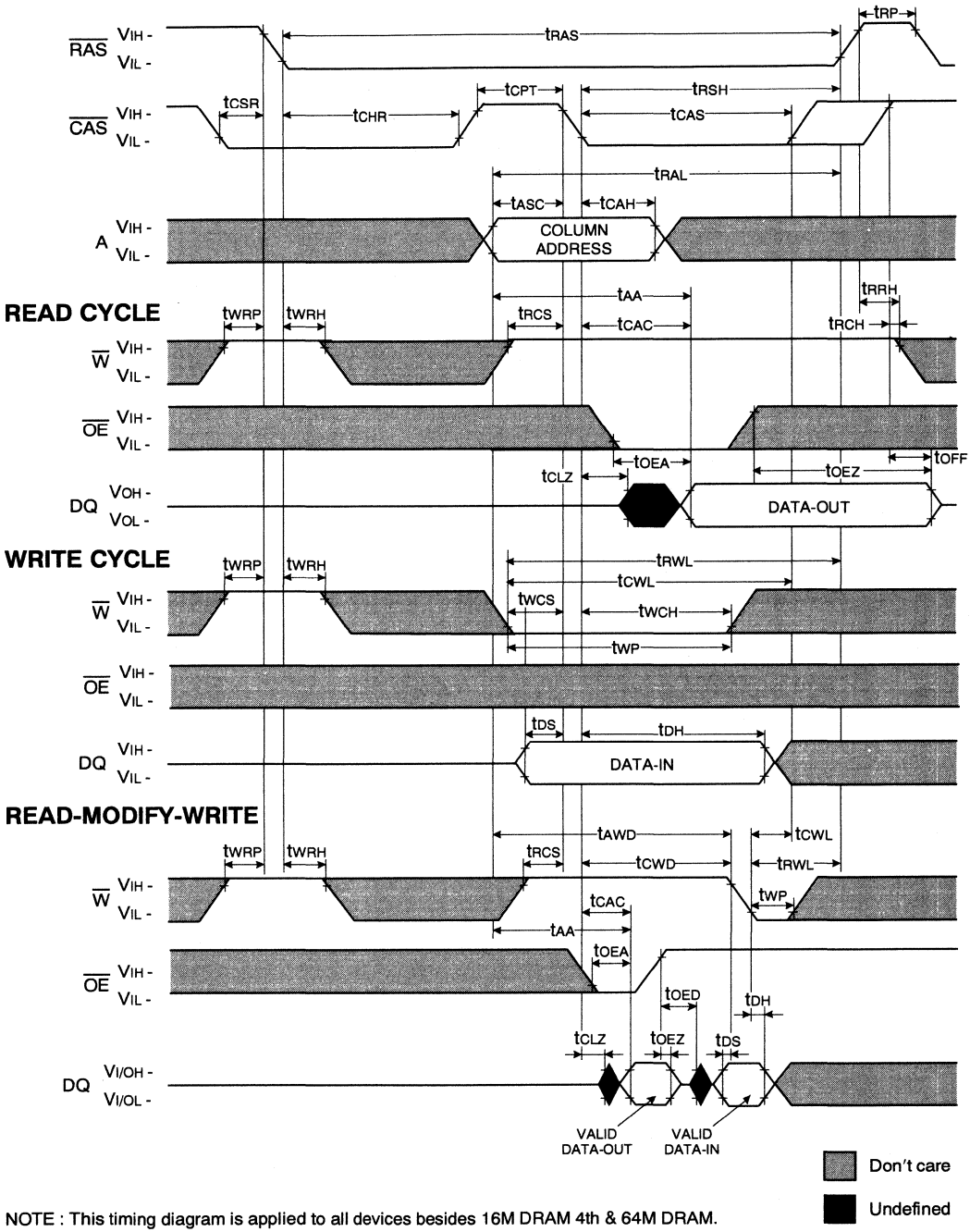
HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



5

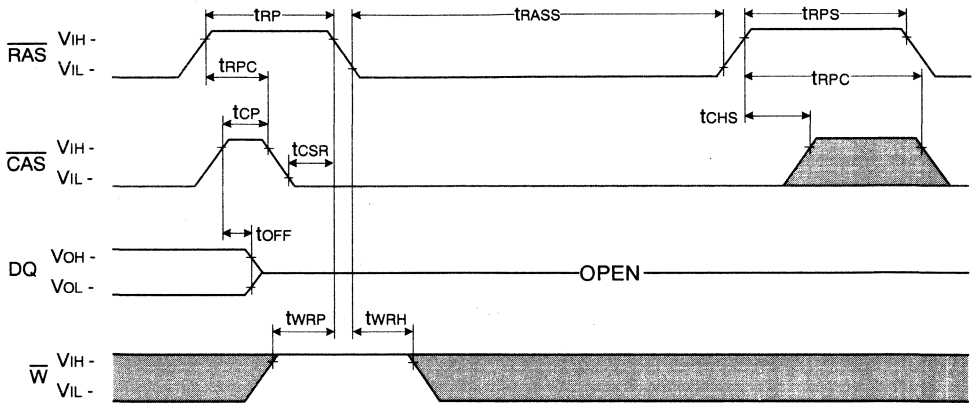
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



NOTE : This timing diagram is applied to all devices besides 16M DRAM 4th & 64M DRAM.

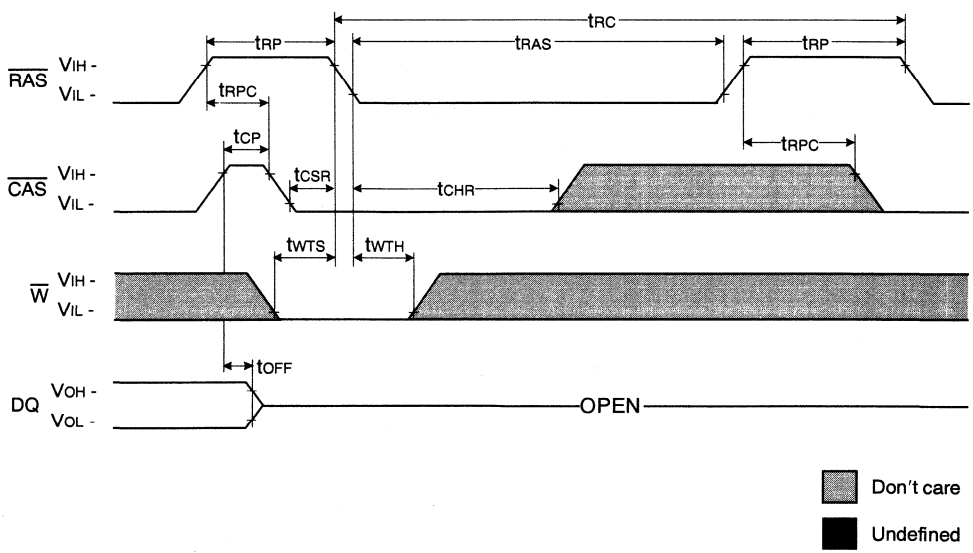
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



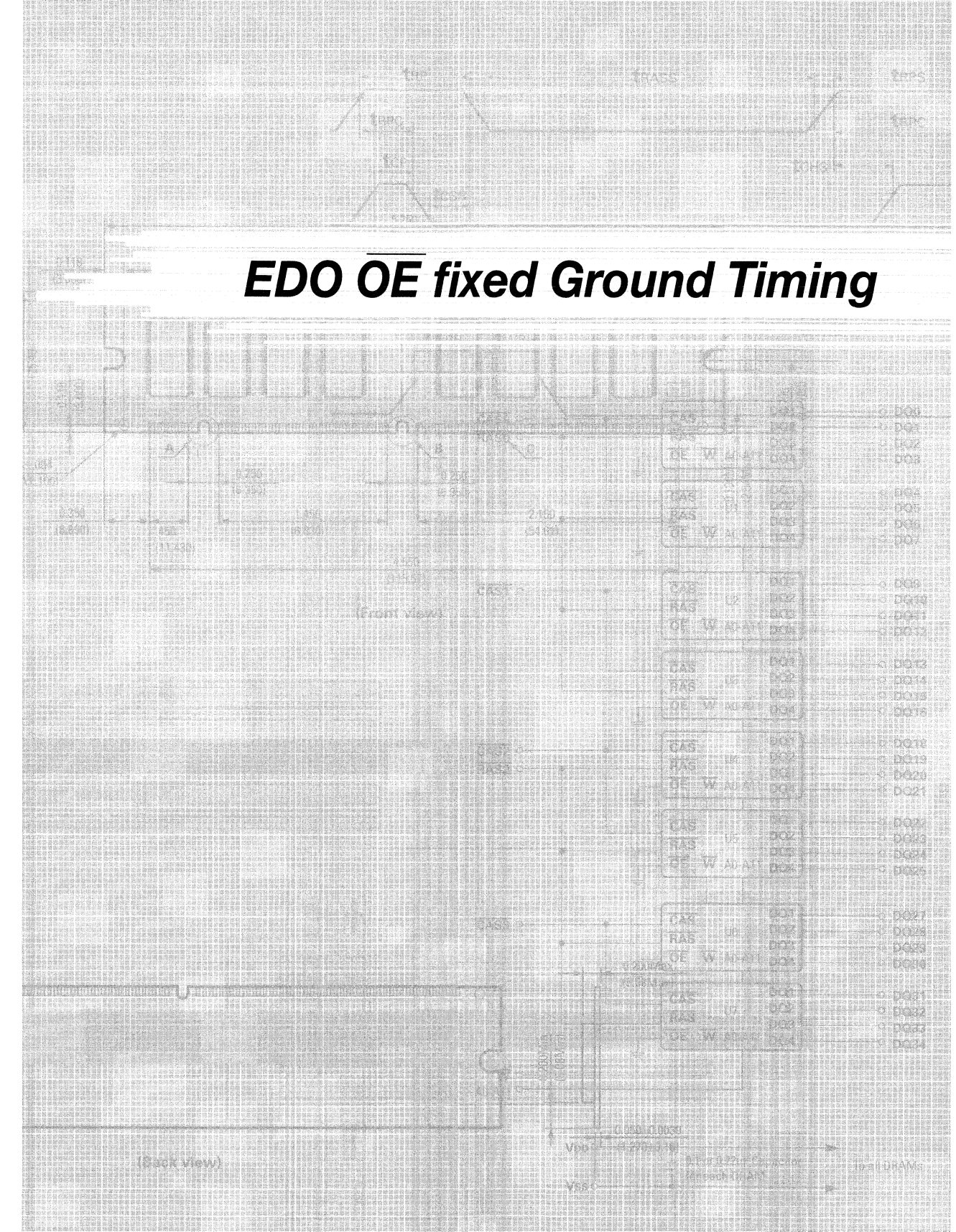
TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't care

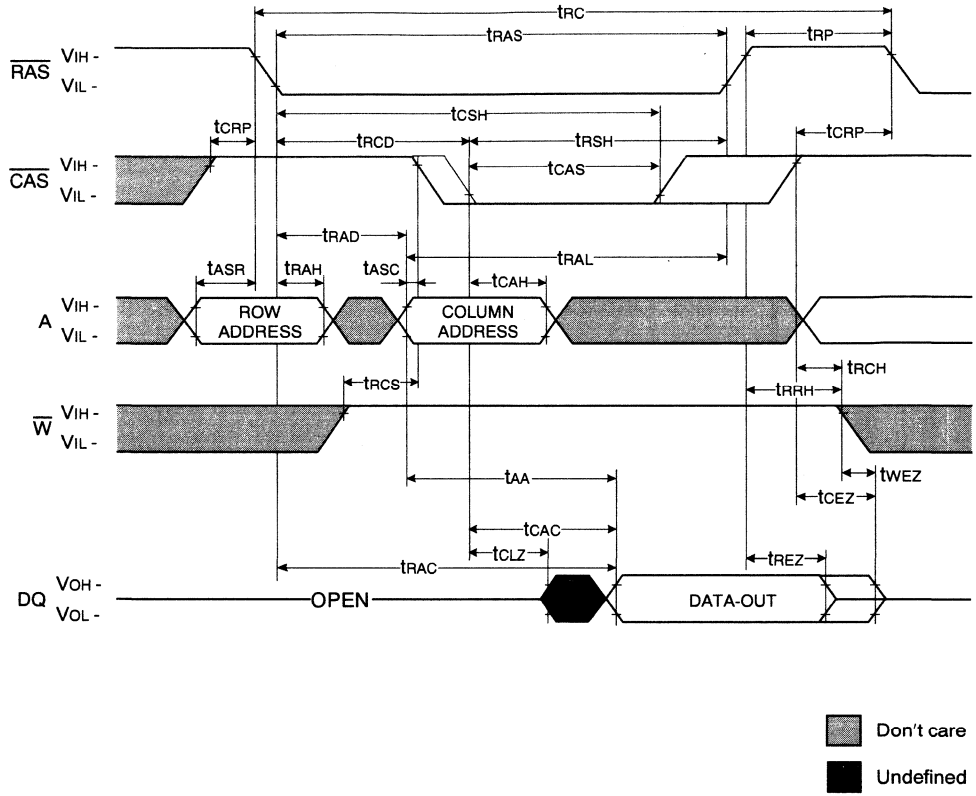


5

EDO $\overline{OE}$ fixed Ground Timing



READ CYCLE

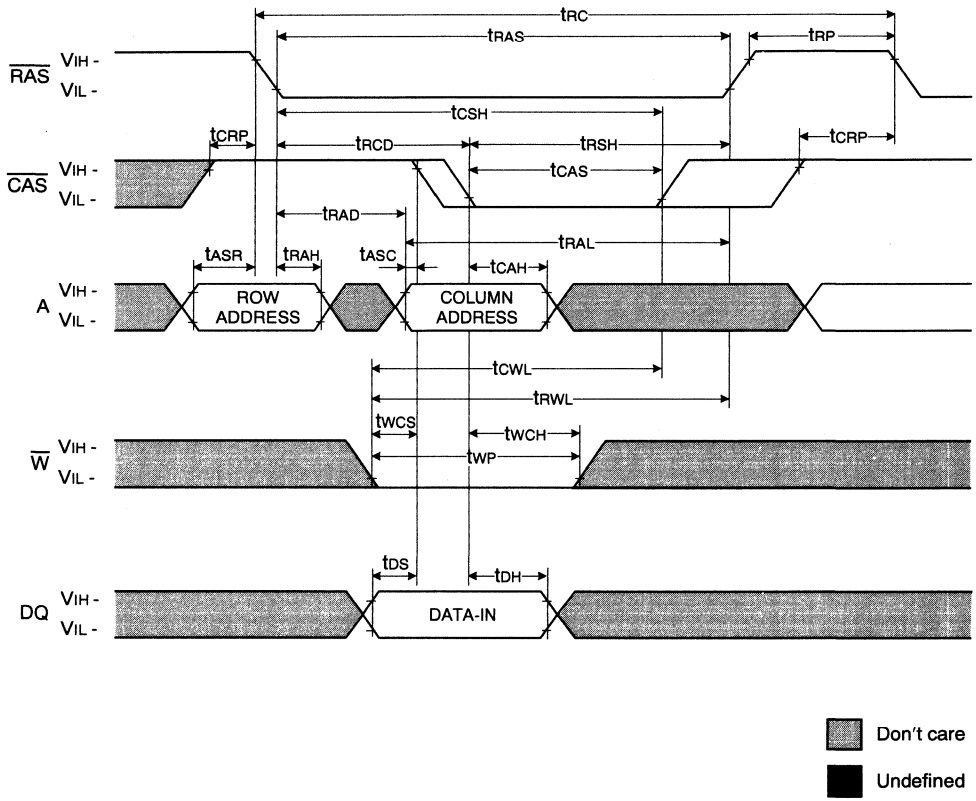


5

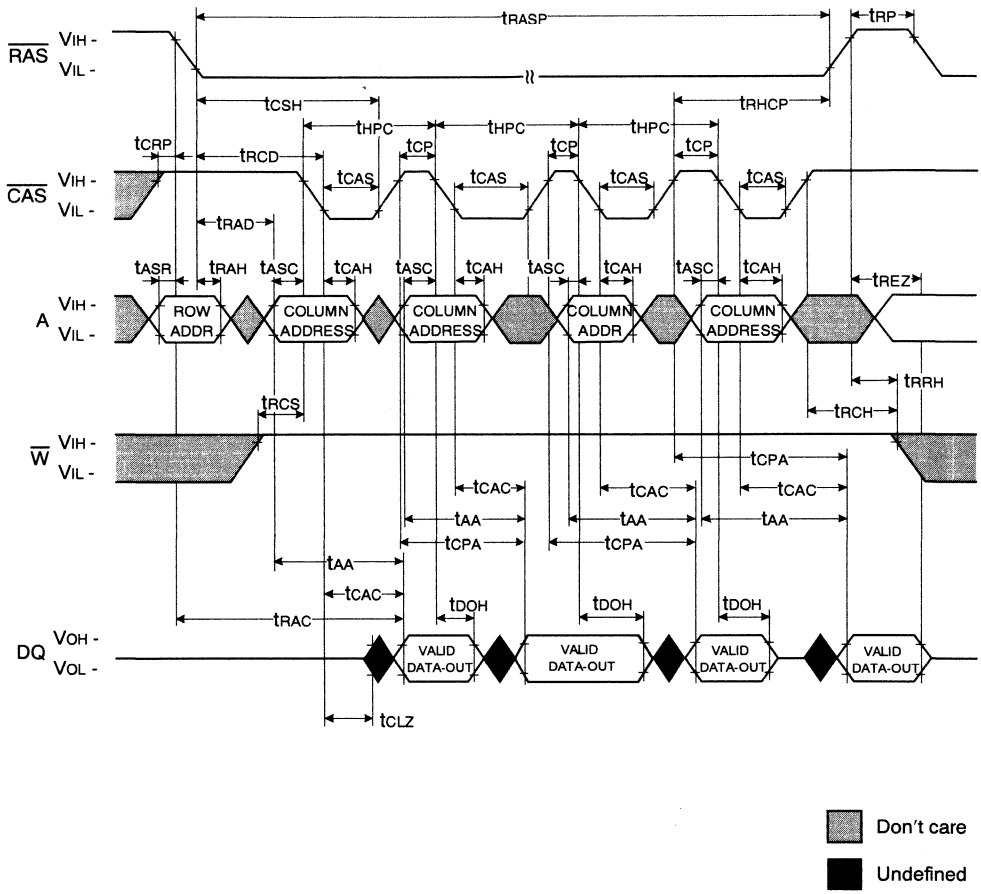
SAMSUNG ELECTRONICS

WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

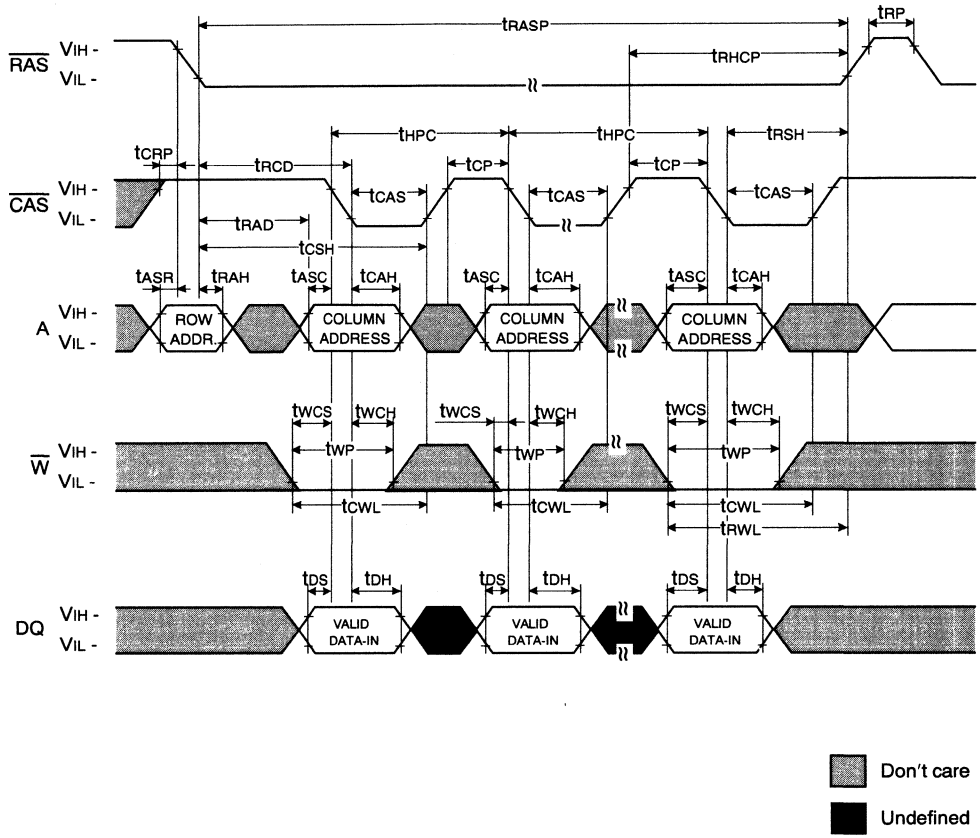


HYPER PAGE READ CYCLE



HYPER PAGE WRITE CYCLE (EARLY WRITE)

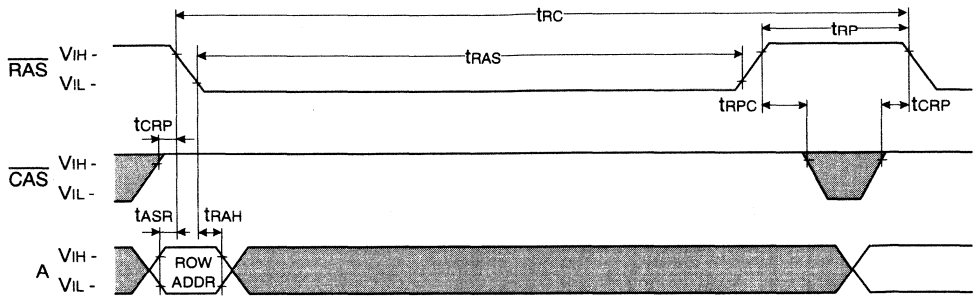
NOTE : DOUT = OPEN



$\overline{RAS}$ - ONLY REFRESH CYCLE*

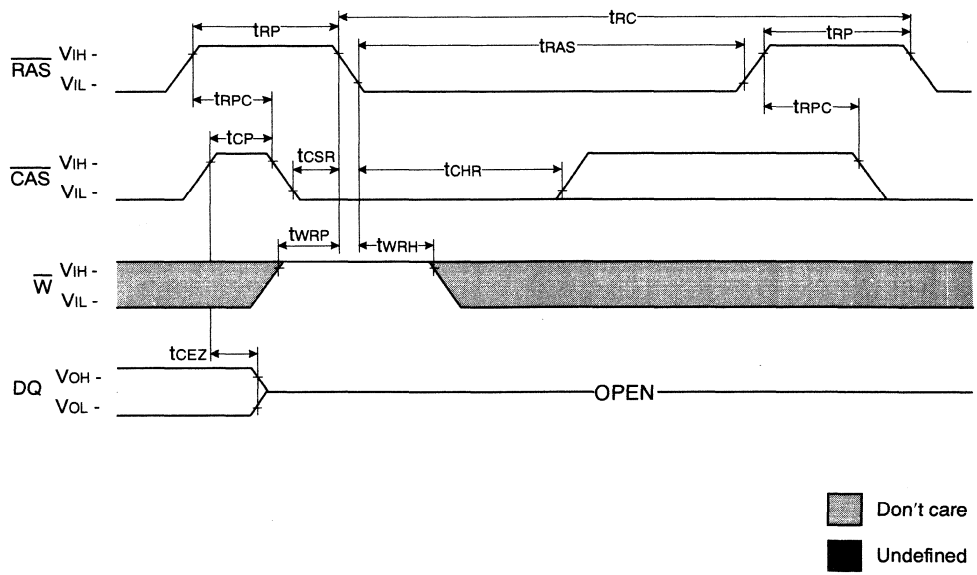
NOTE : $\overline{W}$, $\overline{OE}$, DIN = Don't care

DOUT = OPEN



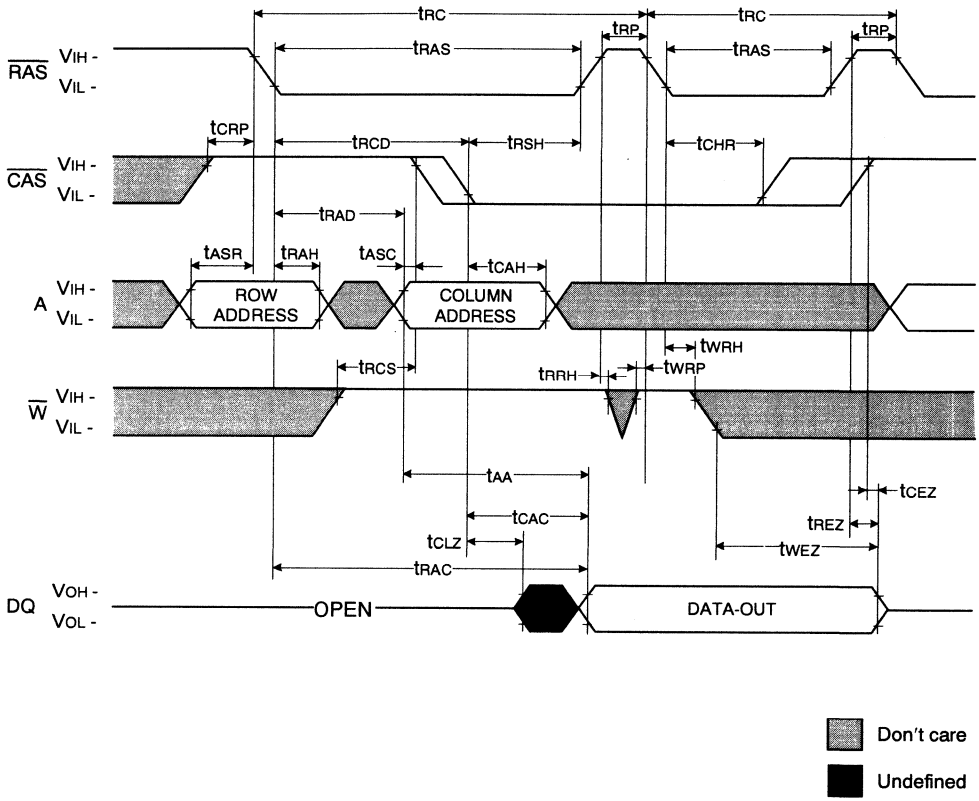
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



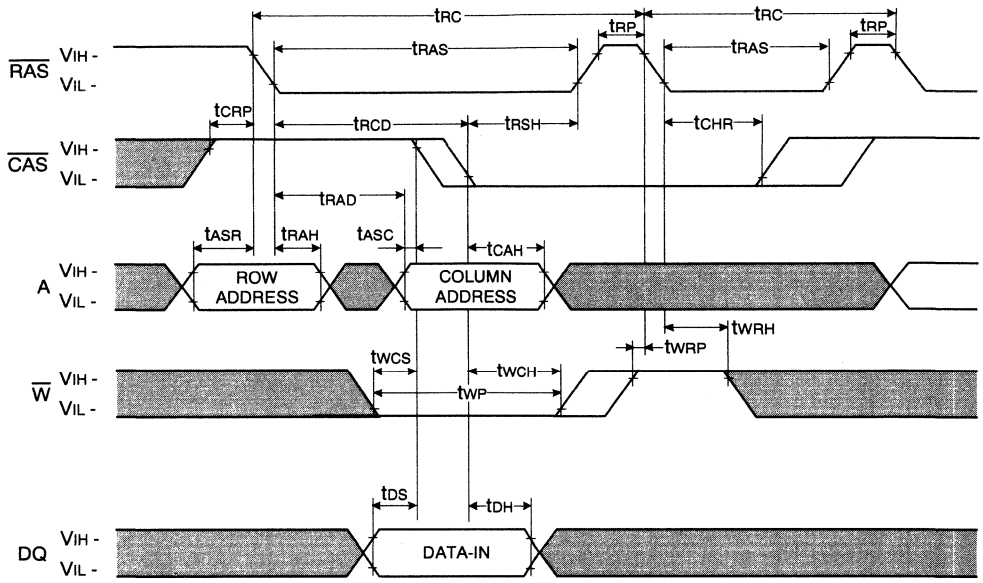
* In $\overline{RAS}$-only refresh cycle of 64Mb A-dile & B-die, when $\overline{CAS}$ signal transits from Low to High, the valid data may be cut off.

HIDDEN REFRESH CYCLE (READ)



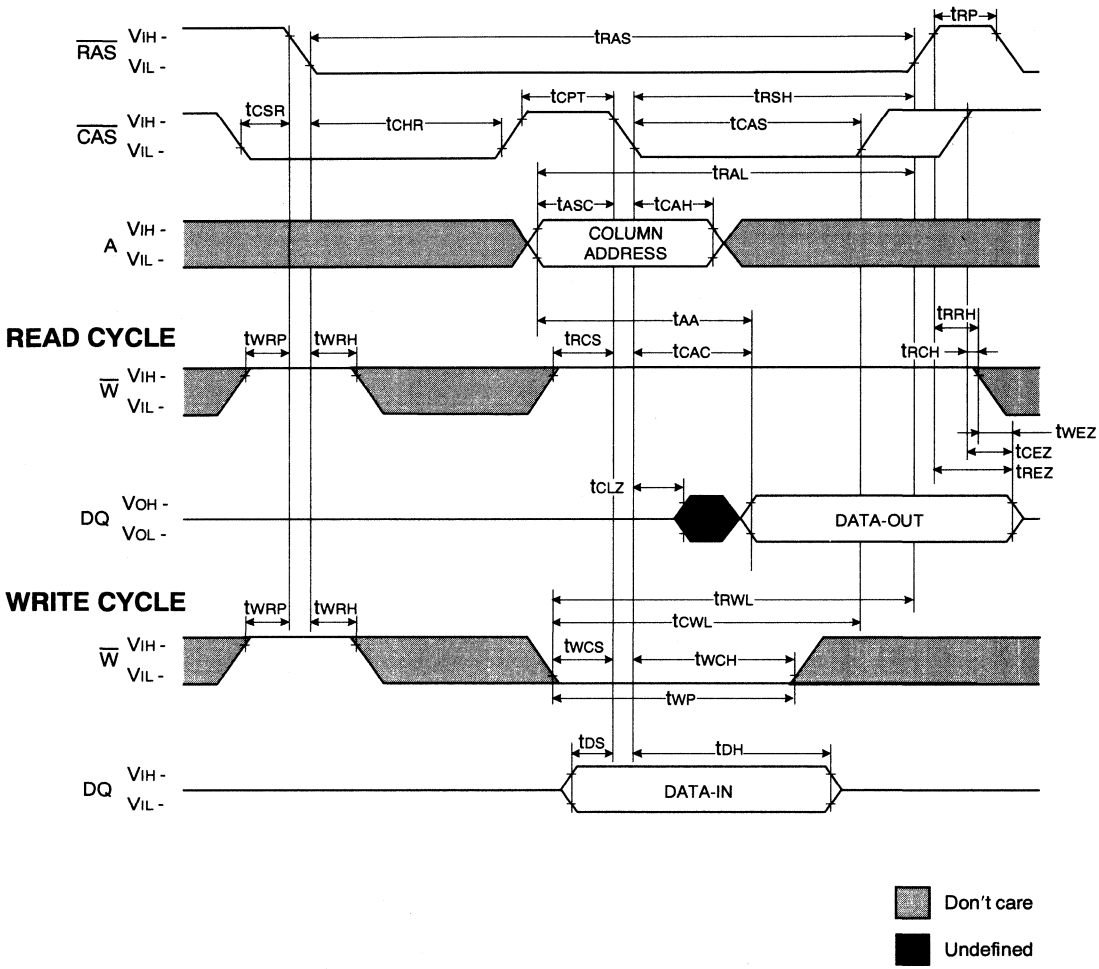
HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



5

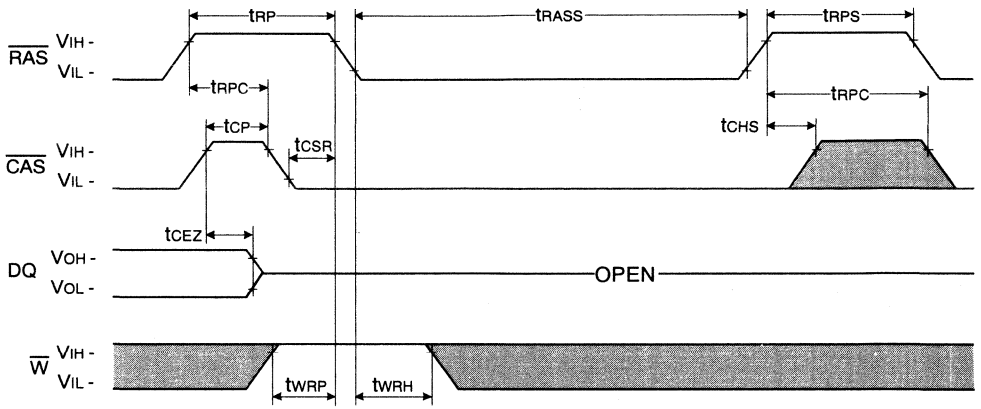
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

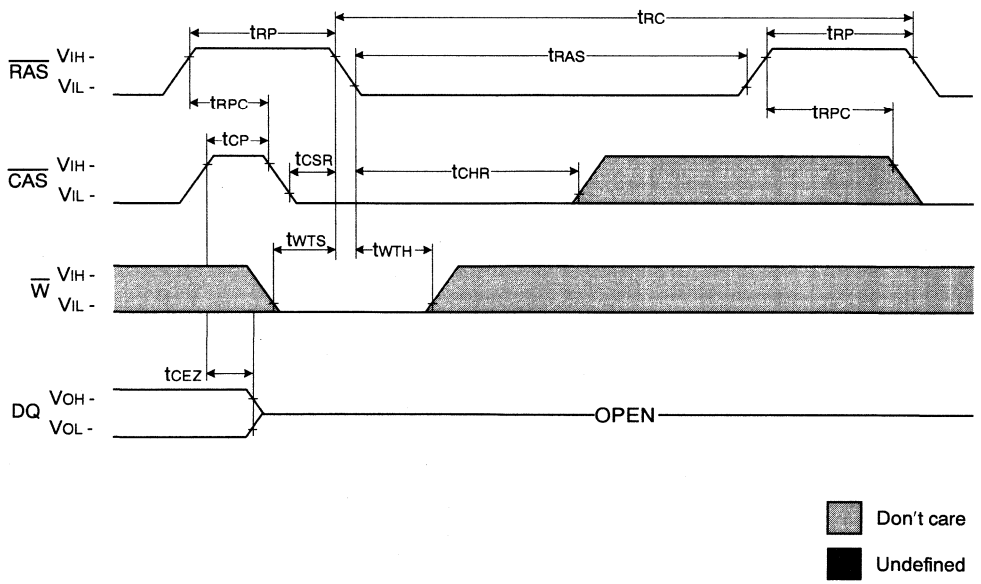
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care

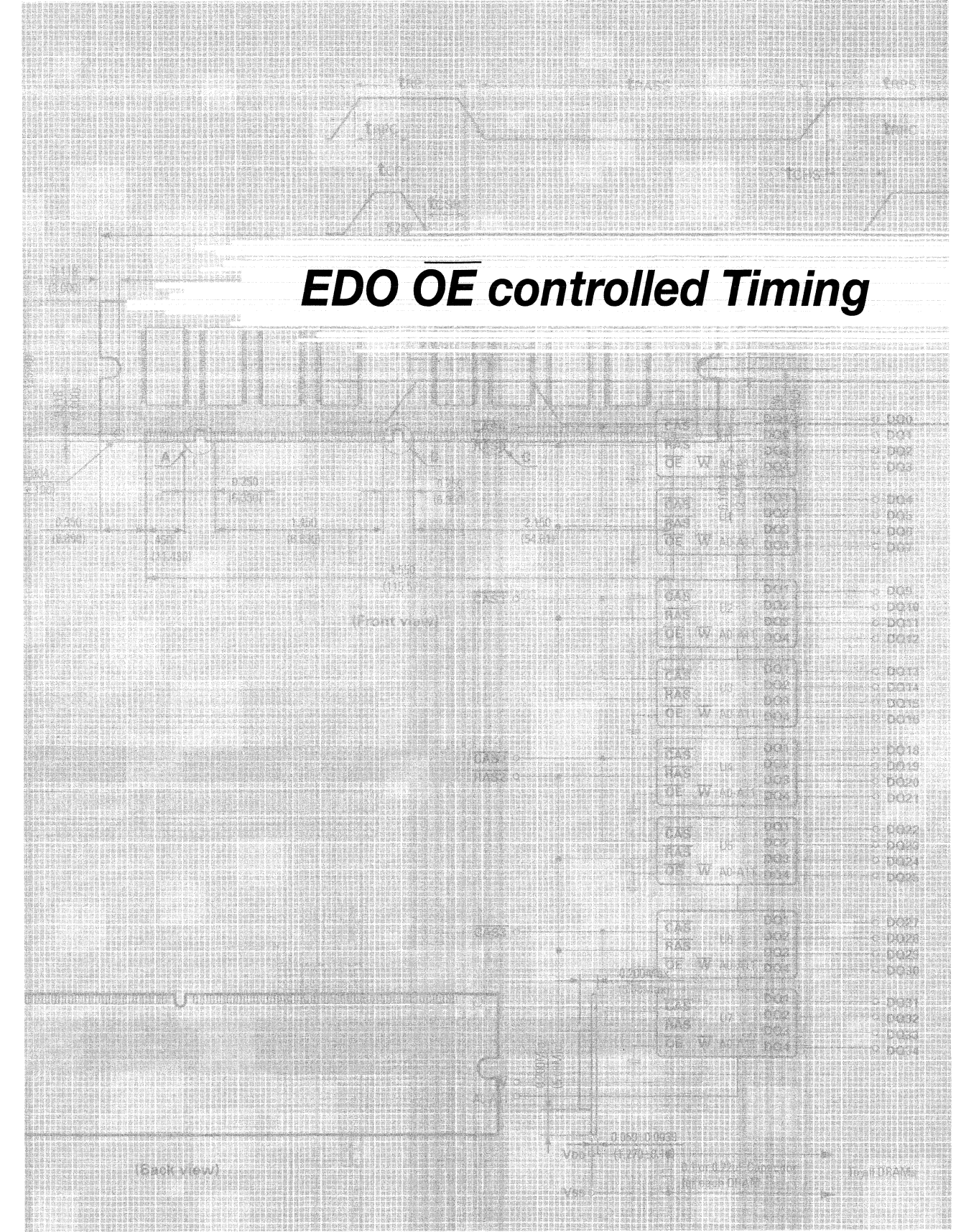


TEST MODE IN CYCLE

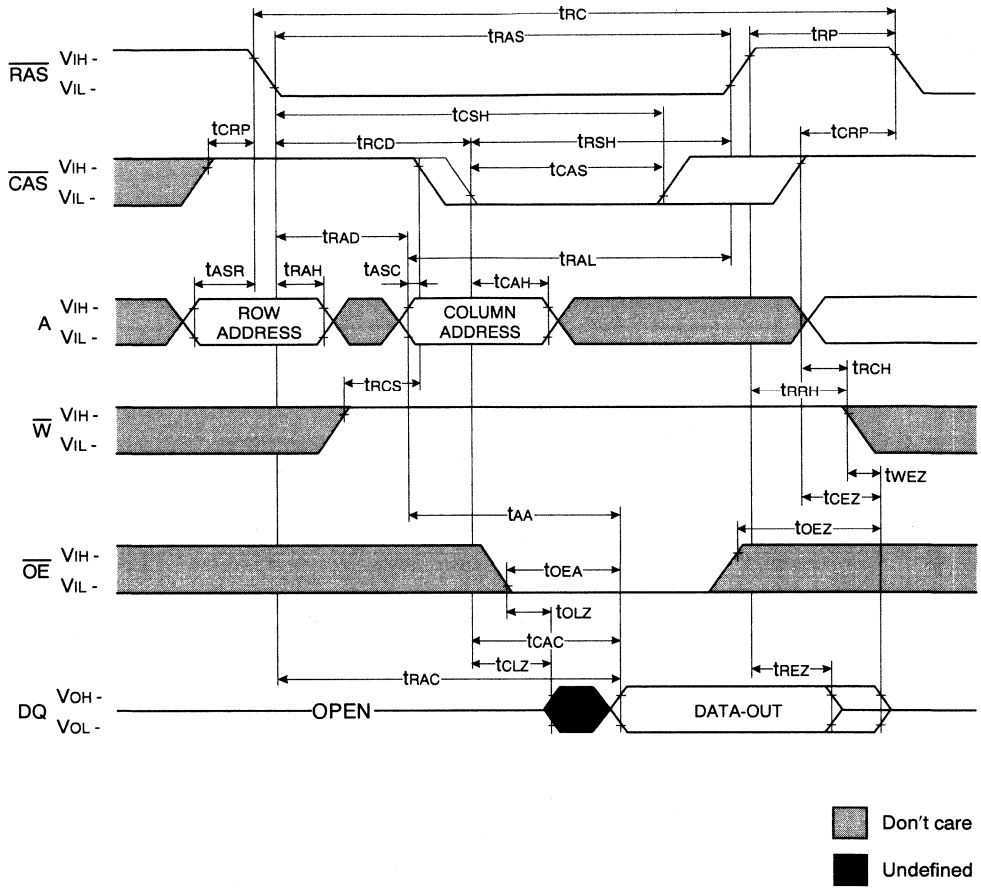
NOTE : $\overline{OE}$, A = Don't care



EDO $\overline{OE}$ controlled Timing



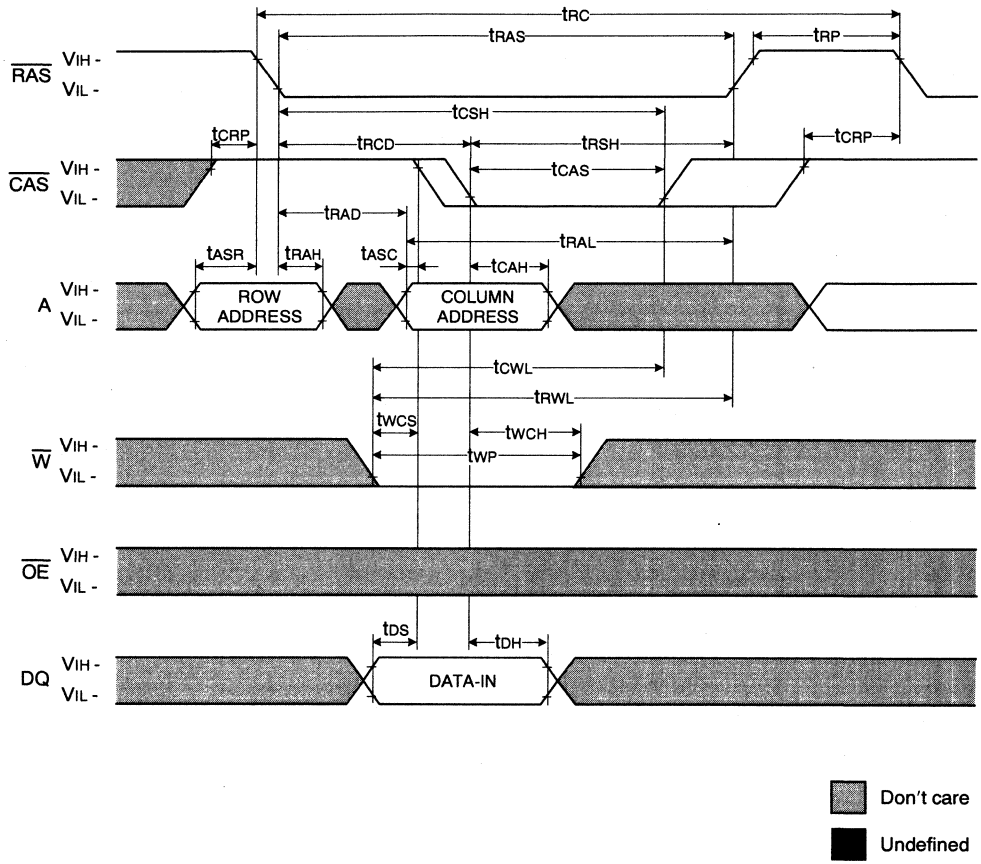
READ CYCLE


tRC
tRAS
tRP
RAS
VIH -
VIL -
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A
ROW ADDRESS
COLUMN ADDRESS
tRCH
tRCS
tRRH
W
tWEZ
tCEZ
tAA
tOEZ
OE
tOEA
tOLZ
tCAC
tCLZ
tREZ
tRAC
DQ
VOH -
VOL -
OPEN
DATA-OUT
Don't care
Undefined

5

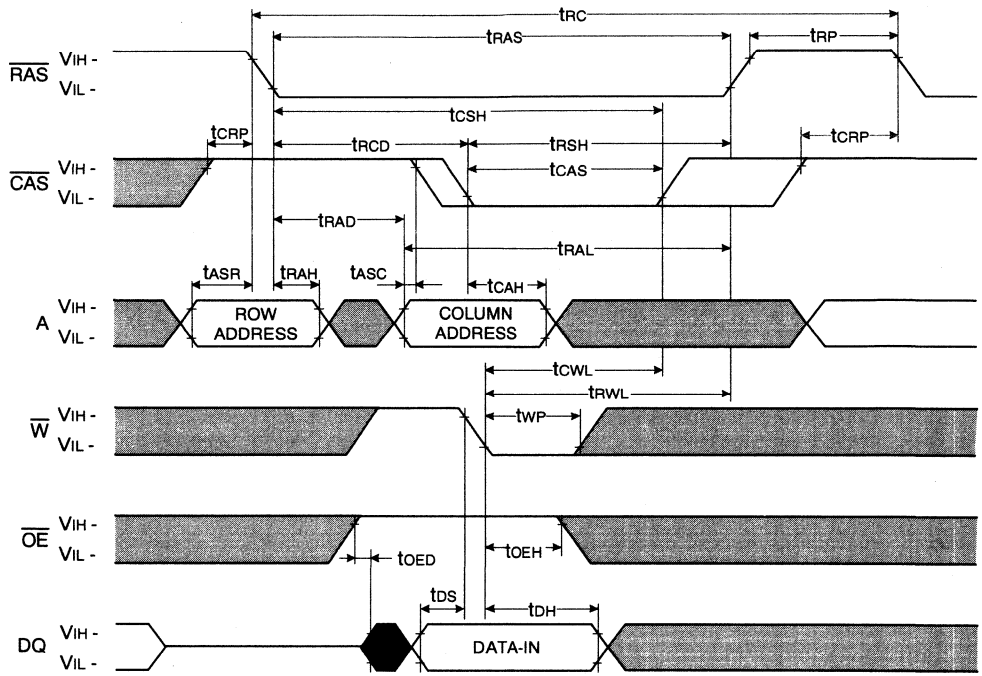
WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : DOUT = OPEN

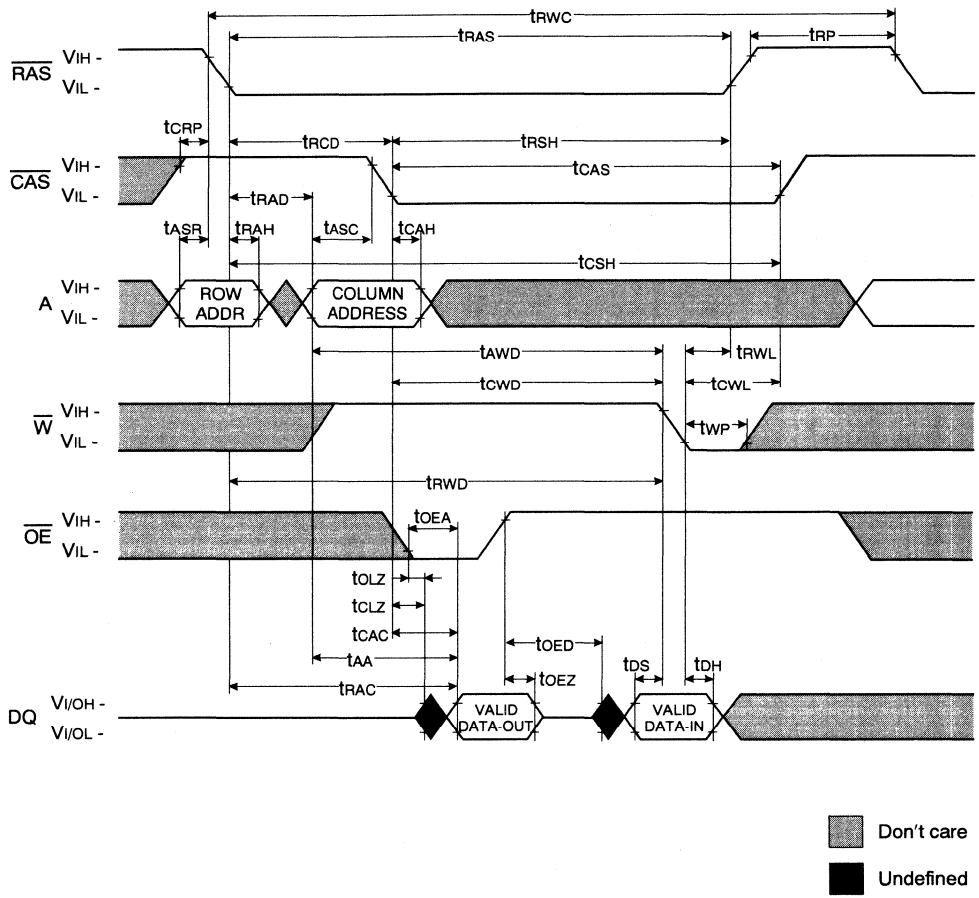


Don't care

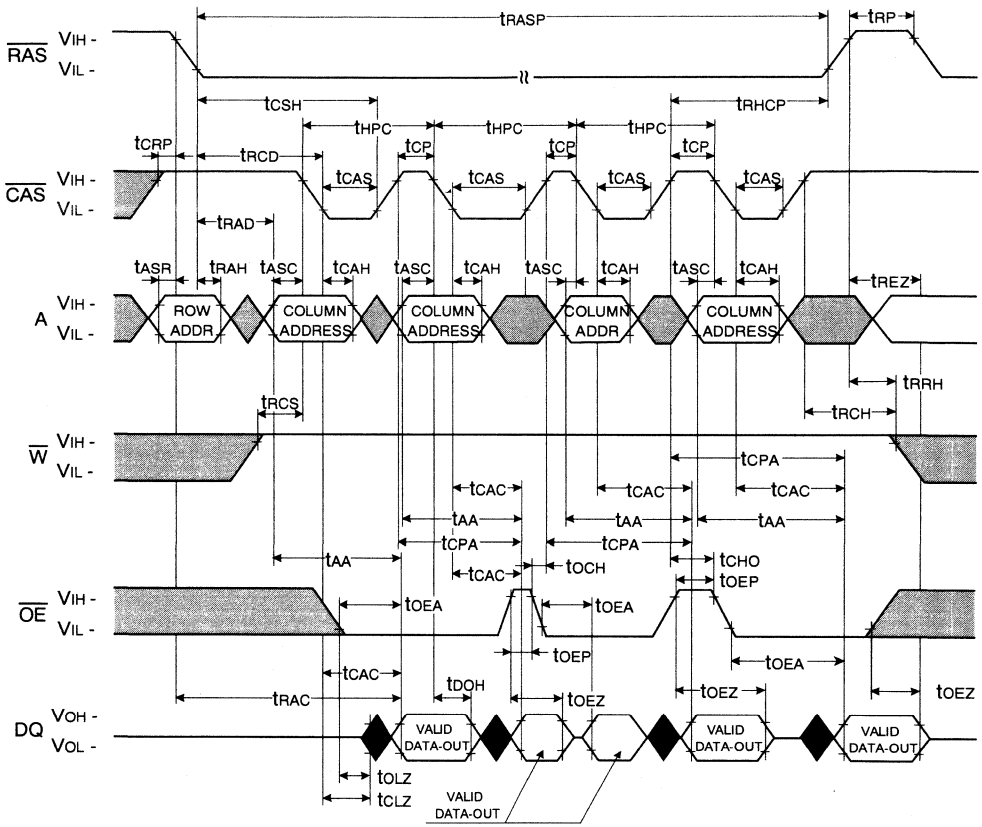
Undefined

5

READ - MODIFY - WRITE CYCLE

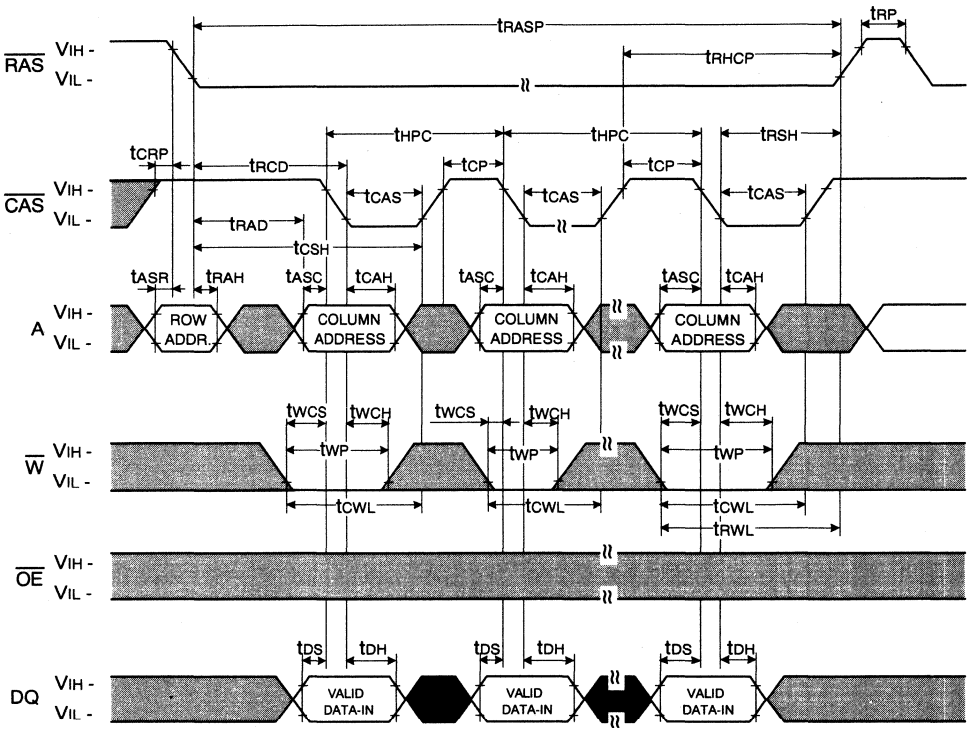


HYPER PAGE READ CYCLE

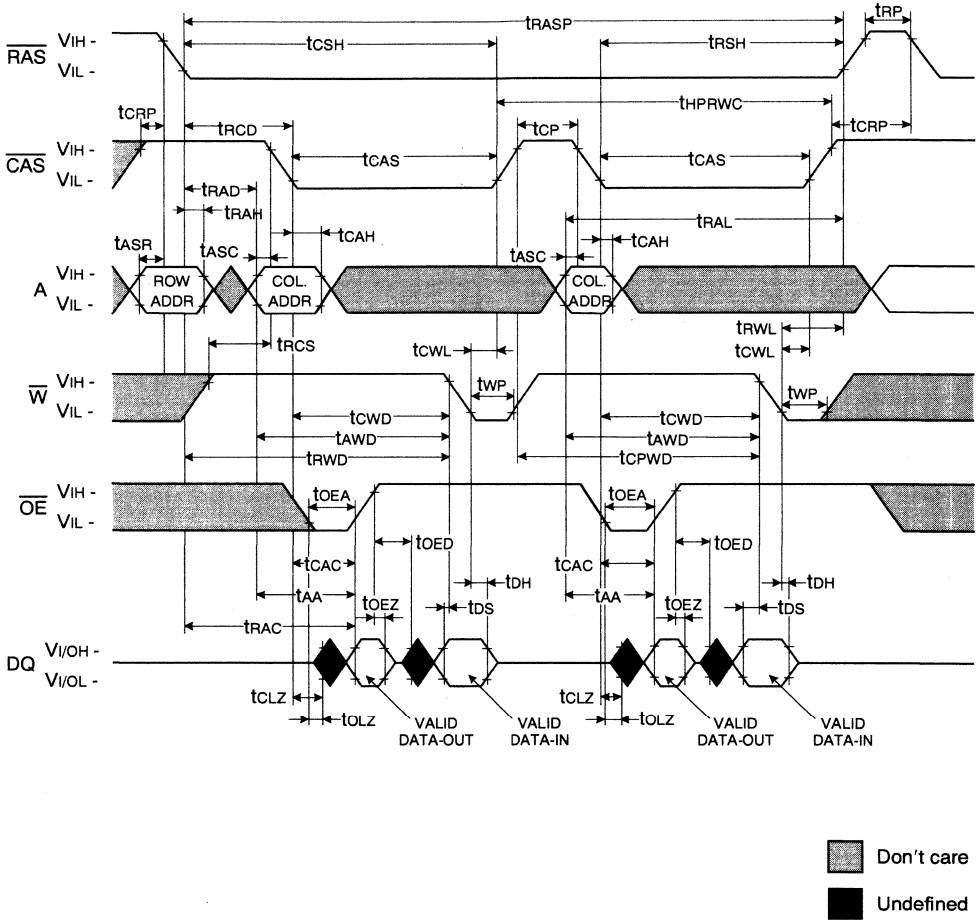


HYPER PAGE WRITE CYCLE (EARLY WRITE)

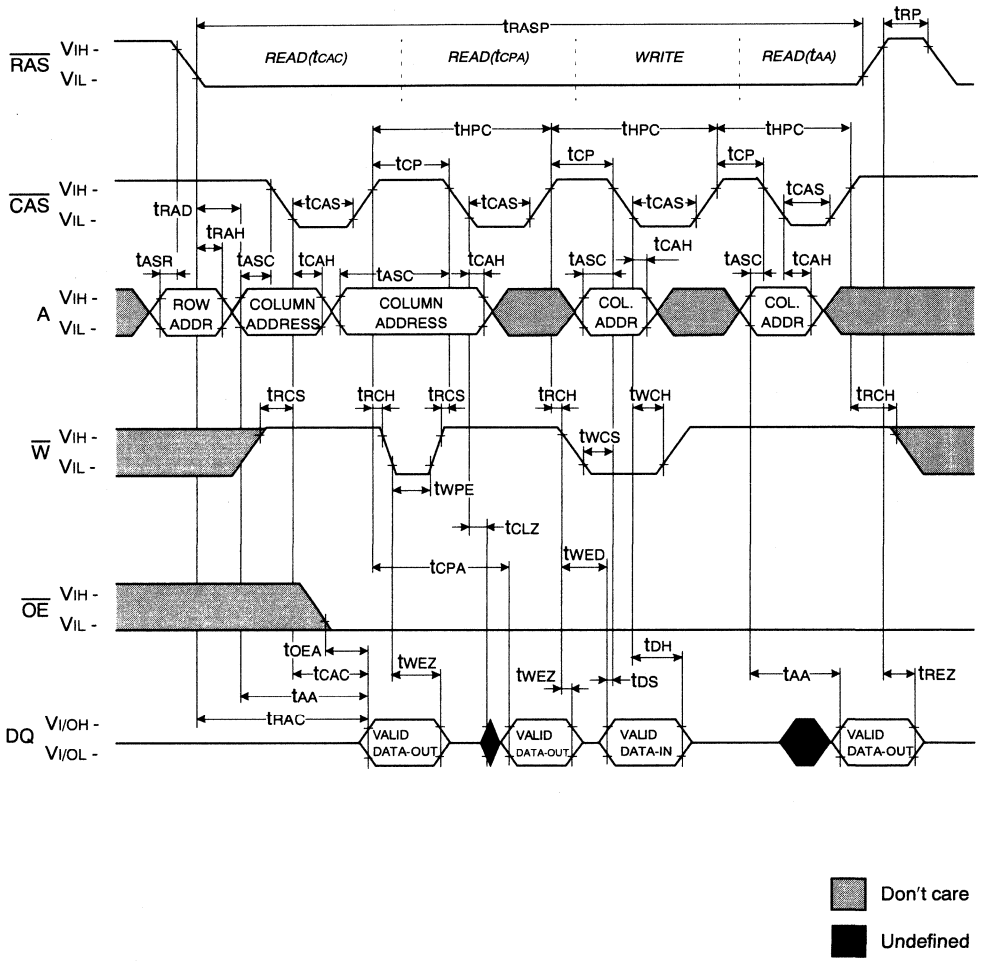
NOTE : DOUT = OPEN



HYPER PAGE READ-MODIFY-WRITE CYCLE



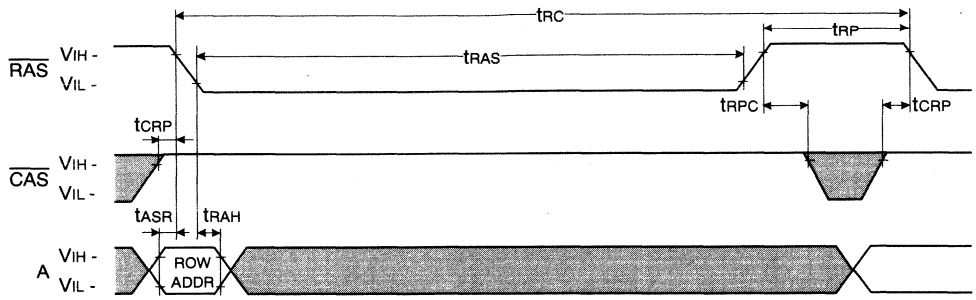
HYPER PAGE READ AND WRITE MIXED CYCLE



$\overline{RAS}$ - ONLY REFRESH CYCLE*

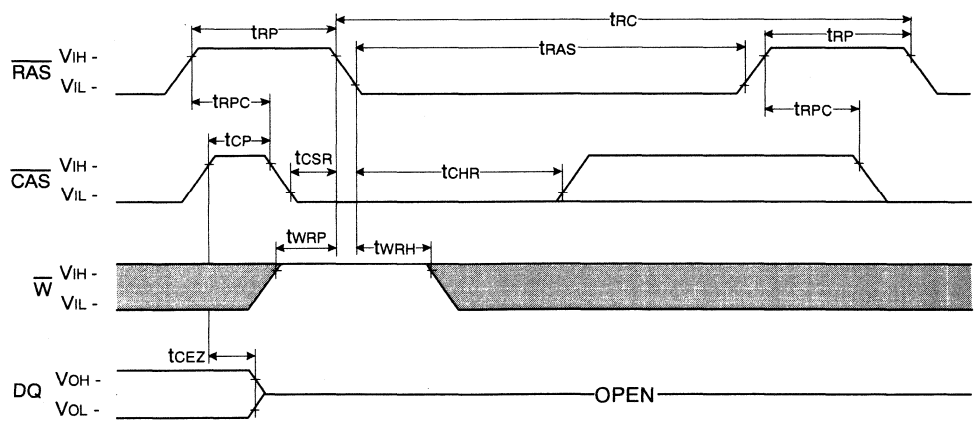
NOTE : $\overline{W}$, $\overline{OE}$, DIN = Don't care

DOUT = OPEN



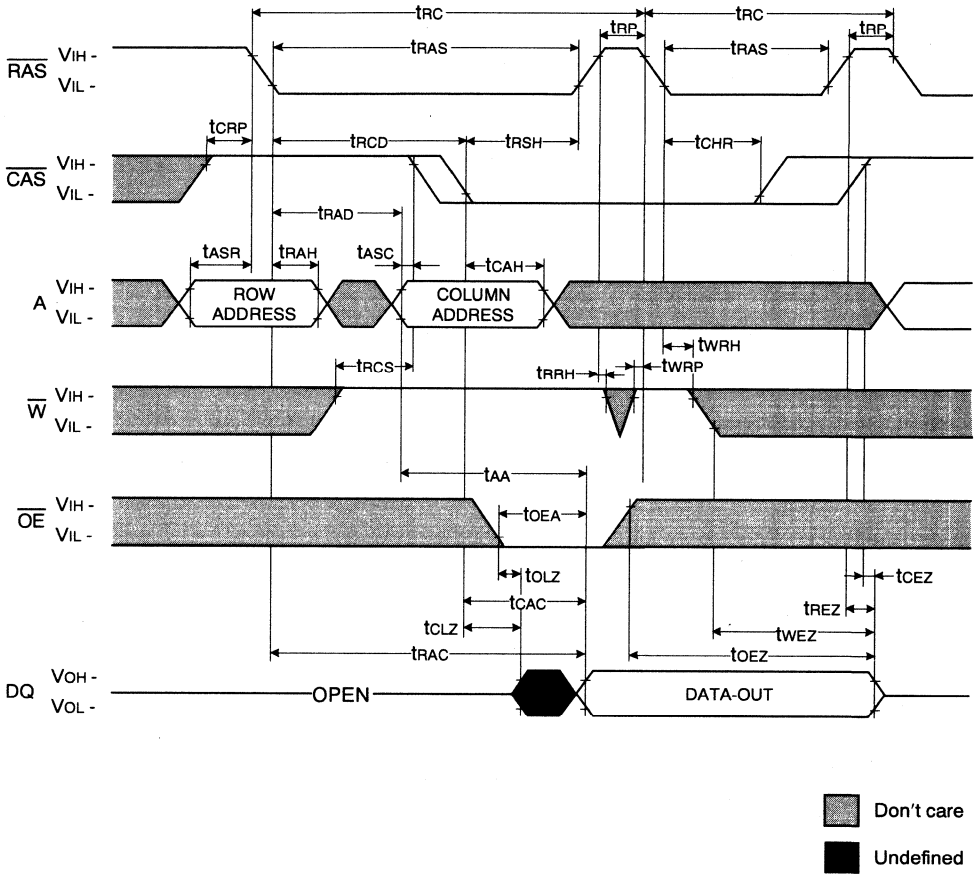
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



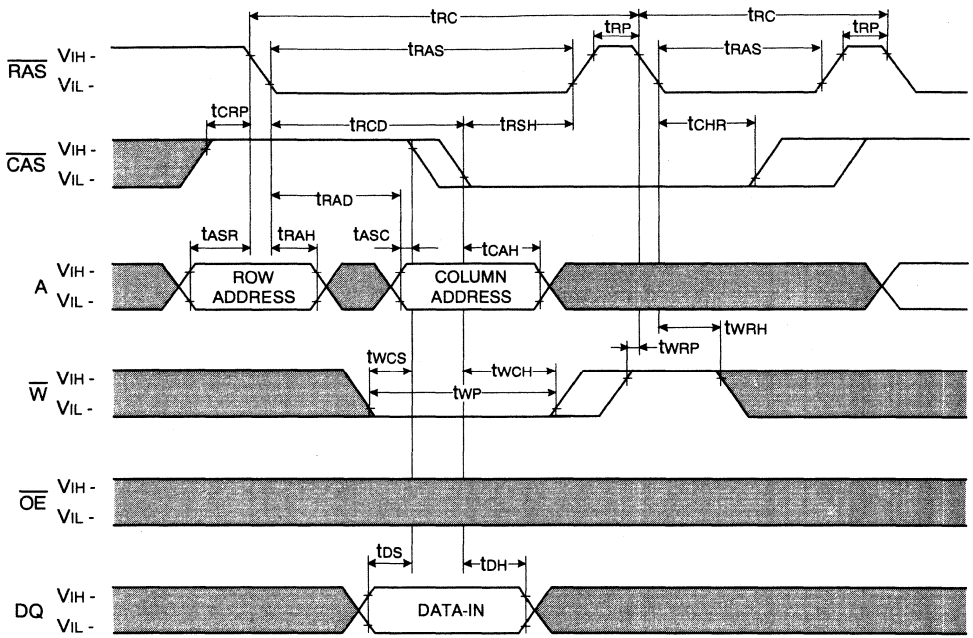
* In $\overline{RAS}$-only refresh cycle of 64Mb A-dile & B-die, when $\overline{CAS}$ signal transits from Low to High, the valid data may be cut off.

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN

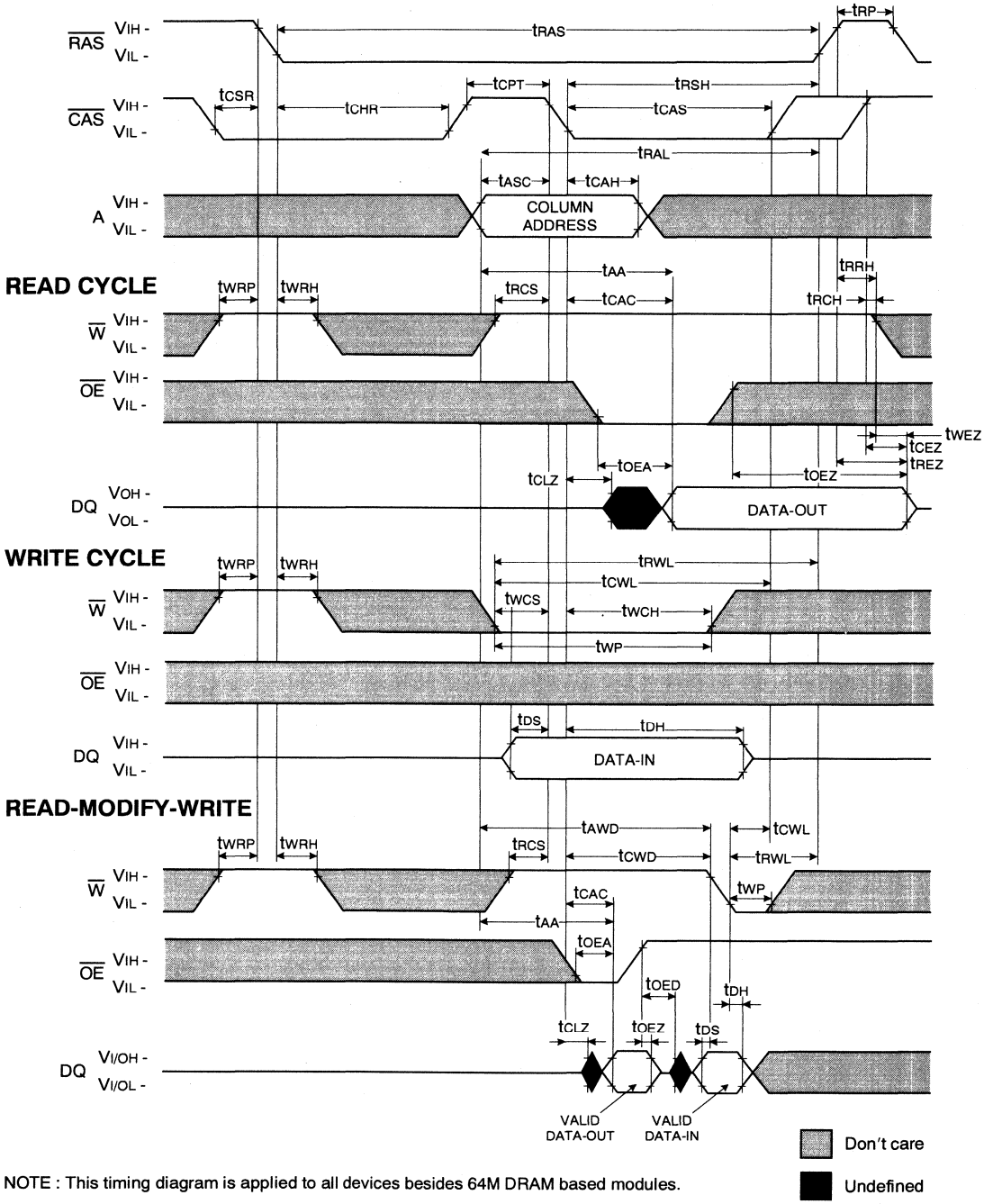


Don't care

Undefined

5

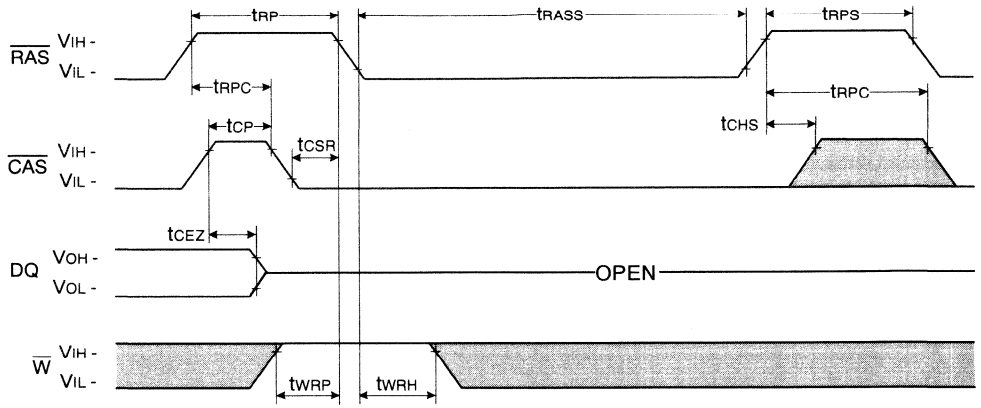
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

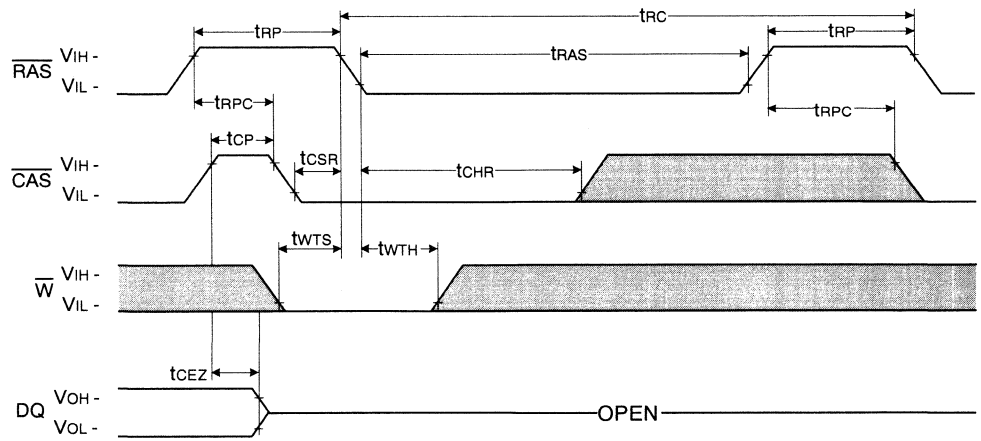
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't care



5

NOTES

SPD Information 6

Serial Presence Detect Specification

for FP/EDO DRAM

JEDEC Standard

June 1999

GENERAL DESCRIPTION

This Serial Presence Detect Specification describes the Presence Detects for Fast Page Mode DRAM and Extended Data Out(EDO) DRAM Modules. These PDs are those referenced in the SPD standard as "Specific Features". The following PD fields will occur, in the order presented, at the point in the standard where the Specific Features are referenced; that is after the identification of the Fundamental Memory Type and before identification of whether there is any Superset Features presented.

ADDRESS MAP

The following the SPD address map for FPM and EDO. It describes where the individual LUT-Entries/bytes will be held in the serial EEPROM;

Byte Number	Function Described	Notes
0	Defines # bytes written into serial memory at module mfgr	1
1	Total # bytes of SPD memory device	2
2	Fundamental memory type (FPM, EDO, SDRAM...) from appendix A	
3	# Row Address on this assembly	3
4	# Column Address on this assembly	3
5	# of DRAM Banks on this assembly	
6	Data Width of this assembly	
7	... Data Width Continuation	
8	Voltage interface standard of this assembly	
9	RAS # access time of this assembly	4
10	CAS # access time of this assembly	4
11	DIMM Configuration type (Non-parity, Parity, ECC)	
12	Refresh Rate/Type	4, 5
13	DRAM width, Primary DRAM	
14	Error Checking DRAM data width	
15 ~ 31	Reserved for future offerings	
32 ~ 61	Superset information (may be used in future)	
62	SPD data revision code	
63	Checksum for bytes 0 ~62	
64 ~ 127	Manufacturer's Information (Optional)	6
128+	Unused storage locations	

Notes :

1) This will be 128 bytes for FPM and EDO DRAM.
2) This will typically be 256 bytes.
3) High order bit defines if assembly has "redundant" addressing (if set to "1", highest order RAS# address must be re-sent as highest order CAS# address.)
4) From data sheet.
5) High order bit (MSB) is Self Refresh 'flag' : If bit seven is "1", assembly supports self refresh.
6) This is optional.
7) The unused Bytes are programed by FFh.

BYTE ASSIGNMENTS

BYTE 0 : From General SPD Standard, Number of Bytes used by module Manufacturer

This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data;

Number SPD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

BYTE 1 : From General SPD Standard, Total SPD Memory Size

This field describes the total size of the serial memory to hold the Serial Presence Detect data. The following lookup table describes serial memory densities (in bytes) along with the corresponding descriptor;

Serial Memory	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RFU	0	0	0	0	0	0	0	0
2 Bytes	0	0	0	0	0	0	0	1
4 Bytes	0	0	0	0	0	0	1	0
8 Bytes	0	0	0	0	0	0	1	1
16 Bytes	0	0	0	0	0	1	0	0
32 Bytes	0	0	0	0	0	1	0	1
64 Bytes	0	0	0	0	0	1	1	0
128 Bytes	0	0	0	0	0	1	1	1
256 Bytes	0	0	0	0	1	0	0	0
512 Bytes	0	0	0	0	1	0	0	1
1024 Bytes	0	0	0	0	1	0	1	0
2048 Bytes	0	0	0	0	1	0	1	1
4096 Bytes	0	0	0	0	1	1	0	0
8192 Bytes	0	0	0	0	1	1	0	1
16384 Bytes	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	1	1	1	1	1	1	1	0
.	1	1	1	1	1	1	1	1

BYTE 2 : From Appendix A, Memory Type

This byte describes the fundamental memory type (or technology) implemented on the module;

Fundamental Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	0	0	0	0	0	0	0	0
Standard FPM DRAM	0	0	0	0	0	0	0	1
EDO	0	0	0	0	0	0	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

BYTE 3 : Number of ROW Addresses

This first describes the number of ROW Address in the DRAM array;

No. of ROW Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1
Undefined	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
12(redundant)	1	0	0	0	1	1	0	0
13(redundant)	1	0	0	0	1	1	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
126(redundant)	1	1	1	1	1	1	1	0
127(redundant)	1	1	1	1	1	1	1	1

Bit 7 : "0" indicates normal addressing; "1" indicates redundant addressing

BYTE 4 : Number of COLUMN Addresses

This field describes the number of COLUMN Address in the DRAM array;

No. of COLUMN Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

BYTE 5 : Number of Banks

This field describes the number of banks on the DRAM module;

Number of Banks	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

BYTE 6 & 7 : Module Data Width

Byte 6 and 7 are used to designate the modules data width. The data width is presented as a 16 bit word; bit 0 of byte 6 becomes the LSB of the 16 bit width indentifier and bit 7 of byte 7 becomes the MSB. Consequently, if the module has a width of less than 255 bits or higher, byte 7 is used in conjunction with byte 6 to designate the total module width.

BYTE 6 : Module Data Width (0 ~ 255 bits)

Data Width	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
32	0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
64	0	1	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
72	0	1	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
144	1	0	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

BYTE 7 : Module Data Width Continued

This byte will be left at 00h if the original module data width is less than 256 bits wide. If the width is more than 255, then this byte will be used in conjunction with byte 6;

Module Data Width Cont.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0(+)	0	0	0	0	0	0	0	0
256(+)	0	0	0	0	0	0	0	1
512(+)	0	0	0	0	0	0	1	0
1024(+)	0	0	0	0	0	0	1	1
2048(+)	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

BYTE 8 : Module Interface Levels

This field describes the module's voltage;

Voltage Interface	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5.0 Volt/TTL	0	0	0	0	0	0	0	0
LVTTL	0	0	0	0	0	0	0	1
HSTL 1.5	0	0	0	0	0	0	1	0
SSTL 3.3	0	0	0	0	0	0	1	1
SSTL 2.5	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
New Table	1	1	1	1	1	1	1	1

BYTE 9 : RAS Access Time (tRAC)

This field describes the module's RAS Access Time;

RAS Access Time	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Undefined	0	0	0	0	0	0	0	0
1ns	0	0	0	0	0	0	0	1
2ns	0	0	0	0	0	0	1	0
3ns	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
50ns	0	0	1	1	0	0	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
60ns	0	0	1	1	1	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
70ns	0	1	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
80ns	0	1	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
254ns	1	1	1	1	1	1	1	0
255ns	1	1	1	1	1	1	1	1

BYTE 10 : CAS Access Time (tCAC)

This field describes the module's CAS Access Time;

CAS Access Time	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Undefined	0	0	0	0	0	0	0	0
1ns	0	0	0	0	0	0	0	1
2ns	0	0	0	0	0	0	1	0
3ns	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

10ns	0	0	0	0	1	0	1	0
11ns	0	0	0	0	1	0	1	1
12ns	0	0	0	0	1	1	0	0
13ns	0	0	0	0	1	1	0	1
14ns	0	0	0	0	1	1	1	0
15ns	0	0	0	0	1	1	1	1
16ns	0	0	0	1	0	0	0	0
17ns	0	0	0	1	0	0	0	1
18ns	0	0	0	1	0	0	1	0
19ns	0	0	0	1	0	0	1	1
20ns	0	0	0	1	0	1	0	0
21ns	0	0	0	1	0	1	0	1
22ns	0	0	0	1	0	1	1	0
23ns	0	0	0	1	0	1	1	1
24ns	0	0	0	1	0	0	0	0
25ns	0	0	0	1	0	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254ns	1	1	1	1	1	1	1	0
255ns	1	1	1	1	1	1	1	1

BYTE 11 : Module Configuration Type

This field describes the module's error detection or correction schemes;

Error Det./Cor.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
None	0	0	0	0	0	0	0	0
Parity	0	0	0	0	0	0	0	1
ECC	0	0	0	0	0	0	1	0
TBD	0	0	0	0	0	0	1	1
TBD	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	1	1

BYTE 12 : Refresh Rate/Type

This field describes the module's refresh rate and type;

Error Period	Bit7, Self Refresh Flag	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Normal (15.625us)	0	0	0	0	0	0	0	0
Reduced (.25x)...3.9us	0	0	0	0	0	0	0	1
Reduced (.5x)...7.8us	0	0	0	0	0	0	1	0
Extended (2x)...31.3us	0	0	0	0	0	0	1	1
Extended (4x)...62.5us	0	0	0	0	0	1	0	0
Extended (8x)...125us	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0

TBD	0	0	0	0	0	1	1	1
TBD	0	0	0	0	1	0	0	0
TBD	0	0	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
Self Refresh Entries								
Normal (15.625us)	1	0	0	0	0	0	0	0
Reduced (.25x)...3.9us	1	0	0	0	0	0	0	1
Reduced (.5x)...7.8us	1	0	0	0	0	0	1	0
Extended (2x)...31.3us	1	0	0	0	0	0	1	1
Extended (4x)...62.5us	1	0	0	0	0	1	0	0
Extended (8x)...125us	1	0	0	0	0	1	0	1
TBD	1	0	0	0	0	1	1	0
TBD	.	.	.	.	.	.	.	.
TBD	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	1	0
TBD	1	1	1	1	1	1	1	1

BYTE 13 : DRAM Width, Primary DRAM

This field describes the width of the primary DRAMs used on the module. The primary DRAM is that which is used for data; examples of primary(data) DRAM widths are x4, x8, x16, x32. The primary DRAMs used may incorporate data and error checking e.g. x9, x18, x36.

DRAM Width Primary DRAM	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
15	0	0	0	0	1	1	1	1
16	0	0	0	1	0	0	0	0
17	0	0	0	1	0	0	0	1
18	0	0	0	1	0	0	1	0
.	.	.	.	.	.	.	.	.
32	0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
255	1	1	1	1	1	1	1	1

BYTE 14 : Error Checking DRAM data width

If the module incorporates error checking and if the primary data DRAM does not include these bits; i.e. there are separate error checking DRAM's width is expressed in this byte. Examples of error checking DRAM widths include x1, x4, x8.

DRAM Width Error Checking DRAM	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
255	1	1	1	1	1	1	1	1

BYTE 15~31 : Reserved for future offerings

BYTE 32~61 : Superset Information (may be used in future)

These fields are reserved for superset information. Currently, these fields are programmed by "00h" because the standardization for these fields are not fixed yet.

BYTE 62 : SPD data revision code

This field identifies the DRAM DIMM SPD data revision to which the module conforms. Currently, this field is programmed by "00h".

SPD data revision code	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Initial code	0	0	0	0	0	0	0	0
Rev. 1	0	0	0	0	0	0	0	1
Rev. 2	0	0	0	0	0	0	1	0
Rev. 3	0	0	0	0	0	0	1	1
Rev. 4	0	0	0	0	0	1	0	0
Rev. 5	0	0	0	0	0	1	0	1
-	-	-	-	-	-	-	-	-

BYTE 63 : Checksum for bytes 0~62

This field is checksum for bytes 0 through 62. For details, refer to the SPD specifications of each module.

BYTES 64~127 : Manufacturer's Information (optional)

This field describes manufacturer's information is optional.

BYTE 64~71 : Manufacturer's JEDEC ID code per EIA/JEP106-E

This field describes the manufacturer's JEDEC ID code per EIA/JEP106-E;

Byte	64	65	66	67	68	69	70	71
code	CEh	00h	00h	00h	00h	00h	00h	00h

BYTE 72 : Manufacturer's Location

This field describes the manufacturer's location;

Location	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Kihung Korea	0	0	0	0	0	0	0	0
Onyang Korea	0	0	0	0	0	0	0	1
TBD	.	.	.	.	.	.	.	.

BYTE 73~90 : Manufacturer's Part Number (ASCII code)

This field describes the manufacturer's Part Number;

BYTE 73 : Samsung Memory (ASCII code)

Samsung Korea	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
K	0	1	0	0	1	0	1	1
TBD	.	.	.	.	.	.	.	.

BYTE 74 : Samsung Memory (ASCII code)

Samsung Korea	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
M	0	1	0	0	1	1	0	1
TBD	.	.	.	.	.	.	.	.

BYTE 75 : Module (ASCII code)

Module	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
M	0	1	0	0	1	1	0	1
TBD	.	.	.	.	.	.	.	.

BYTE 76 : Memory Type & Edge Connector (ASCII code)

Memory Type	Code	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FLASH	1	0	0	1	1	0	0	0	1
Mask ROM	2	0	0	1	1	0	0	1	0
DRAM DIMM	3	0	0	1	1	0	0	1	1
DRAM 8B SODIMM	4	0	0	1	1	0	0	0	0
Old JEDEC DRAM SIMM	5	0	0	1	1	0	1	0	1
SRAM	6	0	0	1	1	0	1	1	0
Reserved	7	0	0	1	1	0	1	1	1
Reserved	8	0	0	1	1	1	0	0	0
VRAM	9	0	0	1	1	1	0	0	1
TBD	.	.	.	.	.	.	.	.	.

BYTE 77~79 : Data bit (ASCII code)

Data bit	Byte 77	Byte 78	Byte 79
x8	7Fh	7Fh	38h
x9	7Fh	7Fh	39h
x32	7Fh	33h	32h
x36	7Fh	33h	36h
x64	7Fh	36h	34h
x72	7Fh	37h	32h
x66	7Fh	36h	36h
x74	7Fh	37h	34h
x144	31h	34h	34h
TBD	.	.	.

BYTE 80 : Mode/Feature & Process & Operating Voltage (ASCII code)

Mode & Voltage	Code	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
F/P 5V	C	0	1	0	0	0	0	1	1
F/P 3.3V	V	0	1	0	1	0	1	1	0
EDO 5V	E	0	1	0	0	0	1	0	1
EDO 3.3V	F	0	1	0	0	0	1	1	0
Window RAM 5V	W	0	1	0	1	0	1	1	1
Sync. 3.3V	S	0	1	0	1	0	0	1	1
Sync. Graphic 3.3V	G	0	1	0	0	0	1	1	1
TBD	.	.	.	.	.	.	.	.	

BYTE 81~82 : Density (ASCII code)

Data bit	Byte 81	Byte 82
1M	7Fh	31h
2M	7Fh	32h
4M	7Fh	34h
8M	7Fh	38h
16M	31h	36h
32M	33h	32h
TBD	.	.

BYTE 83 : Refresh (ASCII code)

Refresh	Code	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4K Refresh	0	0	0	1	1	0	0	0	0
1K Refresh	2	0	0	1	1	0	0	1	0
2K Refresh	1	0	0	1	1	0	0	0	1
8K Refresh	8	0	0	1	1	1	0	0	0
TBD	.	.	.	.	.	.	.	.	

BYTE 84 : Composition Component (ASCII code)

Composition	Code	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
x4	0	0	0	1	1	0	0	0	0
x4 + x1	1	0	0	1	1	0	0	0	1
x4 + Quad CAS	2	0	0	1	1	0	0	1	0
x8	3	0	0	1	1	0	0	1	1
x16	4	0	0	1	1	0	1	0	0
x16 + Quad CAS	5	0	0	1	1	0	1	0	1
TBD	.	.	.	.	.	.	.	.	.

BYTE 85 : Component Revision (ASCII code)

Component Revision	Code	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
None	Blank	0	1	1	1	1	1	1	1
First Rev.	A	0	1	0	0	0	0	0	1
Second Rev.	B	0	1	0	0	0	0	1	0
Third Rev.	C	0	1	0	0	0	0	1	1
TBD	.	.	.	.	.	.	.	.	.

BYTE 86 : Package Type (ASCII code)

Package Type	Code	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SOJ first	J	0	1	0	0	1	0	1	0
SOJ second	K	0	1	0	0	1	0	1	1
TSOP first	T	0	1	0	1	0	1	0	0
TSOP second	S	0	1	0	1	0	0	1	1
TSOJ first	Y	0	1	0	1	1	0	0	1
TSOJ second	X	0	1	0	1	1	0	0	0
TBD	.	.	.	.	.	.	.	.	.

BYTE 87 : PCB Revision (ASCII code)

PCB Revision	Code	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
None	Blank	0	1	1	1	1	1	1	1
First Rev.	1	0	0	1	1	0	0	0	1
Second Rev.	2	0	0	1	1	0	0	1	0
Third Rev.	3	0	0	1	1	0	0	1	1
TBD	.	.	.	.	.	.	.	.	.

BYTE 88 : Hyphen (ASCII code)

PCB Revision	Code	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
"-"	-	0	0	1	0	1	1	0	1

BYTE 89 : Power (ASCII code)

Power	Code	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Normal	Blank	0	1	1	1	1	1	1	1
Low power & Self refresh	L	0	1	0	0	1	1	0	0
Super Low power	H	0	1	0	0	1	0	0	0
Self refresh only	G	0	1	0	0	0	1	1	1
TBD	.	.	.	.	.	.	.	.	.

BYTE 90 : Speed (ASCII code)

Speed	Code	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
70ns	7	0	0	1	1	0	1	1	1
60ns	6	0	0	1	1	0	1	1	0
50ns	5	0	0	1	1	0	1	0	1
TBD	.	.	.	.	.	.	.	.	.

BYTE 91 : Manufacturer's Revision

This field describes the manufacturer's revision history which is described in manufacturer's P/N as well;

Manufacturer's Revision	Code	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
None	Blank	0	1	1	1	1	1	1	1
First Rev.	1	0	0	1	1	0	0	0	1
Second Rev.	2	0	0	1	1	0	0	1	0
Third Rev.	3	0	0	1	1	0	0	1	1
TBD	.	.	.	.	.	.	.	.	.

BYTE 92 : Reserved for Manufacturer's Revision

BYTE 93 : Manufacturer Date Week (Binary)

This field describes the manufacturer Date Week;

Manufacturer's Revision	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
First Rev.	0	0	0	0	0	0	0	1
Second Rev.	0	0	0	0	0	0	0	0
Third Rev.	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
52nd week	0	0	1	1	0	1	0	0
53rd week	0	0	1	1	0	1	0	1

BYTE 94 : Manufacturer Date Year (Binary)

This field describes the manufacturer Date Year;

Date Week	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
'95	0	1	0	1	1	1	1	1
'96	0	1	1	0	0	0	0	0
'97	0	1	1	0	0	0	0	1
.	.	.	.	.	.	.	.	.
'00	0	0	0	0	0	0	0	0
'01	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.
'94	0	1	0	1	1	1	1	1

BYTE 95~98 : Assembly Serial

This field describes Assembly Serial #.

BYTE 99~127 : Manufacturer Specific Data Area (may be used in future)

BYTE 128~255 : Unused Storage Locations (may be used in future)

Introduction

New memory technologies are continually being introduced to the industry. As these new technologies are considered, the need for expansion modules becomes evident : consequently, new memory technologies are being incorporated onto existing module from factors. Unfortunately, upon a module's first implementation, the module designer is often unable to predict all of the (as yet unreleased) memory technologies which would eventually be used on the module from factor; hence the Parallel Presence Detect (PPD) method did not allow for these newer technologies. Given that memory modules do not regularly change from factor when a new memory technology is implemented, a Serial Presence Detect (SPD) method should be available and predefined so that it can be considered for new memory modules when needed.

1.0 Scope

This standard defines the means to implement a Presence Detect (PD) scheme serially. This Serial Presence Detect (SPD) standard is intended for use on any memory module independent of memory technology or module from factor. At the point of standardization of any given memory module, SPD being defined within this standard, may be easily implemented if so chosen. The body of this standard will depict generally how SPD is implemented; this will be independent of the module's memory technology. When a specific memory technology is being depicted (e.g. Fast Page DRAM), an appendix to this standard will be added describing the characteristics, features and attributes of that memory technology needed for Presence Detection. The entire address map of the SPD scheme must be presented in each appendix. When a module implementing SPD is standardized, the (proposed) standard for that module must also include the following information pertinent to the SPD:

- SPD interface protocol (see section 2 herein)
- Acceptable module configurations,
- Legitimate architectures : depth, width, #banks, addressing
- Acceptable error checking schemes (ECC, Parity...)
- SPD writing diagram and pinout to module.

2.0 Interface Protocol

Upon the development/standardization of a new module form factor incorporating SPD, the SPD interface protocol will be defined. As long as that module form factor is used, this protocol must remain constant. Example of SPD interface protocol IIC, Microwire, etc. The physical implementation (pinouts etc.) must also be defined in the standard for the module form factor if it implements SPD.

3.0 Data Order and PD size

This document will present the order in which the PD bytes should follow. It also defines how many bytes must be used to define a given PD; in most cases it will be one byte per PD. The SPD address map is fixed upon selection of any given fundamental technology, this includes all required, optional, and superset data; when a fundamental memory technologies PD bits are defined, then the entire address map for those SPDs must also be defined.

4.0 Scope

SPD data is stored in a non-volatile memory device. The different types of data include, but are not limited to :

- Look Up Table entries
- Binary data
- Optional data (Binary or ASCII data)

4.1 Look Up Table (LUT) Entries

Much of the SPD data is organized as series of table entries. Each table entry contains one or more bytes of information. Each table entry represents one particular characteristics pertinent to the memory module; e.g. fast page mode DRAM will have specific tables for tRAC, tCAC, # of banks, number of row address, number of column address, error detection/correction, refresh rates, data width, and interface standard. Each table entry corresponds to a position on a look-up-table specified within an appendix within this standard. The number of bytes (one or more) needed to express a particular aspect of the module is fixed and defined in this standard or in one of its appendices.

4.2 Optional Data

At the module supplier's discretion, certain optional data may be added to the serial memory. Data which may be added includes manufacturer electronic ID, manufacturer's module serial numbers, and other ASCII or binary data. The optional data which is specifically represented is described fully in section 5 herein.

5.0 SPD Content

The Serial Presence Detect standard calls for various features and items to be defined. Specifically, the following must be addressed in any SPD implementation;

Description	Data Type	Byte Number/Address Map
SPD size	LUT Entry	0
Total SPD memory type	LUT Entry	1
Fundamental memory type	LUT Entry, Appendix A	2
Definition of features specific to the Fundamental memory	See pertinent appendix	See pertinent Fundamental Technology Appendix
(Optional) Superset memory type	See appendix B	See pertinent Fundamental Technology Appendix
(Optional) Definition of features specific to the superset memory	See pertinent appendix	See pertinent Fundamental Technology Appendix
(Optional) Additional ASCII or Binary data	See pertinent appendix	See pertinent Fundamental Technology Appendix

Detailed descriptions follow in paragraphs 4.x

5.1 Byte 0, Number of Bytes used by Module Manufacturer

This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data. The maximum amount of data is consequently 255 bytes.

5.2 Byte 1, Total SPD Memory Size

This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor

5.3 Byte 2, Fundamental Memory Type

This field identifies the total size of the serial memory. The fundamental type of memory may include Fast Page Mode DRAM, EDO DRAM, Masked ROM, EEPROM, Synchronous DRAM, etc. The table listing all the types of Fundamental memory is contained in appendix A herein. New fundamental types can be added to this table anytime after standardization of a fundamental memory type. Note that if a given new technology is completely backward compatible with pre-existing technology, than it should be considered a Superset technology and described as such as detailed within this standard.

5.4 Byte TBD (specific number of bytes address map defined in appendix detailing fundamental technology), Descriptions of Modules Specific Feature

Appendices to this standard detail the tables for the features specific to each of the fundamental memory types as described above. For example, see appendix C for details of SPD features for Fast Page Mode and Extended Data Out DRAM Modules.

5.5 Byte TBD (specific number of bytes and address map defined in appendix detailing fundamental technology), Superset Features

When a new technology is developed which is completely backward compatible to an already specified (fundamental) technology, then it may be considered a 'Superset' technology. The benefits of specifying a technology as a superset are obvious; if a system is capable so pirating in a 'fundamental' mode only and a superset type or technology is as specified in appendix B to this standard. Appendix B will previous the decode of specific superset technologies. It will reference other appendices where the specific PDs are further detailed. As new superset technology are specified just as for any given fundamental technology except that any and all fundamental technologies must be referenced.

5.6 Byte TBD (specific number of bytes and address map defined in appendix detailing fundamental technology), Miscellaneous ASCII or Binary Data

Module manufacturers may at their option include their own ASCII or Binary data within the SPD serial memory. The ASCII or Binary data incorporated by the manufacturer is not defined by this standard; the data presented is entirely up to the supplier to define and use.

APPENDIX A : Table(s) of Fundamental Memory Types:

This table is modified/appended whenever a new fundamental memory technology is to be added to the Serial Presence Detect (SPD) standard. When a new memory type is added to this standard, a new appendix must also be added which details the specific features pertinent to the new fundamental type. The following table details the fundamental memory types.

This fundamental memory types are identified as follows;

Fundamental Mem. Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	See Appendix
Reserved	0	0	0	0	0	0	0	0	N/A
Standard FPM DRAM	0	0	0	0	0	0	0	1	C
EDO	0	0	0	0	0	0	1	0	C
PNEDO	0	0	0	0	0	0	1	1	TBD
Sync. DRAM	0	0	0	0	0	1	0	0	E
TBD	0	0	0	0	0	1	0	1	TBD
TBD	0	0	0	0	0	1	1	0	TBD
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	0	1	TBD
TBD	1	1	1	1	1	1	1	0	TBD
TBD	1	1	1	1	1	1	1	1	TBD

APPENDIX B : Superset Technologies...

There are no Superset Technologies specified at this time.

SERIAL PRESENCE DETECT INFORMATION*1

- Serial PD interface Protocol : I^2C
- Current sink capability of SDA driver≤3mA
- Maximum clock frequency : 80KHz
- Contents :

Byte Number	Function described	Function supported	Hex Value
0	Number of bytes used by Module Manufacturer	128bytes	80h
1	Total SPD memory size	256bytes (2K-bit)	08h
2	Memory type	EDO	02h
3	Number of ROW Addresses	10 (1K ref.)	0Ah
		12 (4K ref.)	0Ch
4	Number of COULMN Addresses	10 (1K ref.)	0Ah
		8 (4K ref.)	08h
5	Number of Banks	1	01h
6	Module Data Width	64bits	40h
7	Module Data Width (Continued)	0(+)	00h
8	Module Interface Levels	LVTTL	01h
9	RAS Access Time (t_{RAC})	50ns (-5)	32h
		60ns (-6)	3Ch
10	CAS Access Time (t_{CAC})	15ns (-5)	0Fh
		17ns (-6)	11h
11	Module Configuration Type	None	00h
12	Refresh Rate/Type	1K : Extended (8x) -- 125us	85h
		4K : Extended (2x) -- 31.3us	83h
13	DRAM width, Primary DRAM	x16	10h
14	ERROR Checking DRAM data width	Undefined	00h
15~61*4	Undefined	Undefined	FFh
62	SPD data revision code	Rev. 1.0	01h
63*5	Checksum for bytes 0~62	Refer to note * 5	
64	Manufacturer's JEDEC ID code	Samsung	CEh
65~71	Manufacturer's JEDEC ID code	Samsung	00h
72	Manufacturer's location	Onyang Korea	01h
73	Manufacturer's Part Number	K	4Bh
74		M	4Dh
75		M	4Dh
76		4	34h
77		66	7Fh
78			36h
79			36h

SERIAL PRESENCE DETECT INFORMATION(continued)

Byte Number	Function described	Function supported	Hex Value
80	Manufacturer's Part Number	F	46h
81		1	7Fh
82			31h
83		0	30h
		2	32h
84		4	34h
85		C	43h
86		T	54h
87		1	31h
88		Hyphen	2Dh
89		L	4Ch
90		5	35h
		6	36h
91	Manufacturer's Revision	1	31h
92*4		Undefined	FFh
93*2	Manufacturer Date Week	Refer to note * 2	
94*2	Manufacturer Date Year	Refer to note * 2	
95~98*3	Assembly Serial #	Refer to note * 3	
99~127*4	Manufacturer Specific Data Area	Undefined	FFh
128~*4	Undefined	Undefined	FFh

* 1 : Above data are based on the SPD specification of JEDEC standard
* 2 : These bytes are programmed by code of Date Week & Date Year.
* 3 : These bytes are programmed by Samsung's own Assembly Serial # system.
* 4 : All undefined bytes will be programmed by "FFh".
* 5 : Checksum for bytes 0~62 :

Row / Column Address	$\overline{RAS}$ / $\overline{CAS}$ Access Time	Ref. rate	Checksum
10 / 10	50 / 15	125us	88h
		31.3us	86h
	60 / 17	125us	94h
		31.3us	92h
12 / 8	50 / 15	125us	88h
		31.3us	86h
	60 / 17	125us	94h
		31.3us	92h

SERIAL PRESENCE DETECT INFORMATION*1

- Serial PD interface Protocol : I^2C
- Current sink capability of SDA driver≤3mA
- Maximum clock frequency : 80KHz
- Contents :

Byte Number	Function described	Function supported	Hex Value
0	Number of bytes used by Module Manufacturer	128bytes	80h
1	Total SPD memory size	256bytes (2K-bit)	08h
2	Memory type	EDO	02h
3	Number of ROW Addresses	11(2K ref.)	0Bh
		12(4K ref.)	0Ch
4	Number of COULMN Addresses	10(2K ref.)	0Ah
		9(4K ref.)	09h
5	Number of Banks	1	01h
6	Module Data Width	64bits	40h
7	Module Data Width (Continued)	0(+)	00h
8	Module Interface Levels	LVTTL	01h
9	RAS Access Time (t_{RAC})	50ns (-5)	32h
		60ns (-6)	3Ch
10	CAS Access Time (t_{CAC})	13ns (-5)	0Dh
		15ns (-6)	0Fh
11	Module Configuration Type	None	00h
12	Refresh Rate/Type	2K : Extended(4x) -- 62.5us	84h
		4K : Extended(2x) -- 31.3us	83h
13	DRAM width, Primary DRAM	x8	08h
14	ERROR Checking DRAM data width	Undefined	00h
15~61*4	Undefined	Undefined	FFh
62	SPD data revision code	Rev. 1.0	01h
63*5	Checksum for bytes 0~62	Refer to note * 5	
64	Manufacturer's JEDEC ID code	Samsung	CEh
65~71	Manufacturer's JEDEC ID code	Samsung	00h
72	Manufacturer's location	Onyang Korea	01h
73	Manufacturer's Part Number	K	4Bh
74		M	4Dh
75		M	4Dh
76		4	34h
77		66	7Fh
78			36h
79			36h

SERIAL PRESENCE DETECT INFORMATION(continued)

Byte Number	Function described	Function supported	Hex Value
80	Manufacturer's Part Number	F	46h
81		2	7Fh
82			32h
83		0	30h
		1	31h
84		3	33h
85		C	43h
86		S	53h
87		2	32h
88		Hyphen	2Dh
89		L	4Ch
90		5	35h
		6	36h
91	Manufacturer's Revision	2	32h
92*4		Undefined	FFh
93*2	Manufacturer Date Week	Refer to note * 2	
94*2	Manufacturer Date Year	Refer to note * 2	
95~98*3	Assembly Serial#	Refer to note * 3	
99~127*4	Manufacturer Specific Data Area	Undefined	FFh
128~*4	Undefined	Undefined	FFh

* 1 : Above data are based on the SPD specification of JEDEC standard
* 2 : These bytes are programmed by code of Date Week & Date Year.
* 3 : These bytes are programmed by Samsung's own Assembly Serial # system.
* 4 : All undefined bytes will be programmed by "FFh".
* 5 : Checksum for bytes 0~62 :

Row / Column Address	$\overline{RAS}$ / $\overline{CAS}$ Access Time	Ref. rate	Checksum
11 / 10	50 / 13	62.5us	7Eh
		31.3us	7Dh
	60 / 15	62.5us	8Ah
		31.3us	89h
12 / 9	50 / 13	62.5us	7Eh
		31.3us	7Dh
	60 / 15	62.5us	8Ah
		31.3us	89h

SERIAL PRESENCE DETECT INFORMATION*1

- Serial PD interface Protocol : I^2C
- Current sink capability of SDA driver≤3mA
- Maximum clock frequency : 80KHz
- Contents :

Byte Number	Function described	Function supported	Hex Value
0	Number of bytes used by Module Manufacturer	128bytes	80h
1	Total SPD memory size	256bytes (2K-bit)	08h
2	Memory type	EDO	02h
3	Number of ROW Addresses	12 (4K ref.)	0Ch
4	Number of COULMN Addresses	10 (4K ref.)	0Ah
5	Number of Banks	1	01h
6	Module Data Width	64bits	40h
7	Module Data Width (Continued)	0(+)	00h
8	Module Interface Levels	LVTTL	01h
9	RAS Access Time (tRAC)	50ns (-5)	32h
		60ns (-6)	3Ch
10	CAS Access Time (tCAC)	13ns (-5)	0Dh
		15ns (-6)	0Fh
11	Module Configuration Type	None	00h
12	Refresh Rate/Type	Extened(2x)--31.3us	83h
13	DRAM width, Primary DRAM	x16	10h
14	ERROR Checking DRAM data width	Undefined	00h
15~61*4	Undefined	Undefined	FFh
62	SPD data revision code	Rev. 1.0	01h
63*5	Checksum for bytes 0~62	Refer to note * 5	
64	Manufacturer's JEDEC ID code	Samsung	CEh
65~71	Manufacturer's JEDEC ID code	Samsung	00h
72	Manufacturer's location	Onyang Korea	01h
73	Manufacturer's Part Number	K	4Bh
74		M	4Dh
75		M	4Dh
76		4	34h
77		66	7Fh
78			36h
79			36h
80		F	46h
81		4	7Fh
82			34h

SERIAL PRESENCE DETECT INFORMATION(continued)

Byte Number	Function described	Function supported	Hex Value
83	Manufacturer's Part Number(continued)	0	30h
84		4	34h
85		C	43h
86		S	53h
87		2	32h
88		Hyphen	2Dh
89		L	4Ch
90		5	35h
		6	36h
91	Manufacturer's Revision	2	32h
92*4		Undefined	FFh
93*2	Manufacturer Date Week	Refer to note * 2	
94*2	Manufacturer Date Year	Refer to note * 2	
95~98*3	Assembly Serial #	Refer to note * 3	
99~127*4	Manufacturer Specific Data Area	Undefined	FFh
128~*4	Undefined	Undefined	FFh

* 1 : Above data are based on the SPD specification of JEDEC standard
* 2 : These bytes are programmed by binary code of Date Week or Year.
* 3 : These bytes are programmed by Samsung's own Assembly Serial # system.
* 4 : All undefined bytes will be programmed by "FFh".
* 5 : Checksum for bytes 0 ~ 62

6

Row / Column Address	$\overline{RAS}$ / $\overline{CAS}$ Access Time	Ref. rate	Checksum
12 / 10	50 / 13	31.3us	86h
	60 / 15		92h

SERIAL PRESENCE DETECT INFORMATION*1

- Serial PD interface Protocol : I^2C
- Current sink capability of SDA driver≤3mA
- Maximum clock frequency : 80KHz
- Contents :

Byte Number	Function described	Function supported	Hex Value
0	Number of bytes used by Module Manufacturer	128bytes	80h
1	Total SPD memory size	256bytes (2K-bit)	08h
2	Memory type	EDO	02h
3	Number of ROW Addresses	12 (4K ref.)	0Ch
4	Number of COULMN Addresses	11 (4K ref.)	0Bh
5	Number of Banks	1	01h
6	Module Data Width	64bits	40h
7	Module Data Width (Continued)	0(+)	00h
8	Module Interface Levels	LVTTL	01h
9	RAS Access Time (tRAC)	50ns (-5)	32h
		60ns (-6)	3Ch
10	CAS Access Time (tCAC)	13ns (-5)	0Dh
		15ns (-6)	0Fh
11	Module Configuration Type	None	00h
12	Refresh Rate/Type	Extened(2x)--31.3us	83h
13	DRAM width, Primary DRAM	x8	08h
14	ERROR Checking DRAM data width	Undefined	00h
15~61*4	Undefined	Undefined	FFh
62	SPD data revision code	Rev. 1.0	01h
63*5	Checksum for bytes 0~62	Refer to note * 5	
64	Manufacturer's JEDEC ID code	Samsung	CEh
65~71	Manufacturer's JEDEC ID code	Samsung	00h
72	Manufacturer's location	Onyang Korea	01h
73	Manufacturer's Part Number	K	4Bh
74		M	4Dh
75		M	4Dh
76		4	34h
77		66	7Fh
78			36h
79			36h
80		F	46h
81		8	7Fh
82			38h

SERIAL PRESENCE DETECT INFORMATION(continued)

Byte Number	Function described	Function supported	Hex Value
83	Manufacturer's Part Number(continued)	0	30h
84		3	33h
85		C	43h
86		S	53h
87		2	32h
88		Hyphen	2Dh
89		L	4Ch
90		5	35h
		6	36h
91	Manufacturer's Revision	2	32h
92*4		Undefined	FFh
93*2	Manufacturer Date Week	Refer to note * 2	
94*2	Manufacturer Date Year	Refer to note * 2	
95~98*3	Assembly Serial #	Refer to note * 3	
99~127*4	Manufacturer Specific Data Area	Undefined	FFh
128~*4	Undefined	Undefined	FFh

* 1 : Above data are based on the SPD specification of JEDEC standard
* 2 : These bytes are programmed by binary code of Date Week or Year.
* 3 : These bytes are programmed by Samsung's own Assembly Serial # system.
* 4 : All undefined bytes will be programmed by "FFh".
* 5 : Checksum for bytes 0 ~ 62.

6

Row / Column Address	$\overline{RAS}$ / $\overline{CAS}$ Access Time	Ref. rate	Checksum
12 / 11	50 / 13	31.3us	7Fh
	60 / 15		8Bh

SERIAL PRESENCE DETECT INFORMATION*1

- Serial PD interface Protocol : I^2C
- Current sink capability of SDA driver≤3mA
- Maximum clock frequency : 80KHz
- Contents :

Byte Number	Function described	Function supported	Hex Value
0	Number of bytes used by Module Manufacturer	128bytes	80h
1	Total SPD memory size	256bytes (2K-bit)	08h
2	Memory type	EDO	02h
3	Number of ROW Addresses	12 (4K ref.)	0Ch
4	Number of COULMN Addresses	11 (4K ref.)	0Bh
5	Number of Banks	1	01h
6	Module Data Width	64bits	40h
7	Module Data Width (Continued)	0(+)	00h
8	Module Interface Levels	LVTTL	01h
9	RAS Access Time (tRAC)	50ns (-5)	32h
		60ns (-6)	3Ch
10	CAS Access Time (tCAC)	13ns (-5)	0Dh
		15ns (-6)	0Fh
11	Module Configuration Type	None	00h
12	Refresh Rate/Type	Extened(2x)--31.3us	83h
13	DRAM width, Primary DRAM	x8	08h
14	ERROR Checking DRAM data width	Undefined	00h
15~61*4	Undefined	Undefined	FFh
62	SPD data revision code	Rev. 1.0	01h
63*5	Checksum for bytes 0~62	Refer to note * 5	
64	Manufacturer's JEDEC ID code	Samsung	CEh
65~71	Manufacturer's JEDEC ID code	Samsung	00h
72	Manufacturer's location	Onyang Korea	01h
73	Manufacturer's Part Number	K	4Bh
74		M	4Dh
75		M	4Dh
76		4	34h
77		66	7Fh
78			36h
79			36h
80		F	46h
81		8	7Fh
82			38h

SERIAL PRESENCE DETECT INFORMATION(continued)

Byte Number	Function described	Function supported	Hex Value
83	Manufacturer's Part Number(continued)	0	30h
84		3	33h
85		C	43h
86		S	53h
87		3	33h
88		Hyphen	2Dh
89		L	4Ch
90		5	35h
		6	36h
91	Manufacturer's Revision	3	33h
92*4		Undefined	FFh
93*2	Manufacturer Date Week	Refer to note * 2	
94*2	Manufacturer Date Year	Refer to note * 2	
95~98*3	Assembly Serial #	Refer to note * 3	
99~127*4	Manufacturer Specific Data Area	Undefined	FFh
128~*4	Undefined	Undefined	FFh

* 1 : Above data are based on the SPD specification of JEDEC standard
* 2 : These bytes are programmed by binary code of Date Week or Year.
* 3 : These bytes are programmed by Samsung's own Assembly Serial # system.
* 4 : All undefined bytes will be programmed by "FFh".
* 5 : Checksum for bytes 0 ~ 62.

6

Row / Column Address	$\overline{RAS}$ / $\overline{CAS}$ Access Time	Ref. rate	Checksum
12 / 11	50 / 13	31.3us	7Fh
	60 / 15		8Bh

SERIAL PRESENCE DETECT INFORMATION*1

- Serial PD interface Protocol : I^2C
- Current sink capability of SDA driver≤3mA
- Maximum clock frequency : 80KHz
- Contents :

Byte Number	Function described	Function supported	Hex Value
0	Number of bytes used by Module Manufacturer	128bytes	80h
1	Total SPD memory size	256bytes (2K-bit)	08h
2	Memory type	EDO	02h
3	Number of ROW Addresses	12 (4K ref.)	0Ch
4	Number of COULMN Addresses	10 (4K ref.)	0Ah
5	Number of Banks	2	02h
6	Module Data Width	64bits	40h
7	Module Data Width (Continued)	0(+)	00h
8	Module Interface Levels	LVTTL	01h
9	RAS Access Time (t_{RAC})	50ns (-5)	32h
		60ns (-6)	3Ch
10	CAS Access Time (t_{CAC})	13ns (-5)	0Dh
		15ns (-6)	0Fh
11	Module Configuration Type	None	00h
12	Refresh Rate/Type	Extened(2x)--31.3us	83h
13	DRAM width, Primary DRAM	x16	10h
14	ERROR Checking DRAM data width	Undefined	00h
15~61*4	Undefined	Undefined	FFh
62	SPD data revision code	Rev. 1.0	01h
63*5	Checksum for bytes 0~62	Refer to note * 5	
64	Manufacturer's JEDEC ID code	Samsung	CEh
65~71	Manufacturer's JEDEC ID code	Samsung	00h
72	Manufacturer's location	Onyang Korea	01h
73	Manufacturer's Part Number	K	4Bh
74		M	4Dh
75		M	4Dh
76		4	34h
77		66	7Fh
78			36h
79			36h
80		F	46h
81		8	7Fh
82			38h

SERIAL PRESENCE DETECT INFORMATION(continued)

Byte Number	Function described	Function supported	Hex Value
83	Manufacturer's Part Number(continued)	0	30h
84		4	34h
85		C	43h
86		S	53h
87		1	31h
88		Hyphen	2Dh
89		L	4Ch
90		5	35h
		6	36h
91	Manufacturer's Revision	1	31h
92*4		Undefined	FFh
93*2	Manufacturer Date Week	Refer to note * 2	
94*2	Manufacturer Date Year	Refer to note * 2	
95~98*3	Assembly Serial #	Refer to note * 3	
99~127*4	Manufacturer Specific Data Area	Undefined	FFh
128~*4	Undefined	Undefined	FFh

* 1 : Above data are based on the SPD specification of JEDEC standard
* 2 : These bytes are programmed by binary code of Date Week or Year.
* 3 : These bytes are programmed by Samsung's own Assembly Serial # system.
* 4 : All undefined bytes will be programmed by "FFh".
* 5 : Checksum for bytes 0 ~ 62

Row / Column Address	$\overline{RAS}$ / $\overline{CAS}$ Access Time	Ref. rate	Checksum
12 / 11	50 / 13	31.3us	87h
	60 / 15		93h

SERIAL PRESENCE DETECT INFORMATION*1

- Serial PD interface Protocol : I^2C
- Current sink capability of SDA driver≤3mA
- Maximum clock frequency : 80KHz
- Contents :

Byte Number	Function described	Function supported	Hex Value
0	Number of bytes used by Module Manufacturer	128bytes	80h
1	Total SPD memory size	256bytes (2K-bit)	08h
2	Memory type	EDO	02h
3	Number of ROW Addresses	10 (1K ref.)	0Ah
4	Number of COULMN Addresses	10 (1K ref.)	0Ah
5	Number of Banks	1	01h
6	Module Data Width	64bits	40h
7	Module Data Width (Continued)	0(+)	00h
8	Module Interface Levels	LVTTL	01h
9	RAS Access Time (t_{RAC})	50ns (-5)	32h
		60ns (-6)	3Ch
10	CAS Access Time (t_{CAC})	15ns (-5)	0Fh
		17ns (-6)	11h
11	Module Configuration Type	None	00h
12	Refresh Rate/Type	Normal (15.625us)	00h
13	DRAM width, Primary DRAM	x16	10h
14	ERROR Checking DRAM data width	Undefined	00h
15~61*4	Undefined	Undefined	FFh
62	SPD data revision code	Rev. 1.0	01h
63*5	Checksum for bytes 0~62	Refer to note * 5	
64	Manufacturer's JEDEC ID code	Samsung	CEh
65~71	Manufacturer's JEDEC ID code	Samsung	00h
72	Manufacturer's location	Onyang Korea	01h
73	Manufacturer's Part Number	K	4Bh
74		M	4Dh
75		M	4Dh
76		3	33h
77		66	7Fh
78			36h
79			36h
80		F	46h
81		1	7Fh
82			31h

SERIAL PRESENCE DETECT INFORMATION(continued)

Byte Number	Function described	Function supported	Hex Value
83	Manufacturer's Part Number	2	32h
84		4	34h
85		C	43h
86		J	4Ah
87		1	31h
88		Hyphen	2Dh
89		Blank	7Fh
90		5	35h
		6	36h
91	Manufacturer's Revision	1	31h
92*4		Undefined	FFh
93*2	Manufacturer Date Week	Refer to note * 2	
94*2	Manufacturer Date Year	Refer to note * 2	
95~98*3	Assembly Serial #	Refer to note * 3	
99~127*4	Manufacturer Specific Data Area	Undefined	FFh
128~*4	Undefined	Undefined	FFh

* 1 : Above data are based on the SPD specification of JEDEC standard
* 2 : These bytes are programmed by code of Date Week & Date Year.
* 3 : These bytes are programmed by Samsung's own Assembly Serial # system.
* 4 : All undefined bytes will be programmed by "FFh".
* 5 : Checksum for bytes 0~62 :

Row / Column Address	$\overline{RAS}$ / $\overline{CAS}$ Access Time	Ref. rate	Checksum
10 / 10	50 / 15	15.625us	03h
	60 / 17		0Fh

SERIAL PRESENCE DETECT INFORMATION*1

- Serial PD interface Protocol : I^2C
- Current sink capability of SDA driver≤3mA
- Maximum clock frequency : 80KHz
- Contents :

Byte Number	Function described	Function supported	Hex Value
0	Number of bytes used by Module Manufacturer	128bytes	80h
1	Total SPD memory size	256bytes (2K-bit)	08h
2	Memory type	EDO	02h
3	Number of ROW Addresses	10 (1K ref.)	0Ah
4	Number of COULMN Addresses	10 (1K ref.)	0Ah
5	Number of Banks	1	01h
6	Module Data Width	72bits	48h
7	Module Data Width (Continued)	0(+)	00h
8	Module Interface Levels	LVTTL	01h
9	RAS Access Time (t_{RAC})	60ns (-6)	3Ch
10	CAS Access Time (t_{CAC})	17ns (-6)	11h
11	Module Configuration Type	ECC	02h
12	Refresh Rate/Type	Normal (15.625us)	00h
13	DRAM width, Primary DRAM	x16	10h
14	ERROR Checking DRAM data width	x4	04h
15~61*4	Undefined	Undefined	FFh
62	SPD data revision code	Rev. 1.0	01h
63*5	Checksum for bytes 0~62	Refer to note * 5	
64	Manufacturer's JEDEC ID code	Samsung	CEh
65~71	Manufacturer's JEDEC ID code	Samsung	00h
72	Manufacturer's location	Onyang Korea	01h
73	Manufacturer's Part Number	K	4Bh
74		M	4Dh
75		M	4Dh
76		3	33h
77		74	7Fh
78			37h
79			34h
80		F	46h
81		1	7Fh
82			31h
83		2	32h
84		4	34h

SERIAL PRESENCE DETECT INFORMATION(continued)

Byte Number	Function described	Function supported	Hex Value
85	Manufacturer's Part Number	C	43h
86		J	4Ah
87		1	31h
88		Hyphen	2Dh
89		Blank	7Fh
90		5	35h
		6	36h
91	Manufacturer's Revision	1	31h
92*4	Reserved for Manufacturer's Revision	Undefined	FFh
93*2	Manufacturer Date Week	Refer to note * 2	
94*2	Manufacturer Date Year	Refer to note * 2	
95~98*3	Assembly Serial #	Refer to note * 3	
99~127*4	Manufacturer Specific Data Area	Undefined	FFh
128~*4	Undefined	Undefined	FFh

* 1 : Above data are based on the SPD specification of JEDEC standard
* 2 : These bytes are programmed by code of Date Week & Date Year.
* 3 : These bytes are programmed by Samsung's own Assembly Serial # system.
* 4 : All undefined bytes will be programmed by "FFh".
* 5 : Checksum for bytes 0~62 :

Row / Column Address	$\overline{RAS}$ / $\overline{CAS}$ Access Time	Ref. rate	Checksum
10 / 10	60 / 17	15.625us	1Dh

SERIAL PRESENCE DETECT INFORMATION*1

- Serial PD interface Protocol : I^2C
- Current sink capability of SDA driver≤3mA
- Maximum clock frequency : 80KHz
- Contents :

Byte Number	Function described	Function supported	Hex Value
0	Number of bytes used by Module Manufacturer	128bytes	80h
1	Total SPD memory size	256bytes (2K-bit)	08h
2	Memory type	EDO	02h
3	Number of ROW Addresses	10 (1K ref.)	0Ah
4	Number of COULMN Addresses	10 (1K ref.)	0Ah
5	Number of Banks	2	02h
6	Module Data Width	64bits	40h
7	Module Data Width (Continued)	0(+)	00h
8	Module Interface Levels	LVTTL	01h
9	RAS Access Time (t_{RAC})	50ns (-5)	32h
		60ns (-6)	3Ch
10	CAS Access Time (t_{CAC})	15ns (-5)	0Fh
		17ns (-6)	11h
11	Module Configuration Type	None	00h
12	Refresh Rate/Type	Normal (15.625us)	00h
13	DRAM width, Primary DRAM	x16	10h
14	ERROR Checking DRAM data width	Undefined	00h
15~61*4	Undefined	Undefined	FFh
62	SPD data revision code	Rev. 1.0	01h
63*5	Checksum for bytes 0~62	Refer to note * 5	
64	Manufacturer's JEDEC ID code	Samsung	CEh
65~71	Manufacturer's JEDEC ID code	Samsung	00h
72	Manufacturer's location	Onyang Korea	01h
73	Manufacturer's Part Number	K	4Bh
74		M	4Dh
75		M	4Dh
76		3	33h
77		66	7Fh
78			36h
79			36h
80		F	46h
81		2	7Fh
82			32h

SERIAL PRESENCE DETECT INFORMATION(continued)

Byte Number	Function described	Function supported	Hex Value
83	Manufacturer's Part Number	2	32h
84		4	34h
85		C	43h
86		J	4Ah
87		1	31h
88		Hyphen	2Dh
89		Blank	7Fh
90		5	35h
		6	36h
91	Manufacturer's Revision	1	31h
92*4		Undefined	FFh
93*2	Manufacturer Date Week	Refer to note * 2	
94*2	Manufacturer Date Year	Refer to note * 2	
95~98*3	Assembly Serial #	Refer to note * 3	
99~127*4	Manufacturer Specific Data Area	Undefined	FFh
128~*4	Undefined	Undefined	FFh

* 1 : Above data are based on the SPD specification of JEDEC standard
* 2 : These bytes are programmed by code of Date Week & Date Year.
* 3 : These bytes are programmed by Samsung's own Assembly Serial # system.
* 4 : All undefined bytes will be programmed by "FFh".
* 5 : Checksum for bytes 0~62 :

Row / Column Address	$\overline{RAS}$ / $\overline{CAS}$ Access Time	Ref. rate	Checksum
10 / 10	50 / 15	15.625us	04h
	60 / 17		10h

SERIAL PRESENCE DETECT INFORMATION*1

- Serial PD interface Protocol : I^2C
- Current sink capability of SDA driver≤3mA
- Maximum clock frequency : 80KHz
- Contents :

Byte Number	Function described	Function supported	Hex Value
0	Number of bytes used by Module Manufacturer	128bytes	80h
1	Total SPD memory size	256bytes (2K-bit)	08h
2	Memory type	EDO	02h
3	Number of ROW Addresses	12 (4K ref.)	0Ch
		11 (2K ref.)	0Bh
4	Number of COULMN Addresses	9 (4K ref.)	09h
		10 (2K ref.)	0Ah
5	Number of Banks	1	01h
6	Module Data Width	64bits	40h
7	Module Data Width (Continued)	0(+)	00h
8	Module Interface Levels	LVTTL	01h
9	RAS Access Time (t_{RAC})	50ns (-5)	32h
		60ns (-6)	3Ch
10	CAS Access Time (t_{CAC})	13ns (-5)	0Dh
		15ns (-6)	0Fh
11	Module Configuration Type	None	00h
12	Refresh Rate/Type	Normal (15.625us)	00h
13	DRAM width, Primary DRAM	x8	08h
14	ERROR Checking DRAM data width	Undefined	00h
15~61*4	Undefined	Undefined	FFh
62	SPD data revision code	Rev. 1.0	01h
63*5	Checksum for bytes 0~62	Refer to note * 5	
64	Manufacturer's JEDEC ID code	Samsung	CEh
65~71	Manufacturer's JEDEC ID code	Samsung	00h
72	Manufacturer's location	Onyang Korea	01h
73	Manufacturer's Part Number	K	4Bh
74		M	4Dh
75		M	4Dh
76		3	33h
77		66	7Fh
78			36h
79			36h
80		F	46h

SERIAL PRESENCE DETECT INFORMATION(continued)

Byte Number	Function described	Function supported	Hex Value
81	Manufacturer's Part Number	2	7Fh
82			32h
83		0	30h
		1	31h
84		3	33h
85		C	43h
86		K	4Bh
87		Blank	7Fh
88		Hyphen	2Dh
89		Blank	7Fh
90		5	35h
		6	36h
91	Manufacturer's Revision	Blank	7Fh
92*4	Reserved for Manufacturer's Revision	Undefined	FFh
93*2	Manufacturer Date Week	Refer to note * 2	
94*2	Manufacturer Date Year	Refer to note * 2	
95~98*3	Assembly Seraial #	Refer to note * 3	
99~127*4	Manufacturer Specific Data Area	Undefined	FFh
128~*4	Undefined	Undefined	FFh

* 1 : Above data are based on the SPD specification of JEDEC standard
* 2 : These bytes are programmed by code of Date Week & Date Year.
* 3 : These bytes are programmed by Samsung's own Assembly Serial # system.
* 4 : All undefined bytes will be programmed by "FFh".
* 5 : Checksum for bytes 0~62 :

Row / Column Address	$\overline{RAS}$ / $\overline{CAS}$ Access Time	Ref. rate	Checksum
12 / 9	50 / 13	15.625us	FAh
	60 / 15		06h
11 / 10	50 / 13		FAh
	60 / 15		06h

SERIAL PRESENCE DETECT INFORMATION*1

- Serial PD interface Protocol : I^2C
- Current sink capability of SDA driver≤3mA
- Maximum clock frequency : 80KHz
- Contents :

Byte Number	Function described	Function supported	Hex Value
0	Number of bytes used by Module Manufacturer	128bytes	80h
1	Total SPD memory size	256bytes (2K-bit)	08h
2	Memory type	EDO	02h
3	Number of ROW Addresses	10 (1K ref.)	0Ah
4	Number of COULMN Addresses	10 (1K ref.)	0Ah
5	Number of Banks	2	02h
6	Module Data Width	72bits	48h
7	Module Data Width (Continued)	0(+)	00h
8	Module Interface Levels	LVTTL	01h
9	RAS Access Time (t_{RAC})	60ns (-6)	3Ch
10	CAS Access Time (t_{CAC})	17ns (-6)	11h
11	Module Configuration Type	ECC	02h
12	Refresh Rate/Type	Normal (15.625us)	00h
13	DRAM width, Primary DRAM	x16	10h
14	ERROR Checking DRAM data width	x4	04h
15~61*4	Undefined	Undefined	FFh
62	SPD data revision code	Rev. 1.0	01h
63*5	Checksum for bytes 0~62	Refer to note * 5	
64	Manufacturer's JEDEC ID code	Samsung	CEh
65~71	Manufacturer's JEDEC ID code	Samsung	00h
72	Manufacturer's location	Onyang Korea	01h
73	Manufacturer's Part Number	K	4Bh
74		M	4Dh
75		M	4Dh
76		3	33h
77		74	7Fh
78			37h
79			34h
80		F	46h
81		2	7Fh
82			32h
83		2	32h
84		4	34h

SERIAL PRESENCE DETECT INFORMATION(continued)

Byte Number	Function described	Function supported	Hex Value
85	Manufacturer's Part Number	C	43h
86		J	4Ah
87		1	31h
88		Hyphen	2Dh
89		Blank	7Fh
90		5	35h
		6	36h
91	Manufacturer's Revision	1	31h
92*4		Undefined	FFh
93*2	Manufacturer Date Week	Refer to note * 2	
94*2	Manufacturer Date Year	Refer to note * 2	
95~98*3	Assembly Serial #	Refer to note * 3	
99~127*4	Manufacturer Specific Data Area	Undefined	FFh
128~*4	Undefined	Undefined	FFh

* 1 : Above data are based on the SPD specification of JEDEC standard
* 2 : These bytes are programmed by code of Date Week & Date Year.
* 3 : These bytes are programmed by Samsung's own Assembly Serial # system.
* 4 : All undefined bytes will be programmed by "FFh".
* 5 : Checksum for bytes 0~62 :

Row / Column Address	$\overline{RAS}$ / $\overline{CAS}$ Access Time	Ref. rate	Checksum
10 / 10	60 / 17	15.625us	1Eh

SERIAL PRESENCE DETECT INFORMATION*1

- Serial PD interface Protocol : I^2C
- Current sink capability of SDA driver≤3mA
- Maximum clock frequency : 80KHz
- Contents :

Byte Number	Function described	Function supported	Hex Value
0	Number of bytes used by Module Manufacturer	128bytes	80h
1	Total SPD memory size	256bytes (2K-bit)	08h
2	Memory type	EDO	02h
3	Number of ROW Addresses	12 (4K ref.)	0Ch
		11 (2K ref.)	0Bh
4	Number of COULMN Addresses	9 (4K ref.)	09h
		10 (2K ref.)	0Ah
5	Number of Banks	1	01h
6	Module Data Width	72bits	48h
7	Module Data Width (Continued)	0(+)	00h
8	Module Interface Levels	LVTTL	01h
9	RAS Access Time (t_{RAC})	50ns (-5)	32h
		60ns (-6)	3Ch
10	CAS Access Time (t_{CAC})	13ns (-5)	0Dh
		15ns (-6)	0Fh
11	Module Configuration Type	ECC	02h
12	Refresh Rate/Type	Normal (15.625us)	00h
13	DRAM width, Primary DRAM	x8	08h
14	ERROR Checking DRAM data width	x8	08h
15~61*4	Undefined	Undefined	FFh
62	SPD data revision code	Rev. 1.0	01h
63*5	Checksum for bytes 0~62	Refer to note * 5	
64	Manufacturer's JEDEC ID code	Samsung	CEh
65~71	Manufacturer's JEDEC ID code	Samsung	00h
72	Manufacturer's location	Onyang Korea	01h
73	Manufacturer's Part Number	K	4Bh
74		M	4Dh
75		M	4Dh
76		3	33h
77		74	7Fh
78			37h
79			34h
80		F	46h

SERIAL PRESENCE DETECT INFORMATION(continued)

Byte Number	Function described	Function supported	Hex Value
81	Manufacturer's Part Number(continued)	2	7Fh
82			32h
83		0	30h
		1	31h
84		3	33h
85		C	43h
86		K	4Bh
87		Blank	7Fh
88		Hyphen	2Dh
89		Blank	7Fh
90		5	35h
		6	36h
91	Manufacturer's Revision	Blank	7Fh
92*4	Reserved for Manufacturer's Revision	Undefined	FFh
93*2	Manufacturer Data Week	Refer to note * 2	
94*2	Manufacturer Data Year	Refer to note * 2	
95~98*3	Assembly Serial #	Refer to note * 3	
99~127*4	Manufacturer Specific Data Area	Undefined	FFh
128~*4	Undefined	Undefined	FFh

* 1 : Above data are based on the SPD specification of JEDEC standard
* 2 : These bytes are programmed by code of Date Week & Date Year.
* 3 : These bytes are programmed by Samsung's own Assembly Serial # system.
* 4 : All undefined bytes will be programmed by "FFh".
* 5 : Checksum for bytes 0~62 :

Row / Column Address	$\overline{RAS}$ / $\overline{CAS}$ Access Time	Ref. rate	Checksum
12 / 9	50 / 13	15.625us	0Ch
	60 / 15		18h
11 / 10	50 / 13		0Ch
	60 / 15		18h

SERIAL PRESENCE DETECT INFORMATION*1

- Serial PD interface Protocol : I^2C
- Current sink capability of SDA driver≤3mA
- Maximum clock frequency : 80KHz
- Contents :

Byte Number	Function described	Function supported	Hex Value
0	Number of bytes used by Module Manufacturer	128bytes	80h
1	Total SPD memory size	256bytes (2K-bit)	08h
2	Memory type	EDO	02h
3	Number of ROW Addresses	12 (4K ref.)	0Ch
		13 (8K ref.)	0Dh
4	Number of COULMN Addresses	10 (4K ref.)	0Ah
		9 (8K ref.)	09h
5	Number of Banks	1	01h
6	Module Data Width	64bits	40h
7	Module Data Width (Continued)	0(+)	00h
8	Module Interface Levels	LVTTL	01h
9	RAS Access Time (t_{RAC})	50ns (-5)	32h
		60ns (-6)	3Ch
10	CAS Access Time (t_{CAC})	13ns (-5)	0Dh
		15ns (-6)	0Fh
11	Module Configuration Type	None	00h
12*5	Refresh Rate/Type	Reduced (7.8us)	02h
		Normal (15.625us)	00h
13	DRAM width, Primary DRAM	x16	10h
14	ERROR Checking DRAM data width	Undefined	00h
15~61*4	Undefined	Undefined	FFh
62	SPD data revision code	Rev. 1.0	01h
63*6	Checksum for bytes 0~62	Refer to note * 6	
64	Manufacturer's JEDEC ID code	Samsung	CEh
65~71	Manufacturer's JEDEC ID code	Samsung	00h
72	Manufacturer's location	Onyang Korea	01h
73	Manufacturer's Part Number	K	4Bh
74		M	4Dh
75		M	4Dh
76		3	33h
77		66	7Fh
78			36h
79			36h

SERIAL PRESENCE DETECT INFORMATION(continued)

Byte Number	Function described	Function supported	Hex Value
80	Manufacturer's Part Number	F	46h
81		4	7Fh
82			34h
83		0	30h
		8	38h
84		4	34h
85		C	43h
86		S	53h
87		1	31h
88		Hyphen	2Dh
89		Blank	7Fh
90		5	35h
		6	36h
91	Manufacturer's Revision	1	31h
92*4		Undefined	FFh
93*2	Manufacturer Date Week	Refer to note * 2	
94*2	Manufacturer Date Year	Refer to note * 2	
95~98*3	Assembly Serial #	Refer to note * 3	
99~127*4	Manufacturer Specific Data Area	Undefined	FFh
128~*4	Undefined	Undefined	FFh

* 1 : Above data are based on the SPD specification of JEDEC standard
* 2 : These bytes are programmed by binary code of Date Week or Year.
* 3 : These bytes are programmed by Samsung's own Assembly Serial # system.
* 4 : All undefined bytes will be programmed by "FFh".
* 5 : 8K refresh - CBR : 15.625us, ROR : 7.8us
  4K refresh - CBR & ROR : 15.625us
* 6 : Checksum for bytes 0 ~ 62

Row / Column Address	$\overline{RAS}$ / $\overline{CAS}$ Access Time	Ref. rate	Checksum
12 / 10	50 / 13	7.8us	05h
		15.625us	03h
	60 / 15	7.8us	11h
		15.625us	0Fh
13 / 9	50 / 13	7.8us	05h
		15.625us	03h
	60 / 15	7.8us	11h
		15.625us	0Fh

SERIAL PRESENCE DETECT INFORMATION*1

- Serial PD interface Protocol : I^2C
- Current sink capability of SDA driver≤3mA
- Maximum clock frequency : 80KHz
- Contents :

Byte Number	Function described	Function supported	Hex Value
0	Number of bytes used by Module Manufacturer	128bytes	80h
1	Total SPD memory size	256bytes (2K-bit)	08h
2	Memory type	EDO	02h
3	Number of ROW Addresses	12 (4K ref.)	0Ch
4	Number of COULMN Addresses	10 (4K ref.)	0Ah
5	Number of Banks	1	01h
6	Module Data Width	72bits	48h
7	Module Data Width (Continued)	0(+)	00h
8	Module Interface Levels	LVTTL	01h
9	RAS Access Time (t_{RAC})	50ns (-5)	32h
		60ns (-6)	3Ch
10	CAS Access Time (t_{CAC})	13ns (-5)	0Dh
		15ns (-6)	0Fh
11	Module Configuration Type	ECC	02h
12	Refresh Rate/Type	Normal (15.625us)	00h
13	DRAM width, Primary DRAM	x16	10h
14	ERROR Checking DRAM data width	x4	04h
15~61*4	Undefined	Undefined	FFh
62	SPD data revision code	Rev. 1.0	01h
63*5	Checksum for bytes 0~62	Refer to note * 5	
64	Manufacturer's JEDEC ID code	Samsung	CEh
65~71	Manufacturer's JEDEC ID code	Samsung	00h
72	Manufacturer's location	Onyang Korea	01h
73	Manufacturer's Part Number	K	4Bh
74		M	4Dh
75		M	4Dh
76		3	33h
77		74	7Fh
78			37h
79			34h
80		F	46h
81		4	7Fh
82			34h

SERIAL PRESENCE DETECT INFORMATION(continued)

Byte Number	Function described	Function supported	Hex Value
83	Manufacturer's Part Number	0	30h
84		4	34h
85		C	43h
86		S	53h
87		1	31h
88		Hyphen	2Dh
89		Blank	7Fh
90		5	35h
		6	36h
91	Manufacturer's Revision	1	31h
92*4		Undefined	FFh
93*2	Manufacturer Date Week	Refer to note * 2	
94*2	Manufacturer Date Year	Refer to note * 2	
95~98*3	Assembly Serial #	Refer to note * 3	
99~127*4	Manufacturer Specific Data Area	Undefined	FFh
128~*4	Undefined	Undefined	FFh

* 1 : Above data are based on the SPD specification of JEDEC standard
* 2 : These bytes are programmed by binary code of Date Week or Year.
* 3 : These bytes are programmed by Samsung's own Assembly Serial # system.
* 4 : All undefined bytes will be programmed by "FFh".
* 5 : Checksum for bytes 0 ~ 62

Row / Column Address	$\overline{RAS}$ / $\overline{CAS}$ Access Time	Ref. rate	Checksum
12 / 10	50 / 13	15.625us	11h
	60 / 15		1Dh

SERIAL PRESENCE DETECT INFORMATION*1

- Serial PD interface Protocol : I^2C
- Current sink capability of SDA driver≤3mA
- Maximum clock frequency : 80KHz
- Contents :

Byte Number	Function described	Function supported	Hex Value
0	Number of bytes used by Module Manufacturer	128bytes	80h
1	Total SPD memory size	256bytes (2K-bit)	08h
2	Memory type	EDO	02h
3	Number of ROW Addresses	12 (4K ref.)	0Ch
		13 (8K ref.)	0Dh
4	Number of COULMN Addresses	11 (4K ref.)	0Bh
		10 (8K ref.)	0Ah
5	Number of Banks	1	01h
6	Module Data Width	64bits	40h
7	Module Data Width (Continued)	0(+)	00h
8	Module Interface Levels	LVTTL	01h
9	RAS Access Time (t_{RAC})	50ns (-5)	32h
		60ns (-6)	3Ch
10	CAS Access Time (t_{CAC})	13ns (-5)	0Dh
		15ns (-6)	0Fh
11	Module Configuration Type	None	00h
12*5	Refresh Rate/Type	Reduced (7.8us)	02h
		Normal (15.625us)	00h
13	DRAM width, Primary DRAM	x8	08h
14	ERROR Checking DRAM data width	Undefined	00h
15~61*4	Undefined	Undefined	FFh
62	SPD data revision code	Rev. 1.0	01h
63*6	Checksum for bytes 0~62	Refer to note * 6	
64	Manufacturer's JEDEC ID code	Samsung	CEh
65~71	Manufacturer's JEDEC ID code	Samsung	00h
72	Manufacturer's location	Onyang Korea	01h
73	Manufacturer's Part Number	K	4Bh
74		M	4Dh
75		M	4Dh
76		3	33h
77		66	7Fh
78			36h
79			36h

SERIAL PRESENCE DETECT INFORMATION(continued)

Byte Number	Function described	Function supported	Hex Value
80	Manufacturer's Part Number(continued)	F	46h
81		8	7Fh
82			38h
83		0	30h
		8	38h
84		3	33h
85		C	43h
86		K	4Bh
87		2	32h
88		Hyphen	2Dh
89		Blank	7Fh
90		5	35h
		6	36h
91	Manufacturer's Revision	2	32h
92*4		Undefined	FFh
93*2	Manufacturer Date Week	Refer to note * 2	
94*2	Manufacturer Date Year	Refer to note * 2	
95~98*3	Assembly Serial #	Refer to note * 3	
99~127*4	Manufacturer Specific Data Area	Undefined	FFh
128~*4	Undefined	Undefined	FFh

* 1 : Above data are based on the SPD specification of JEDEC standard
* 2 : These bytes are programmed by binary code of Date Week or Year.
* 3 : These bytes are programmed by Samsung's own Assembly Serial # system.
* 4 : All undefined bytes will be programmed by "FFh".
* 5 : 8K refresh - CBR : 15.625us, ROR : 7.8us
  4K refresh - CBR & ROR : 15.625us
* 6 : Checksum for bytes 0 ~ 62

Row / Column Address	$\overline{RAS}$ / $\overline{CAS}$ Access Time	Ref. rate	Checksum
12 / 11	50 / 13	7.8us	FEh
		15.625us	FCh
	60 / 15	7.8us	0Ah
		15.625us	08h
13 / 10	50 / 13	7.8us	FEh
		15.625us	FCh
	60 / 15	7.8us	0Ah
		15.625us	08h

SERIAL PRESENCE DETECT INFORMATION*1

- Serial PD interface Protocol : I^2C
- Current sink capability of SDA driver≤3mA
- Maximum clock frequency : 80KHz
- Contents :

Byte Number	Function described	Function supported	Hex Value
0	Number of bytes used by Module Manufacturer	128bytes	80h
1	Total SPD memory size	256bytes (2K-bit)	08h
2	Memory type	EDO	02h
3	Number of ROW Addresses	12 (4K ref.)	0Ch
		13 (8K ref.)	0Dh
4	Number of COULMN Addresses	10 (4K ref.)	0Ah
		9 (8K ref.)	09h
5	Number of Banks	2	02h
6	Module Data Width	64bits	40h
7	Module Data Width (Continued)	0(+)	00h
8	Module Interface Levels	LVTTL	01h
9	RAS Access Time (t_{RAC})	50ns (-5)	32h
		60ns (-6)	3Ch
10	CAS Access Time (t_{CAC})	13ns (-5)	0Dh
		15ns (-6)	0Fh
11	Module Configuration Type	None	00h
12*5	Refresh Rate/Type	Reduced (7.8us)	02h
		Normal (15.625us)	00h
13	DRAM width, Primary DRAM	x16	10h
14	ERROR Checking DRAM data width	Undefined	00h
15~61*4	Undefined	Undefined	FFh
62	SPD data revision code	Rev. 1.0	01h
63*6	Checksum for bytes 0~62	Refer to note * 6	
64	Manufacturer's JEDEC ID code	Samsung	CEh
65~71	Manufacturer's JEDEC ID code	Samsung	00h
72	Manufacturer's location	Onyang Korea	01h
73	Manufacturer's Part Number	K	4Bh
74		M	4Dh
75		M	4Dh
76		3	33h
77		66	7Fh
78			36h
79			36h

SERIAL PRESENCE DETECT INFORMATION(continued)

Byte Number	Function described	Function supported	Hex Value
80	Manufacturer's Part Number	F	46h
81		8	7Fh
82			38h
83		0	30h
		8	38h
84		4	34h
85		C	43h
86		S	53h
87		1	31h
88		Hyphen	2Dh
89		Blank	7Fh
90		5	35h
		6	36h
91	Manufacturer's Revision	1	31h
92*4		Undefined	FFh
93*2	Manufacturer Date Week	Refer to note * 2	
94*2	Manufacturer Date Year	Refer to note * 2	
95~98*3	Assembly Seraial #	Refer to note * 3	
99~127*4	Manufacturer Specific Data Area	Undefined	FFh
128~*4	Undefined	Undefined	FFh

* 1 : Above data are based on the SPD specification of JEDEC standard
* 2 : These bytes are programmed by binary code of Date Week or Year.
* 3 : These bytes are programmed by Samsung's own Assembly Serial # system.
* 4 : All undefined bytes will be programmed by "FFh".
* 5 : 8K refresh - CBR : 15.625us, ROR : 7.8us
  4K refresh - CBR & ROR : 15.625us
* 6 : Checksum for bytes 0 ~ 62

Row / Column Address	$\overline{RAS}$ / $\overline{CAS}$ Access Time	Ref. rate	Checksum
12 / 10	50 / 13	7.8us	06h
		15.625us	04h
	60 / 15	7.8us	12h
		15.625us	10h
13 / 9	50 / 13	7.8us	06h
		15.625us	04h
	60 / 15	7.8us	12h
		15.625us	10h

SERIAL PRESENCE DETECT INFORMATION*1

- Serial PD interface Protocol : I^2C
- Current sink capability of SDA driver≤3mA
- Maximum clock frequency : 80KHz
- Contents :

Byte Number	Function described	Function supported	Hex Value
0	Number of bytes used by Module Manufacturer	128bytes	80h
1	Total SPD memory size	256bytes (2K-bit)	08h
2	Memory type	EDO	02h
3	Number of ROW Addresses	12 (4K ref.)	0Ch
		13 (8K ref.)	0Dh
4	Number of COULMN Addresses	11 (4K ref.)	0Bh
		10 (8K ref.)	0Ah
5	Number of Banks	1	01h
6	Module Data Width	72bits	48h
7	Module Data Width (Continued)	0(+)	00h
8	Module Interface Levels	LVTTL	01h
9	RAS Access Time (t_{RAC})	50ns (-5)	32h
		60ns (-6)	3Ch
10	CAS Access Time (t_{CAC})	13ns (-5)	0Dh
		15ns (-6)	0Fh
11	Module Configuration Type	ECC	02h
12*5	Refresh Rate/Type	Reduced (7.8us)	02h
		Normal (15.625us)	00h
13	DRAM width, Primary DRAM	x8	08h
14	ERROR Checking DRAM data width	x8	08h
15~61*4	Undefined	Undefined	FFh
62	SPD data revision code	Rev. 1.0	01h
63*6	Checksum for bytes 0~62	Refer to note * 6	
64	Manufacturer's JEDEC ID code	Samsung	CEh
65~71	Manufacturer's JEDEC ID code	Samsung	00h
72	Manufacturer's location	Onyang Korea	01h
73	Manufacturer's Part Number	K	4Bh
74		M	4Dh
75		M	4Dh
76		3	33h
77		74	7Fh
78			37h
79			34h

SERIAL PRESENCE DETECT INFORMATION(continued)

Byte Number	Function described	Function supported	Hex Value
80	Manufacturer's Part Number(continued)	F	46h
81		8	7Fh
82			38h
83		0	30h
		8	38h
84		3	33h
85		C	43h
86		K	4Bh
87		1	31h
88		Hyphen	2Dh
89		Blank	7Fh
90		5	35h
		6	36h
91	Manufacturer's Revision	1	31h
92*4		Undefined	FFh
93*2	Manufacturer Data Week	Refer to note * 2	
94*2	Manufacturer Data Year	Refer to note * 2	
95~98*3	Assembly Serial #	Refer to note * 3	
99~127*4	Manufacturer Specific Data Area	Undefined	FFh
128~*4	Undefined	Undefined	FFh

* 1 : Above data are based on the SPD specification of JEDEC standard
* 2 : These bytes are programmed by binary code of Date Week or Year.
* 3 : These bytes are programmed by Samsung's own Assembly Serial # system.
* 4 : All undefined bytes will be programmed by "FFh".
* 5 : 8K refresh - CBR : 15.625us, ROR : 7.8us
4K refresh - CBR & ROR : 15.625us
* 6 : Checksum for bytes 0 ~ 62

Row / Column Address	$\overline{RAS}$ / $\overline{CAS}$ Access Time	Ref. rate	Checksum
12 / 11	50 / 13	7.8us	10h
		15.625us	0Eh
	60 / 15	7.8us	1Ch
		15.625us	1Ah
13 / 10	50 / 13	7.8us	10h
		15.625us	0Eh
	60 / 15	7.8us	1Ch
		15.625us	1Ah

SERIAL PRESENCE DETECT INFORMATION*1

- Serial PD interface Protocol : I^2C
- Current sink capability of SDA driver≤3mA
- Maximum clock frequency : 80KHz
- Contents :

Byte Number	Function described	Function supported	Hex Value
0	Number of bytes used by Module Manufacturer	128bytes	80h
1	Total SPD memory size	256bytes (2K-bit)	08h
2	Nemory type	EDO	02h
3	Number of ROW Addresses	12 (4K ref.)	0Ch
4	Number of COULMN Addresses	10 (4K ref.)	0Ah
5	Number of Banks	2	02h
6	Module Data Width	72bits	48h
7	Module Data Width (Continued)	0(+)	00h
8	Module Interface Levels	LVTTL	01h
9	RAS Access Time (t_{RAC})	50ns (-5)	32h
		60ns (-6)	3Ch
10	CAS Access Time (t_{CAC})	13ns (-5)	0Dh
		15ns (-6)	0Fh
11	Module Configuration Type	ECC	02h
12	Refresh Rate/Type	Normal (15.625us)	00h
13	DRAM width, Primary DRAM	x16	10h
14	ERROR Checking DRAM data width	x4	04h
15~61*4	Undefined	Undefined	FFh
62	SPD data revision code	Rev. 1.0	01h
63*5	Checksum for bytes 0~62	Refer to note * 5	
64	Manufacturer's JEDEC ID code	Samsung	CEh
65~71	Manufacturer's JEDEC ID code	Samsung	00h
72	Manufacturer's location	Onyang Korea	01h
73	Manufacturer's Part Number	K	4Bh
74		M	4Dh
75		M	4Dh
76		3	33h
77		74	7Fh
78			37h
79			34h
80		F	46h
81		8	7Fh
82			38h

SERIAL PRESENCE DETECT INFORMATION(continued)

Byte Number	Function described	Function supported	Hex Value
83	Manufacturer's Part Number	0	30h
84		4	34h
85		C	43h
86		S	53h
87		1	31h
88		Hyphen	2Dh
89		Blank	7Fh
90		5	35h
		6	36h
91	Manufacturer's Revision	1	31h
92*4		Undefined	FFh
93*2	Manufacturer Data Week	Refer to note * 2	
94*2	Manufacturer Data Year	Refer to note * 2	
95~98*3	Assembly Serial #	Refer to note * 3	
99~127*4	Manufacturer Specific Data Area	Undefined	FFh
128~*4	Undefined	Undefined	FFh

* 1 : Above data are based on the SPD specification of JEDEC standard
* 2 : These bytes are programmed by binary code of Date Week or Year.
* 3 : These bytes are programmed by Samsung's own Assembly Serial # system.
* 4 : All undefined bytes will be programmed by "FFh".
* 5 : Checksum for bytes 0 ~ 62

6

Row / Column Address	$\overline{RAS}$ / $\overline{CAS}$ Access Time	Ref. rate	Checksum
12 / 10	50 / 13	15.625us	12h
	60 / 15		1Eh

SERIAL PRESENCE DETECT INFORMATION*1

- Serial PD interface Protocol : I^2C
- Current sink capability of SDA driver≤3mA
- Maximum clock frequency : 80KHz
- Contents :

Byte Number	Function described	Function supported	Hex Value
0	Number of bytes used by Module Manufacturer	128bytes	80h
1	Total SPD memory size	256bytes (2K-bit)	08h
2	Memory type	EDO	02h
3	Number of ROW Addresses	12 (4K ref.)	0Ch
		13 (8K ref.)	0Dh
4	Number of COULMN Addresses	12 (4K ref.)	0Ch
		11 (8K ref.)	0Bh
5	Number of Banks	1	01h
6	Module Data Width	64bits	40h
7	Module Data Width (Continued)	0(+)	00h
8	Module Interface Levels	LVTTL	01h
9	RAS Access Time (t_{RAC})	50ns (-5)	32h
		60ns (-6)	3Ch
10	CAS Access Time (t_{CAC})	13ns (-5)	0Dh
		15ns (-6)	0Fh
11	Module Configuration Type	None	00h
12*5	Refresh Rate/Type	Reduced (7.8us)	02h
		Normal (15.625us)	00h
13	DRAM width, Primary DRAM	x4	04h
14	ERROR Checking DRAM data width	Undefined	00h
15~61*4	Undefined	Undefined	FFh
62	SPD data revision code	Rev. 1.0	01h
63*6	Checksum for bytes 0~62	Refer to note * 6	
64	Manufacturer's JEDEC ID code	Samsung	CEh
65~71	Manufacturer's JEDEC ID code	Samsung	00h
72	Manufacturer's location	Onyang Korea	01h
73	Manufacturer's Part Number	K	4Bh
74		M	4Dh
75		M	4Dh
76		3	33h
77		66	7Fh
78			36h
79			36h

SERIAL PRESENCE DETECT INFORMATION(continued)

Byte Number	Function described	Function supported	Hex Value
80	Manufacturer's Part Number(continued)	F	46h
81		16	31h
82			36h
83		0	30h
		8	38h
84		0	30h
85		C	43h
86		K	4Bh
87		2	32h
88		Hyphen	2Dh
89		Blank	7Fh
90		5	35h
		6	36h
91	Manufacturer's Revision	2	32h
92*4		Undefined	FFh
93*2	Manufacturer Data Week	Refer to note * 2	
94*2	Manufacturer Data Year	Refer to note * 2	
95~98*3	Assembly Serial #	Refer to note * 3	
99~127*4	Manufacturer Specific Data Area	Undefined	FFh
128~*4	Undefined	Undefined	FFh

* 1 : Above data are based on the SPD specification of JEDEC standard
* 2 : These bytes are programmed by binary code of Date Week or Year.
* 3 : These bytes are programmed by Samsung's own Assembly Serial # system.
* 4 : All undefined bytes will be programmed by "FFh".
* 5 : 8K refresh - CBR : 15.625us, ROR : 7.8us
  4K refresh - CBR & ROR : 15.625us
* 6 : Checksum for bytes 0 ~ 62

Row / Column Address	$\overline{RAS}$ / $\overline{CAS}$ Access Time	Ref. rate	Checksum
12 / 12	50 / 13	7.8us	FBh
		15.625us	F9h
	60 / 15	7.8us	07h
		15.625us	05h
13 / 11	50 / 13	7.8us	FBh
		15.625us	F9h
	60 / 15	7.8us	07h
		15.625us	05h

SERIAL PRESENCE DETECT INFORMATION*1

- Serial PD interface Protocol : I^2C
- Current sink capability of SDA driver≤3mA
- Maximum clock frequency : 80KHz
- Contents :

Byte Number	Function described	Function supported	Hex Value
0	Number of bytes used by Module Manufacturer	128bytes	80h
1	Total SPD memory size	256bytes (2K-bit)	08h
2	Memory type	EDO	02h
3	Number of ROW Addresses	12 (4K ref.)	0Ch
		13 (8K ref.)	0Dh
4	Number of COULMN Addresses	12 (4K ref.)	0Ch
		11 (8K ref.)	0Bh
5	Number of Banks	1	01h
6	Module Data Width	72bits	48h
7	Module Data Width (Continued)	0(+)	00h
8	Module Interface Levels	LVTTL	01h
9	RAS Access Time (tRAC)	50ns (-5)	32h
		60ns (-6)	3Ch
10	CAS Access Time (tCAC)	13ns (-5)	0Dh
		15ns (-6)	0Fh
11	Module Configuration Type	ECC	02h
12*5	Refresh Rate/Type	Reduced (7.8us)	02h
		Normal (15.625us)	00h
13	DRAM width, Primary DRAM	x4	04h
14	ERROR Checking DRAM data width	x4	04h
15~61*4	Undefined	Undefined	FFh
62	SPD data revision code	Rev. 1.0	01h
63*6	Checksum for bytes 0~62	Refer to note * 6	
64	Manufacturer's JEDEC ID code	Samsung	CEh
65~71	Manufacturer's JEDEC ID code	Samsung	00h
72	Manufacturer's location	Onyang Korea	01h
73	Manufacturer's Part Number	K	4Bh
74		M	4Dh
75		M	4Dh
76		3	33h
77		74	7Fh
78			37h
79			34h

SERIAL PRESENCE DETECT INFORMATION(continued)

Byte Number	Function described	Function supported	Hex Value
80	Manufacturer's Part Number(continued)	F	46h
81		16	31h
82			36h
83		0	30h
		8	38h
84		0	30h
85		C	43h
86		K	4Bh
87		1	31h
88		Hyphen	2Dh
89		Blank	7Fh
90		5	35h
		6	36h
91	Manufacturer's Revision	1	31h
92*4		Undefined	FFh
93*2	Manufacturer Date Week	Refer to note * 2	
94*2	Manufacturer Date Year	Refer to note * 2	
95~98*3	Assembly Serial #	Refer to note * 3	
99~127*4	Manufacturer Specific Data Area	Undefined	FFh
128~*4	Undefined	Undefined	FFh

* 1 : Above data are based on the SPD specification of JEDEC standard
* 2 : These bytes are programmed by binary code of Date Week or Year.
* 3 : These bytes are programmed by Samsung's own Assembly Serial # system.
* 4 : All undefined bytes will be programmed by "FFh".
* 5 : 8K refresh - CBR : 15.625us, ROR : 7.8us
  4K refresh - CBR & ROR : 15.625us
* 6 : Checksum for bytes 0 ~ 62

Row / Column Address	$\overline{RAS}$ / $\overline{CAS}$ Access Time	Ref. rate	Checksum
12 / 12	50 / 13	7.8us	09h
		15.625us	07h
	60 / 15	7.8us	15h
		15.625us	13h
13 / 11	50 / 13	7.8us	09h
		15.625us	07h
	60 / 15	7.8us	15h
		15.625us	13h

SERIAL PRESENCE DETECT INFORMATION*1

- Serial PD interface Protocol : I^2C
- Current sink capability of SDA driver≤3mA
- Maximum clock frequency : 80KHz
- Contents :

Byte Number	Function described	Function supported	Hex Value
0	Number of bytes used by Module Manufacturer	128bytes	80h
1	Total SPD memory size	256bytes (2K-bit)	08h
2	Memory type	EDO	02h
3	Number of ROW Addresses	12 (4K ref.)	0Ch
		13 (8K ref.)	0Dh
4	Number of COULMN Addresses	12 (4K ref.)	0Ch
		11 (8K ref.)	0Bh
5	Number of Banks	2	02h
6	Module Data Width	72bits	48h
7	Module Data Width (Continued)	0(+)	00h
8	Module Interface Levels	LVTTL	01h
9	RAS Access Time (t_{RAC})	50ns (-5)	32h
		60ns (-6)	3Ch
10	CAS Access Time (t_{CAC})	13ns (-5)	0Dh
		15ns (-6)	0Fh
11	Module Configuration Type	ECC	02h
12*5	Refresh Rate/Type	Reduced (7.8us)	02h
		Normal (15.625us)	00h
13	DRAM width, Primary DRAM	x4	04h
14	ERROR Checking DRAM data width	x4	04h
15~61*4	Undefined	Undefined	FFh
62	SPD data revision code	Rev. 1.0	01h
63*6	Checksum for bytes 0~62	Refer to note * 6	
64	Manufacturer's JEDEC ID code	Samsung	CEh
65~71	Manufacturer's JEDEC ID code	Samsung	00h
72	Manufacturer's location	Onyang Korea	01h
73	Manufacturer's Part Number	K	4Bh
74		M	4Dh
75		M	4Dh
76		3	33h
77		74	7Fh
78			37h
79			34h

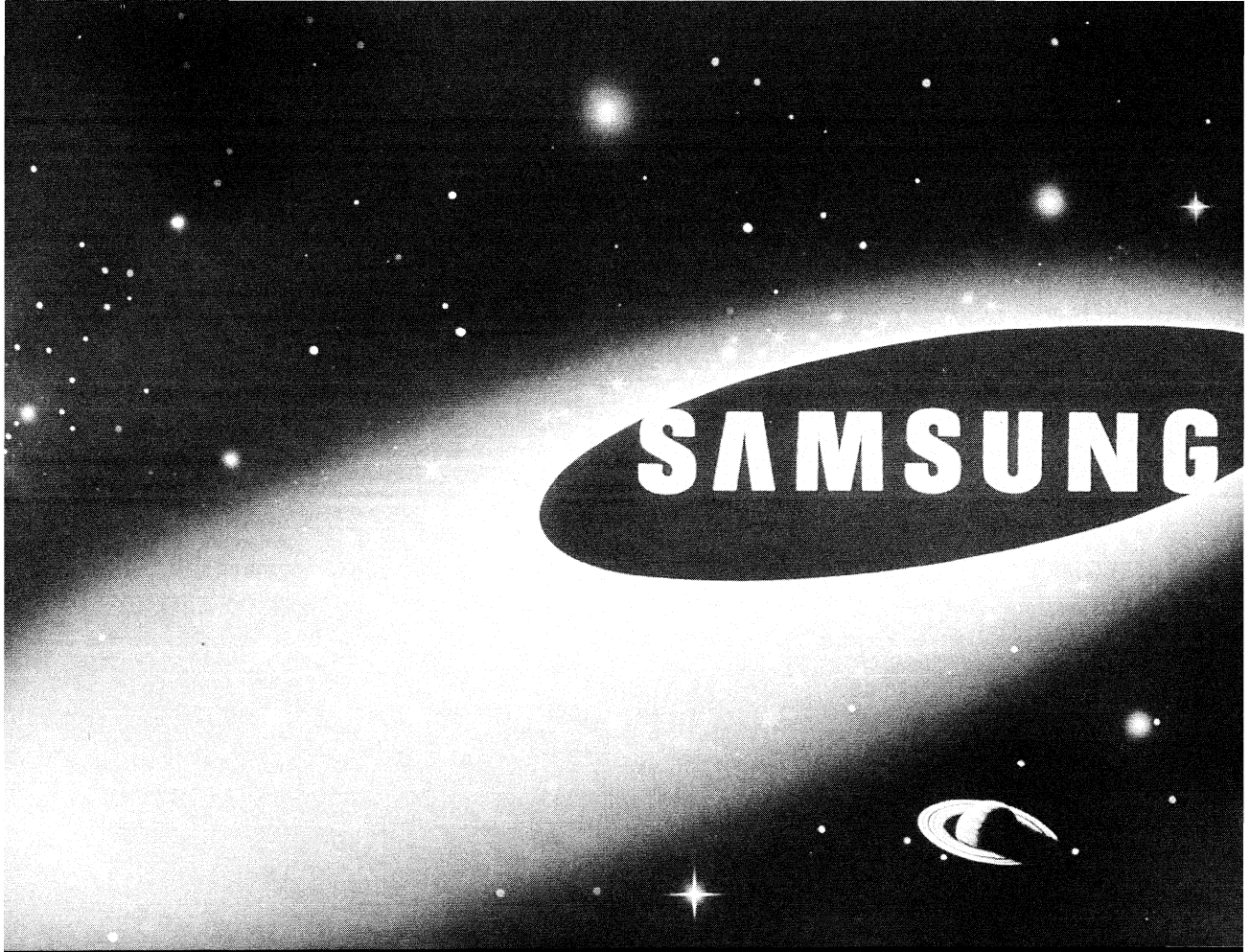
SERIAL PRESENCE DETECT INFORMATION(continued)

Byte Number	Function described	Function supported	Hex Value
80	Manufacturer's Part Number(continued)	F	46h
81		32	33h
82			32h
83		0	30h
		8	38h
84		0	30h
85		C	43h
86		K	4Bh
87		1	31h
88		Hyphen	2Dh
89		Blank	7Fh
90		5	35h
		6	36h
91	Manufacturer's Revision	1	31h
92*4		Undefined	FFh
93*2	Manufacturer Date Week	Refer to Note * 2	
94*2	Manufacturer Date Year	Refer to Note * 2	
95~98*3	Assembly Serial #	Refer to Note * 3	
99~127*4	Manufacturer Specific Data Area	Undefined	FFh
128~*4	Undefined	Undefined	FFh

* 1 : Above data are based on the SPD specification of JEDEC standard
* 2 : These bytes are programmed by binary code of Date Week or Year.
* 3 : These bytes are programmed by Samsung's own Assembly Serial # system.
* 4 : All undefined bytes will be programmed by "FFh".
* 5 : 8K refresh - CBR : 15.625us, ROR : 7.8us
  4K refresh - CBR & ROR : 15.625us
* 6 : Checksum for bytes 0 ~ 62

Row / Column Address	$\overline{RAS}$ / $\overline{CAS}$ Access Time	Ref. rate	Checksum
12 / 12	50 / 13	7.8us	0Ah
		15.625us	08h
	60 / 15	7.8us	16h
		15.625us	14h
13 / 11	50 / 13	7.8us	0Ah
		15.625us	08h
	60 / 15	7.8us	16h
		15.625us	14h

NOTES



SALES OFFICES and MANUFACTURER'S REPRESENTATIVES 7

SAMSUNG SEMICONDUCTOR SALES OFFICE-U.S.A.

Northwest
3655 North First Street
San Jose, CA 95134
TEL : 408-544-4000
FAX : 408-544-4934

Southwest
7700 Irvine Center Drive
Suite 150, Irvine, CA 92618
TEL : 714-753-7530
FAX : 714-753-7544

North Central
1111 Plaza Drive, Suite 100
Schaumburg, IL 60173
TEL : 847-969-9515
FAX : 847-969-9509

South Central
8303 Mopac Blvd. Suite A100
Austin, TX 78759
TEL : 512-342-1904
FAX : 512-342-1915

Northeast
238 Littleton Road. Suite 201
Westford, MA 01886
TEL : 978-392-2220
FAX : 978-392-2240

Southeast
8000 Regency Pkwy, Suite 585
Cary, NC 27511
TEL : 919-380-8483
FAX : 919-380-8492

SAMSUNG SEMICONDUCTOR REPRESENTATIVES

ALABAMA

REP ONE
2707 Artie Street, Bldg 200 — TEL : 205-539-7371
Suite 12, Huntsville, AL 35805 — FAX : 205-533-4509

ARIZONA

SUMMIT SALES
7802 E. Gray Rd. Suite #600 — TEL : 602-998-4850
Scottsdale, AZ 85260 — FAX : 602-998-5274

CALIFORNIA

BESTRONICS
9988 Hibert Street — TEL : 619-693-1111
Suite 210, San Diego, CA 92131 — FAX : 619-693-1963

I-SQUARED
3255-1 Scott Blvd, Suite 102 — TEL : 408-988-3400
Santa Clara, CA 95054 — FAX : 408-988-2079

I-SQUARED
9198 Greenback Lane, #101 — TEL : 916-989-0843
Orangevale, CA 95662 — FAX : 916-989-2841

WESTAR
15265 Alton Parkway, — TEL : 714-453-7900
Suite #400, Irvine, CA 92718 — FAX : 714-453-7930

WESTAR
26500 Agoura Rd., Suite #204 — TEL : 818-880-0594
Calabasas, CA 91302 — FAX : 818-880-5013

CANADA

InTELaTECH, INC.
5225 Orbitor Drive, Suite 2 — TEL : 905-629-0082
Mississauga, Ontario — FAX : 905-629-1795
Canada L4W 4Y8

InTELaTECH, INC.
300 3665 Kings Way — TEL : 604-434-5699
Vancouver, B.C. V5R 5W2 — FAX : 604-434-5655

InTELaTECH, INC.
6765 Cote De Liesse, Suite #366 — TEL : 514-343-4877
St. Laurent, Quebec — FAX : 514-343-4355
Canada H4T 1E5

InTELaTECH, INC.
140, 6815 8th Street N.E — TEL : 403-686-2268
Calgary, AB T2E7H7 Canada — FAX : 403-686-6926

InTELaTECH, INC.
260 Hearst Way, Ste 248 — TEL : 613-599-8330
Kanata, ON K2L3H1 Canada — FAX : 613-599-7329

COLORADO

FRONT RANGE MARKETING, INC.
3100 Arapahoe Road, #404 — TEL : 303-443-4780
Boulder, CO 80303 — FAX : 303-447-0371

FLORIDA

DYNE-A-MARK CORPORATION
500 Winderley Place — TEL : 407-660-1661
Suite #100, Maitland, FL 32751 — FAX : 407-660-9407

DYNE-A-MARK CORPORATION
742 Penguin Avenue NE — TEL : 407-725-7470
Palm Bay, FL 32905 — FAX : 407-984-2718

DYNE-A-MARK CORPORATION
Two Prospect Park Business Ctr, — TEL : 954-485-3500
3351 N.W. 55th Street — FAX : 954-485-6555
Fort Lauderdale, FL 33309

DYNE-A-MARK CORPORATION
508 Palm Drive — TEL : 813-586-3778
Largo, FL 34640 — FAX : 813-586-3863

GEORGIA

SOUTH ATLANTIC COMPONENT SALES
728 Holcomb Bridge Rd, — TEL : 770-447-6154
Norcross, GA 30071 — FAX : 770-447-6714

7

ILLINOIS

DAVIX INTERNATIONAL
1655 N. Arlington Heights RD. TEL : 847-259-5300
Suite #204 East, Arlington Heights, FAX : 847-259-5428
IL 60004

IDAHO

INTERMOUNTAIN TECH
1310 East First Street TEL : 208-888-6071
Meridian, Idaho 83642 FAX : 208-888-6074

INDIANA

GEN II MARKETING, INC.
1415 Magnavox Way, #130 TEL : 219-436-4485
Ft, Wayne, IN 46804 FAX : 219-436-1977
GEN II MARKETING, INC.
31 E. Main Street TEL : 317-848-3083
Carmel, IN 46032 FAX : 317-848-1264

IKANSAS

CUSTOMER 1ST
10540 Marty #200N TEL : 913-385-0390
Overland Park, KS 66212 FAX : 612-851-7907

KENTUCKY

GEN II MARKETING, INC.
861 Corporate Drive, Suite 210 TEL : 606-223-9181
Lexington, KY 40503 FAX : 606-223-2864

MARYLAND

BEACON NORTH
8965 Guilford Road TEL : 410-381-4309
Columbia, MD 21046 FAX : 410-381-4752
BESCON NORTH
2821 Sommersby Road TEL : 301-831-5492
Mt. Airy, MD 21771 FAX : 301-829-2167

MASSACHUSETTS

NEW TECH SOLUTIONS
1 Van de Graaff Drive 4th Floor TEL : 617-229-8888
Burlington, MA 01803 FAX : 617-229-1614

MICHIGAN

GEN II MARKETING, INC.
4849 Gallagher Road TEL : 810-231-0004
Whitmore Lake, MI 48189 FAX : 810-231-0009

MINESOTA

CUSTOMER 1ST
2950 Metro Drive, Suite #101 TEL : 612-851-7909
Bloomington, MN 55425 FAX : 612-851-7907

NORTH CAROLINA

SOUTH ATLANTIC COMPONENT SALES
211 Commonwealth Court TEL : 919-380-1133
Cary, NC 27511 FAX : 919-380-0801
SOUTH ATLANTIC COMPONENT SALES
5200 Park Road, STE. 103 TEL : 704-525-0510
Charlotte, NC 28209 FAX : 704-525-9714

NEW YORK

NECCO
11 Oval Drive Suite 169 TEL : 516-234-2525
Islandia, NY 11722 FAX : 516-234-2707
T-SQUARED
7353 Victor-Pittsford Road TEL : 716-924-9101
Victor, NY 14564 FAX : 716-924-4946
T-SQUARED
4226 Bayview Rd, TEL : 716-824-6508
Blasdell, NY 14219 FAX : 716-824-3484
T-SQUARED
1790 Pennsylvania Avenue TEL : 607-625-3983
Apalachin, NY 13732 FAX : 607-625-5294

OREGON

ADVANCED TECH MKTG, INC.
4900 SW Griffith Drive, Suite #155 TEL : 503-643-8307
Beaverton, OR 97005 FAX : 503-643-4364

OHIO

BAILEY, J.N. & ASSOC.
503 Windsor Park DR. TEL : 937-291-1354
Centerville, OH 45459 FAX : 937-291-9023
BAILEY, J.N. & ASSOC.
5366 Trumpeter Blvd, TEL : 440-230-0778
Royalton, OH 44133 FAX : 440-230-0042
BAILEY, J.N. & ASSOC.
3591 Milton Avenue TEL : 614-262-7274
Columbus, OH 43214 FAX : 614-262-0384
BAILEY, J.N. & ASSOC.
1638 Longwood AVE, TEL : 216-605-0410
Cleveland, OH 44124 FAX : 216-605-0411

PENNSYLVANIA

CMS SALES & MARKETING INC.
521 Plymouth Road, Suite #111 TEL : 610-834-6840
Plymouth Meeting, PA 19462 FAX : 610-834-6848

PUERTO RICO

DIGIT-TECH
P.O.BOX 1945 — TEL : 787-892-4260
Calle DR, Veve #59 Altos — FAX : 787-892-3366
San German, Puerto Rico 00683

B/B Tech Sales
Ruiz Belvis Esq. — TEL : 305-477-0341/2
Carro, Altos, San German — FAX : 305-477-0343
Puerto Rico 00683

UTAH

FRONT RANGE MARKETING INC.
448 East 6400 South, Suite 280 — TEL : 801-288-2500
Murray, UT 84107 — FAX : 801-288-2505

VIRGINIA

BEACON NORTH
21607 Goodwin Court — TEL : 703-855-8235
Ashburn, VA 22011 — FAX : 703-724-4033

BEACON NORTH
1324 Gristmill Drive — TEL : 804-296-6245
Charlottesville, VA 22902 — FAX : 804-296-6273

WASHINGTON

ADVANCED TECH MKTG, INC.
8521 154th AVE, NE — TEL : 425-869-7636
Redmond, WA 98052 — FAX : 425-869-9841

WISCONSIN

DAVIX INTERNATIONAL
N84 W15787 Menomonee AVE. — TEL : 414-255-1600
Menomonee Falls, WI 53051 — FAX : 414-255-1863

TEXAS

VIELOCK ASSOCIATES
555 Repulic Drive, suite 105 — TEL : 972-881-1940
Plano, TX 75074 — FAX : 972-423-8556

VIELOCK ASSOC.
9811 Anderson Mill Road, #201 — TEL : 512-918-1189
Austin, TX 78750 — FAX : 512-918-1199

VIELOCK ASSOC.
10700 Richmond Ave, STE. #108 — TEL : 713-974-3287
Houston, TX 77042 — FAX : 713-974-3289

MEXICO

ADELSA HEADQUARTERS
Club Cuicacalli #66 — TEL : 525-374-0981
Cd Satelite, CP Naucalpan, — FAX : 525-374-0997
Edo, de Mexico 53100

ADELSA Reynosa OFFICE
Lago Xochimilco 250 Plant Alta — TEL : 525-8923-7887
Col. Valle Alto — FAX : 525-8923-7747
Reynosa, Tamps C.P 68710

ADELSA Guadalajara OFFICE
Otranto No. 3080-2, Providencia — TEL : 5236-420-865
Guadalajara, Jalisco MEX 44630 — FAX : 5236-419-465

ADELSA Cd.Juarez OFFICE
Jardin Misioneros 1720 — TEL : 5216-188-244
Fracc. Jardines del Seminario — FAX : 5216-188-244
Cd. Juarez, Chihuahua, MEX 32500

ADELSA MONTEREY OFFICE
Niza 2919-4 — TEL : 528-359-0029
Col. Primavera — FAX : 528-359-0029
Monterey, Nuevo Leon MEX 64830

SAMSUNG SEMICONDUCTOR INC. DISTRIBUTORS-U.S.A.

ALABAMA

ADVENT
4717 University DR., #107 TEL : 205-830-6669
Huntsville, AL 35816 FAX : 205-830-5585
ALL AMERICAN
4590 Corporate DR., #115D TEL : 205-837-1555
Huntsville, AL 35805 FAX : 205-837-7733
BELL-Milgray
8215 Highway 20 West TEL : 205-464-8646
Madison, AL 35758 FAX : 205-464-8655

ARIZONA

ALL AMERACAN
4696 E University DR., #155 TEL : 602-966-0006
Phoenix, AZ 85034 FAX : 602-966-0007
JACO
2432 W. Peoria AVE, Ste #1344 TEL : 602-906-4004
Phoenix, AZ 85029 FAX : 602-906-4054

CALIFORNIA

ALL AMERICAN
26010 Mureau RD., #120 TEL : 818-878-0555
Calabasas, CA 91302 FAX : 818-878-0533
ALL AMERICAN
10805 Holder ST., #100 TEL : 714-229-8600
Cypress, CA 90630 FAX : 714-229-8603
ALL AMERICAN
6390 Greenwich DR., #170 TEL : 619-658-0200
San Diego, CA 92122 FAX : 619-658-0201
ALL AMERICAN
230 Devcon DR., TEL : 408-441-1300
San Jose, CA 95112 FAX : 408-437-8970
ALL AMERICAN
14192 Chambers RD. TEL : 714-573-5000
Tustin, CA 92780 FAX : 714-573-5050
ALL AMERICAN
111. S. Court ST., #104 TEL : 209-734-8861
Visalia, CA 93291 FAX : 209-734-8865
BELL-Milgray
2201 E. El Segundo Blvd TEL : 310-563-2355
El Segundo, CA 90245 FAX : 310-563-2508
BELL-Milgray
220 Technology DR., STE. 100 TEL : 714-727-4500
Irvine, CA 92618 FAX : 714-453-4610
BELL-Milgray
125 Auburn Court, STE. 110 TEL : 805-373-5600
Westlake Village, CA 91362 FAX : 805-496-7340
BELL-Milgray
1161 North Fairoaks AVE, TEL : 408-734-8570
Sunnyvale, CA 94089 FAX : 408-734-8875
BELL-Milgray
3001 Douglas BLVD, STE. 205 TEL : 916-781-8070
Roseville, CA 95661 FAX : 916-781-2954
BELL-Milgray
6835 Flanders Dr. Ste #300 TEL : 619-457-7545
San Diego, CA 92121 FAX : 619-459-9750
IEC
9940 Business Park DR., Ste 145 TEL : 916-363-6030
Sacramento, CA 95827 FAX : 916-362-6926
JACO
1610-A Berryessa Road, TEL : 408-928-1600
San Jose, CA 95134 FAX : 408-928-1616
JACO
22815 Savi Ranch Parkway, Ste E TEL : 714-283-8185
Yorda Linda, CA 92680 FAX : 714-283-8191
JACO
2282 Townsgate Rd., TEL : 805-495-9998
Westlake Village, CA 91361 FAX : 805-494-3864

CANADA

ALL AMERICAN
6375 Dixie RD., Units 4,5 & 6 TEL : 905-670-5946
Mississauga, ON L5T2E7 FAX : 905-670-5947
MILGRAY
4185 Still Creek DR., #B201 TEL : 604-291-0044
Burnaby, B.C. CN V5C6G9 FAX : 604-291-9939
MILGRAY
6600 Trans Canada HWY. Suite #209 TEL : 514-426-5900
Pointe Claire, Quebec, CN H9R4S2 FAX : 514-426-5836
MILGRAY
2783 Thamesgate DR., TEL : 905-678-0958
Mississauga, Ontario, CN L4T1G5 FAX : 905-678-1213

COLORADO

ALL AMERICAN
4090 Youngfield ST., TEL : 303-422-1701
Wheatridge, CO 80033 FAX : 303-722-2529
BELL-Milgray
9351 Grant Street, STE. 460 TEL : 303-280-1115
Thornton, CO 80229 FAX : 303-280-0005
IEC
420 East 58th AVE TEL : 303-292-5537
Denver, CO 80216 FAX : 303-292-0114
IEC
5750 North Logan ST., TEL : 303-292-6121
Denver, CO 80216 FAX : 303-297-2053
JACO
695 Pierce Street TEL : 303-828-3074
Erie, CO 80516 FAX : 303-828-3080

CONNECTICUT

ALL AMERICAN
100 Mill Plain RD., #360 TEL : 203-791-3816
Danbury, CT 06811 FAX : 203-791-3801
BELL-Milgray
326 W. MAIN ST., TEL : 203-878-5538
Milford, CT 06460 FAX : 203-878-6970

FLORIDA

ADVENT
111 North Palm AVE., TEL : 407-952-8669
Indialantic, FL 32903 FAX : 407-984-2487
ADVENT
10500 NW 50th ST., #101 TEL : 954-748-9781
Sunrise, FL 33351 FAX : 954-748-9784
ALL AMERICAN
16115 N.W. 52nd AVE., TEL : 305-621-8282
Miami, FL 33014 FAX : 305-620-7831
ALL AMERICAN
14450 46th ST., #116 TEL : 813-832-9800
Clearwater, FL 34622 FAX : 813-592-5567
ALL AMERICAN
1400 E. Newport CTR. DR. #205 TEL : 954-429-2800
Deerfield Beach, FL 33442 FAX : 954-429-0391
BELL-Milgray
650 S. Northlake BLVD., #400 TEL : 407-339-0078
Altamonte Springs, FL 32701 FAX : 407-339-0139
JACO
9900 West Sample RD., Ste #404 TEL : 305-341-8280
Coral Springs, FL 33065 FAX : 305-341-7848

GEORGIA

ALL AMERICAN
6875 Jimmy Carter Blvd #3100 TEL : 770-441-7500
Norcross, GA 30071 FAX : 770-441-3660
BELL-Milgray
3000 Northwoods PKWY., Suite #115 TEL : 770-446-9777
Norcross, GA 30071 FAX : 770-446-1186

ILLINOIS

ADVENT
1865 Miner ST., TEL : 847-297-6200
Des Plaines, IL 60016-8416 FAX : 847-897-6650
ALL AMERICAN
1930 N. Thoreau Ste. #200 TEL : 847-303-1995
Schaumburg, IL 60173 FAX : 847-303-1996
BELL-Milgray
175 W. Central RD., TEL : 847-202-6400
Schaumburg, IL 60195 FAX : 847-202-5850
IEC
2401 W.Hassell RD., Suite #1505 TEL : 847-843-2040
Hoffman Estates, IL 60915 FAX : 847-843-2320
JACO
101 E. Commerce DR., TEL : 847-884-6620
Schaumburg, IL 60172 FAX : 847-884-7273

INDIANA

ADVENT
8446 Moller RD., TEL : 317-812-4910
Indianapolis, IN 46268 FAX : 317-872-9987
BELL-Milgray
6982 Hillsdale Ct TEL : 317-842-4244
Indianapolis, IN 46250 FAX : 317-570-1344

IOWA

ADVENT
682 58TH AVE. CT. SW TEL : 319-363-0221
Cedar Rapids, IA 52404 FAX : 319-363-4514

KANSAS

ADVENT
9521 Mission RD., TEL : 913-381-9003
Overland, KS 66206 FAX : 913-381-0866
MILGRAY
6400 Glenwood, TEL : 913-236-8800
Overland Park, KS 66202 FAX : 913-384-6825

MASSACHUSETTS

ALL AMERICAN
19C Crosby DR., TEL : 617-275-8888
Bedford, MA 01730 FAX : 617-275-1982
BELL-Milgray
100 Burtt RD., #G01 TEL : 502-623-3200
Andover, MA 01810 FAX : 508-474-8902
BELL-Milgray
187 Ballardvale ST. TEL : 508-657-5900
Wilmington, MA 01887-1046 FAX : 508-658-7989
JACO
1053 East ST., TEL : 508-640-0010
Tewksbury, MA 01876 FAX : 508-640-0755

MARYLAND

ALL AMERICAN
14636 Rothgeb DR., TEL : 301-251-1205
Rockville, MD 20850 FAX : 301-251-8574
BELL-Milgray
6460 Dobbin RD., TEL : 410-730-6119
Columbia, MD 21045-5813 FAX : 410-730-8940
JACO
10260 Old Columbia RD., TEL : 410-995-6620
Columbia, MD 21046 FAX : 410-995-6032

MICHIGAN

ADVENT
24713 Crestview CT., TEL : 810-477-1650
Farmington Hills, MI 48335 FAX : 313-477-2630
ALL AMERICAN
39201 Schoolcraft RD., #B20 TEL : 313-464-2202
Livonia, Mi 48150 FAX : 313-464-2433

MINESOTA

ALL AMERICAN
7716 Golden Triangle DR., TEL : 612-944-2151
Eden Prarie, MN 55344 FAX : 612-944-9803
BELL-Milgray
9401 James Avenue south, #142 TEL : 612-888-7747
Bloomington, MN 55431 FAX : 612-888-7757
JACO
10340 Viking DR., Suite #115 TEL : 612-941-2757
Eden Prarie, MN 55344 FAX : 612-941-1989

MISSOURI

ADVENT
1029 East Terra Lane TEL : 314-272-4281
O'Fallon, MO 63366 FAX : 314-272-2950

NEW JERSEY

ADVENT
600 Penn ST., TEL : 609-964-8560
Camden, NJ 08102 FAX : 609-964-0423
ALL AMERICAN
8. E. Stow RD., #100 TEL : 609-596-6666
Marlton, NJ 08053 FAX : 609-797-1700
BELL-Milgray
271 Route 46 West, Suites #F202 TEL : 201-227-6060
Fairfield, NJ 07004 FAX : 201-227-2626
BELL INDUSTRIES
158 Gaither DR., STE. #110 TEL : 609-439-8860
MT. Laurel, NJ 08054 FAX : 609-439-9009

NEW YORK

ALL AMERICAN
275B Marcus BLVD. TEL : 516-434-9000
Hauppauge, NY 11722 FAX : 516-734-9394
ALL AMERICAN
333 Metro Park TEL : 716-292-6700
Rochester, NY 14623 FAX : 716-292-6755
JACO
145 Oser AVE. TEL : 516-273-5500
Hauppauge, NY 11788 FAX : 516-273-5799
BELL-Milgray
77 Schmitt BLVD., TEL : 516-420-9800
Farmingdale, NY 11735 FAX : 516-752-9870
BELL-Milgray
1170 Pittsford Victor RD., TEL : 716-381-9700
Pittsford, NY 14534 FAX : 716-381-9495

NORTH CAROLINA

BELL-Milgray
3100 Smoketree Ct, STE. 800 TEL : 919-874-0011
Raleigh, NC 27604 FAX : 919-874-0013
JACO
5206 Greens Dairy RD., TEL : 919-876-7767
Raleigh, NC 27604 FAX : 919-876-6964

OHIO

ALL AMERICAN
26650 Renaissance PKWY. TEL : 216-514-0625
Warrenville Heights, OH 44128 FAX : 216-514-0822
BELL-Milgray
444 Windsor Park DR., TEL : 937-435-5922
Dayton, OH 45459 FAX : 937-435-3122
BELL-Milgray
6155 Rockside RD., TEL : 216-447-1520
Cleveland, OH 44131 FAX : 216-447-1761

OREGON

ALL AMERICAN
1815 NW 169th PL., Suite #6025 TEL : 503-531-3333
Beaverton, OR 97006 FAX : 503-531-3695
BELL INDUSTRIES
8705 SW Nimbus AVE., STE. #100 TEL : 503-644-3444
Beaverton, OR 97008 FAX : 503-520-1948
IEC
3720 S.W. 141st ST., 102 TEL : 503-641-1690
Beaverton, OR 97005 FAX : 503-646-3737
JACO
4900 SW Griffith Dr. Ste #129 TEL : 503-641-1439
Beaverton, OR 97005 FAX : 503-626-0979

TEXAS

ALL AMERICAN
13706 Research BLVD., STE. #103 TEL : 512-335-2280
Austin, TX 78750 FAX : 512-335-2282
ALL AMERICAN
11210 Steeplecrest, #206 TEL : 713-955-1993
Houston, TX 77065 FAX : 713-955-2215
ALL AMERICAN
1711 International Pkwy, #101 TEL : 214-231-5300
Richardson, TX 75081 FAX : 214-437-0353
BELL-Milgray
14110 Dallas Parkway, Suite #170 TEL : 972-458-0047
Dallas, TX 75240 FAX : 972-404-0267
JACO
2120 A-Braker Lane TEL : 512-835-0220
Austin, TX 78758 FAX : 512-339-9252

JACO
1209 N Glenville DR., TEL : 214-234-5565
Richardson, TX 75081 FAX : 214-238-7068
BELL-Milgray
11824 Jollyville RD., Ste 103 TEL : 512-331-9961
Austin, TX 78759 FAX : 512-331-1070
BELL-Milgray
12000 Richmond AVE., STE #310 TEL : 281-870-8101
Houston, TX 77082 FAX : 281-870-8122

UTAH

ALL AMERICAN
6955 Union Park Center, #101 TEL : 801-565-8300
Midvale, UT 84047 FAX : 801-565-9983
IEC
2117 South 3600 West TEL : 801-977-9750
West Valley City, UT 84119 FAX : 801-975-1207
BELL-Milgray
310 E. 4500 S, STE. #110 TEL : 801-261-2999
Murray, UT 84107 FAX : 801-261-0880

WASHINGTON

ALL AMERICAN
11807 Nothcreek PKWY. S.#112 TEL : 206-806-4800
Bothel, WA 98011 FAX : 206-806-9900
BELL-Milgray
19119 N. Creek PKWY., STE.#102 TEL : 425-486-7124
Bothell, WA 98011 FAX : 425-487-1927

IEC
1750 124th AVE, N.E. TEL : 206-455-2727
Bellevue, WA 98005 FAX : 206-453-2963
JACO
17220 127th Place NE, Ste #300 TEL : 206-481-3372
Woodinville, WA 98072 FAX : 206-481-1664

WISCONSIN

ADVENT
237 South Curtis RD., TEL : 414-475-6860
Swest Allis, WI 53214 FAX : 414-475-0440
ALL AMERICAN
18000 Sarah Lane, Suite #145 TEL : 414-792-0436
Brookfield, WI 53045 FAX : 414-792-9733
BELL INDUSTRIES
W. 226 N.900 Eastmond DR., TEL : 414-547-8879
Waukesha, WI 53186 FAX : 414-547-6547

• • • • •

SAMSUNG SEMICONDUCTOR SALES OFFICE-EUROPE

Central Europe

Samsung Semiconductor Europe Gmbh
Am Kronberger Hang 6 TEL : 0049-6196-663-300
D-65824 Schwalbach FAX : 0049-6196-663-311

MUNICH

Samsung Semiconductor Eurpoe Gmbh
Carl-Zeiss-Ring 9 TEL : 0049-89-964838
D-85737 Ismaning FAX : 0049-89-964873

UK-Hinckley Birmingham

Samsung Semiconductor Europe Gmbh
Florence House St.Marys Road TEL : 0044-1455-891111
Hinckley LEICS LE10 1EQ FAX : 0044-1455-612345

UK-Brentford

Samsung Semiconductor Europe LTD
2nd Fl., Great West House, TEL : 0044-181-380-7200
Great West Road, FAX : 0044-181-380-7220
GB-Brentford, Middlesex TW8 9DQ

Scotland Glasgow

Samusng Semiconductor Europe Gmbh
Representative Office
Trojan House, Phoenix Business Park, TEL : 00441-41-840-2424
Paisley PA1 2BH, Scotland FAX : 00441-41-840-4747

Ireland Dublin

Samusng Semiconductor Europe Gmbh
Representative Office
Block 8, St. John's Court, TEL : 0035-3186-21688
Swords Road, Santry, Dublin 9, Ireland FAX : 0035-3186-21684

France Paris

Samsung Semiconductor France S.A.R.L
Centre d'affaires la, TEL : 0033-1-46017181
Boursidiere RN 186, BAT. FAX : 0033-1-40940216
Bourgogne, BP202, F-92357 Le,
Plessis-Robinson

Italy Milano

Samsung Semiconductor Italia S.A.R.L
Procaccini Center, Via Messina, 38 TEL : 0039-2-34578-231
I-20154 Milano FAX : 0039-2-33604027

Nordic Stockhoim

Samusng Semiconductor Europe Gmbh
Representative Office
Johanneslundsvägen4 TEL : 0046-8-59410841
S-194 81 Upplands Väsby FAX : 0046-8-59410849

Spain, Hospitalet

Samusng Semiconductor Europe Gmbh
Representative Office
Edificio samsung Electronica 1st Fl., TEL : 0034-3-2616700
Ciencies, 55- 65, Pol. Pedrosa, FAX : 0034-3-2616790
08908 Hospitalet de Llobregat

Turkey, Istanbul

Samusng Semiconductor Europe Gmbh
Representative Office
Bahariye Caddesi, Dr.Dilemre Is TEL : 0090-216-348-8557
MerkeziNo 80/7 81300 Kadiköy, FAX : 0090-216-348-3964
Istanbul, Turkey

SAMSUNG SEMICONDUCTOR DISTRIBUTORS-EUROPE

Austria

SEI-Elbatex Ges
Eitnergasse 6, TEL : 1866420
A-1230, Wien FAX : 186642201

Belgium

AVER S.A.
Zoning Gosset, Avenue Gossetlaan 15, TEL : 2-4633414
B-1702, Groot-Bijgaarden FAX : 2-4632219
Malchus Belgium
Generaal de Wittelaan 9/14 TEL : 15-287898
B-2800, Mechelen FAX : 15-287890

Denmark

Arrow-Exatec
Mileparken 20E TEL : 449-27000
DK-2740 Skovlunde FAX : 449-26020
Future Electronics
Holstebro TEL : 961-00961
FAX : 961-00962

East Europe

Eltron Electronic
Ul. Szewska 3, PL-50-053 TEL : 71-442532
Wroclaw FAX : 71-441141
Future Electronics
Warszawa TEL : 226189202
FAX : 226188050

GM
Karlinske Nam.6 TEL : 2-2322606
CZ-18600 Prag 8 FAX : 2-2321194

Finland

Computer 2000 Finland
P.O.Box 44 (Pyyntitie 3) TEL : 3589-8873330
FIN-02231, Espoo FAX : 3589-88733289
Future Electronics
Espoo TEL : 3589-5259950
FAX : 3589-4551050

FRANCE

Arrow-Computer Products
7, Avenue du Canada, TEL : 1-60926060
Z.A.de Courtaboeuf FAX : 1-60926020
F-91966, Les Ulis Cedex
Arrow-CCI Electronique
12, Allée de la Vierge; Silic 577 TEL : 1-41807000
F-94653, Rungis Cedex FAX : 1-46753207

Future Electronics
3 Avenue du Canada-Bat. TEL : 1-69821111
Theta 2; L.P. 854 Les Ulis FAX : 1-69821100
F-91974, Courtabeuf Cedex
SEI-Scaib
6, Rue Ambroise Croizat TEL : 1-69198900
Z.A.E. Les Glaises FAX : 1-69198920
F-91127 Palaiseau Cedex

Germany

Arrow-Spoerle Electronic
Max-Planck-Str. 1-3 TEL : 6103-3040
D-63303, Dreieich FAX : 6103-304201
Distec
Industriestr. 1, TEL : 89-8943630
D-82110, Gemering FAX : 89-89436339
Future Electronics
Münchner Str. 18 TEL : 89-957270
D-85774, Unterföhring FAX : 89-95727173
Micronetics
Dieselstr. 12 TEL : 7259-925830
D-71272, Renningen FAX : 7159-9258355
MSC HQ
Industriestr. 16 TEL : 7249-9100
D-76297, Stutensee FAX : 7249-4232
SEI-Jermyn
Kapellenstr. 15 TEL : 6431-508-220
D-65555, Limburg FAX : 6431-54662
Distron
Ammerthalstraße 28 TEL : 89-991140
D-85551, Kichheim-Helmstetten FAX : 89-99114414

ISRAEL

Data JCE
3, Hashikma Str. TEL : 3-5583318
IR-58001, Azor FAX : 3-5583325

ITALY

Future Electronics
Via Fosse Ardeatine, 4 TEL : 2-660941
I-20092, Cinisello Balsamo Milano FAX : 2-66012843
Kerr Technology Bridge
Piazza Toscana 1 TEL : 2-90782053
I-20090, Peive Emanuele Milano FAX : 2-90781663
Rafl Electronica
Via Savona 134 TEL : 2-4779181
I-20144, Milano FAX : 2-428880
SEI-Sonelco
Via Monfalcone, 15 TEL : 2-66011349
I-20092 Cinisello Balsamo Milano FAX : 2-66011295

7

Netherlands

Future Electronics
Breda — TEL : 765444888, FAX : 765444880

Malchus
Fokkerstraat 511-513, NL-3125, BD schiedam — TEL : 102452452, FAX : 104154466

SEI-Sonetech Netherland
Takkebijsters 2, NL-4817, BL Breda — TEL : 765722333, FAX : 765722395

SPaSE
Kerkenbos 1021, NL-6546 BB Nijmegen — TEL : 24-378-2882, FAX : 24-378-8388

Norway

Future Electronics
Oslo — TEL : 22-905800, FAX : 22-905790

SEI-Jakob Hatteland
Postbox 25, N-5578 Nedre Vats — TEL : 53-763000, FAX : 53-765339

Spain

Iberica de Componentes
Avda, Somosierra, 11; 1 Of A., E-28709, San Sebastian de Los Reyes — TEL : 1-7373671, FAX : 1-7375464

SEI-Selco
Ctra de la Coruna N-VI, KM 18200 Via de Servicio, E-28230, Las Rozas de Madrid — TEL : 1-6371011, FAX : 1-6371506

Sidsa
Isaac. Newton, 1, E-28760 Tres Cantos, Madrid — TEL : 1-8035052, FAX : 1-8039557

Sweden

Arrow-Microtronica Sweden
Ellipsvägen 5, S-14175, Huddinge — TEL : 8-6807800, FAX : 8-74044515

Future Electronics
Solna — TEL : 8-279479, FAX : 8-822833

Ingram Micro
Kronborgsgränd 1, S-16487, Kista — TEL : 8-7525400, FAX : 8-7039348

Miko Komponent
Segersbyvaegen 3, S-14502 Norsborg — TEL : 853-1-93900, FAX : 853-1-93939

Swiss

Primelco
Blegistrasse 23, CH-6342, Baar — TEL : 41-7670170, FAX : 41-7670179

SEI-Elbatex
Hardstr. 72, CH-5430, Wettingen — TEL : 564375111, FAX : 564375454

UK

Arrow-Jermyn
Cambride Road, UK-MK42 0LE, Bedford — TEL : 1-234270027, FAX : 1-234791786

Assured Technologies
581 London Road, UK-TW7 4EJ, Middlesex; Isleworth — TEL : 181-7580758, FAX : 181-7580708

Future Electronics HQ
Future House, Poyle Road, Colnbrook, UK-SL3 0EZ, Berkshire — TEL : 1-753-763000, FAX : 1-753-689100

Just Rams
Unit 6, Iron Bridge Business Park, GT Cent Way, UK-NW10 0UW,London — TEL : 1-814517766, FAX : 1-814596301

Magnatec/Semelab
Coventry Road, Lutterworth, UK-LE17 4JB, Leicestershire — TEL : 1-455-554711, FAX : 1-455-558843

MSC
Pavillion House, 6/7 Old Steine Sussex, UK-BN1 1EJ, Brighton — TEL : 1273-622446, FAX : 1273-622533

Oxford Semiconductors
68, Milton Park, UK-OX14 4RX, Abingdon Oxfordshire — TEL : 1-235861461, FAX : 1-235821141

SEI-2001
Stevenage Business Park, Pin Green-Stevenage, UK-SG1 4SU, Herts — TEL : 1-438742001, FAX : 1-438742002

Dondene/Transonics
Woodside Place, Mount Pleasant, UK-HA0 1UW, Wembley/Middlesex — TEL : 1-819001334, FAX : 1-819002040

• • • • •

SAMSUNG SEMICONDUCTOR REPRESENTATIVES-ASIA

HONG KONG

AV. CONCEPT LTD.
Unit 11-15, 11fl., Block A, TEL : 2334-7333
Focal Industrial Centre FAX : 2764-3108
21 Man Lok Street, Hunghom,
Kowloon, Hong Kong

PROTECH COMPONENTS LTD.
Unit 2, 3fl., Wah Shing Centre, TEL : 2950-2888
11 Shing Yip Street, FAX : 2950-2828
Kwun Tong, Kowloon,Hong Kong

WISEWORLD ELECTRONICS LTD.
Room 708, Tower A, 7fl., TEL : 2765-8923
Hunghom Commercial Centre, FAX : 2363-6203
31-39 Ma Tau Wai Road, Honghom,
Hong Kong

CENTENNIAL ELECTRONICS LTD.
Unit 2, 23fl., Westlands Center, TEL : 2565-5898
No.20 Westlands Road., FAX : 2564-5411
Quarry Bay, Hong Kong

SOLARBRITE ELECTRONICS LTD. (CALCULATOR & WATCH)
Unit 1, 11fl., Tower 1, TEL : 2363-3233
Horbour Centre 1, Hok Cheung St., FAX : 2363-3900
Hunghom, Kowloon,Hong Kong

ATLANTIC COMPONENTS LTD. (MEMORY & PC)
Unit 502, 5fl., Tower 3, TEL : 2799-1996
Enterprise Square,9 Sheung Yuet Rd, FAX : 2755-9452
Kowloon Bay,Kowloon, Hong Kong

SAMTEK SEMICON DEVICES H.K LTD.
Room 2104, Windsor House 311 TEL : 2890-7933
Gloucester Road., Causeway Bay, FAX : 2890-7890
Hong Kong

Li SENG TECHNOLOGY LTD.
Flat B&C. 6fl., TEL : 2540-8348
Four Seas Comm. Bank Bldg FAX : 2547-5706
49-51 Bonham Strand West,
Hong Kong

LEGEND-VALENCE SEMICONDUCTOR DESIGN LTD.
Units 1-7, 19F, Apec Plaza TEL : 2656-1151
49 Hoi Yuen Road, Kwun Tong, FAX : 2652-2301
Kowloon, Hong Kong

MACRO LONG DELEVELOPMENT LTD.
Room 1008, 1 Hung To Road., TEL : 23575780
Kwan Long, Kowloon, Hong Kong FAX : 27935697

TAIWAN

YOSUN INDUSTRIAL CORP.
7FL., No76 SEC 1, Cheng Kung Rd., TEL : 02-788-1991
Nan Kang, Taipei, R.O.C FAX : 02-788-1996

SANT SONG CORP.
4FL., No.12, Lane 94, Tsao TEL : 02-662-7829
Ti Wei, Shen Keng Hsiang FAX : 02-662-0781
Taipei, Hsien, Taiwan, R.O.C.

SUPREME ELECTRONICS CO., LTD.
18FL.,NO.67 Section 2, TEL : 02-7023258/7023278
Tun Hwa S. Road, FAX : 02-7063196
Taipei, Taiwan, R.O.C.

JAPAN

TOMEN DEVICES CORP.
10-15, Horidome-Cho, 1 Chome, TEL : 03-5640-1386
Nihonbashi Chuo-Ku, FAX : 03-5640-8583
Tokyo103 Japan

RIKEI SEMICONDUCTOR CORP.
Meiji Seimei Bldg., TEL : 03-3490-2173
2-27-4, Nishi-Gotanda, FAX : 03-3490-2179
Shinagawa-Ku Tokyo 141 Japan,

ISECO
2-26-3, Kitamagome 2-Chome, TEL : 03-3777-3611
Ota-Ku, Tokyo, 143 Japan FAX : 03-3777-3614

SINGAPORE

SAMSUNG ASIA PTE LTD. MALAYSIA LIAISON OFFICE
9-2 Menara Penang Garden, TEL : 604-2291671
42-A, Jalan Sultan Ahmad Shah FAX : 604-2291678
10500 Penang, Malaysia

SAMSUNG ASIA PTE LTD. BANGALORE LIAISON OFFICE
10FL., Prestige Meridian Building TEL : 9180-555-0555
No.29 M,G,Road, FAX : 9180-555-0558
Bangalore-560 001, India

SAMSUNG ASIA PTE LTD. NEW DELHI LIAISON OFFICE
11FL., DR Gopal Das Bhawan TEL : 9111-3720340~2
28 Barakhamba Road, FAX : 9111-3755390
New Delhi-110001, India

SINGAPORE

Astina Electronics(S) PTE LTD.
203B Henderson Road, TEL : 276-9997
#12-08, Henderson Industrial Park, FAX : 276-9996
Singapore 159548

Bostex Electronics PTE LTD.
219 Henderson Road, TEL : 339-0713
#10-01, Henderson Industrial Park FAX : 338-9536
Singapore 159556

YIC Singapore PTE LTD.
159 Sin Ming Road, TEL : 552-4811
#04-04, Amtech Building FAX : 552-5811
Singapore 575625

Samtek Semicon Devices(S) PTE LTD.
80, Robinson Road, TEL : 225-9177
#16-01, Singapore 068898 FAX : 225-9477

Samtek Semicon Devices New Delhi Liaison Office
Hotel Samrat, #582,Chanakyapuri, TEL : 687-1723
New Delhi-110021, India FAX : 687-1725

South West Electronics PTE LTD.
159 Sin Ming Road, TEL : 553-3118
#04-03, Amtech Building FAX : 553-3008
Singapore 575625

Tomen Devices Corporation Singapore Branch
10 Shenton Way, TEL : 221-1422
#16-02, MAS building FAX : 221-0400
Singapore 079117

Rikei Corporation(S) PTE LTD.
15 Scotts Road, TEL : 235-2427
#03-11, Thong Tech Building FAX : 235-2463
Singapore 228218

Vutipong Technology Co., LTD.
47-49 Pahurat Road, TEL : 662-2266496
Bangkok, Thailand 10200 FAX : 662-2240861

CHINA

Centennial Electronics LTD. (Shanghai Office)
Room 808, Area B, TEL : 021-64810697
Yin Hai Comm. Bldg, FAX : 021-64824668
250 Cao Xi Road, Xu Hui District,
Shanghai, P.R.C

Centennial Electronics LTD. (Shenzhen Office)
Unit 10, 22Fl., Oriental Bldg., TEL : 0755-2284262
39 Jianshe Road., Shenzhen, FAX : 0755-2282536
Guangdong, China

Qinghua-Samsung MICOM Software House (Dept of Electronics)
Qinghua Yuan, TEL : 01-2594785
Beijing, China FAX : 01-2594176

Suman Electronics Products Co.
Room 117, Technology Trading Center TEL : 01-6846-7032~4
No.37 Bai Qiao Road,Beijing, China FAX : 01-6846-7035

Suman Electronics (Tianjin Office)
No.203-205, HongQi Road, TEL : 022-451-6680/1
Nankai District, Tianjin, China FAX : 022-451-6680

Suman Electronics (Hangzhou Office)
No.27, Wen-San Road, TEL : 0571-803607/5
Hangzhou City, China FAX : 0571-806-6087

Suman Electronics (Nanjing Office)
No.8 Shitiao Xiang, Gulou, TEL : 025-3364473/4578
Nanjing, China FAX : 025-336-4658

Suman Electronics (Xian Office)
No.106 Frengging Road, TEL : 029-4262014
Xian, China FAX : 029-4262306

AUSTRALIA

SAMSUNG CO., LTD.
Level 20, Northpoint Bldg., TEL : 61-2-9955-3888
100 Miller Street, North Sydney, FAX : 61-2-9955-4233
NSW 2060 Australia

KOREA

Samtek Corp.
4Fl., ChungLim Bldg., TEL : 02-3458-9000
154-16, Samsung-Dong, FAX : 02-3458-9300
Kangnam-Ku, Seoul, Korea

Samsung Kwangjun Co., LTD.
11FL., Chungjin Bldg., TEL : 02-3271-7871
53-5, 3-Ka, Wonhyo-Ro, FAX : 02-3271-7898~9
Yongsan-Ku, Seoul, Korea

Shinsung Semiconductors Co., LTD.
2FL., 17-10 Yeouido-Dong, TEL : 02-3775-0101
Youngdeungpo-Ku, Seoul, Korea FAX : 02-3775-0222~3

Mirai Semiconductor Co., LTD.
4403 Joongang circulation complex TEL : 02-615-8877
Na-Dong, 1258 Kurobon-Dong, FAX : 02-613-5511
Kuro-Ku, Seoul, Korea

Mujin Electronics Co., LTD.
Sambo Bldg.,13-2, Yeouido-Dong, TEL : 02-783-4890
Youngdeungpo-Ku, Seoul, Korea FAX : 02-785-7661

Hankook Semiconductor & Telecommunications Co., LTD.
3FL., Sungwon Bldg., TEL : 02-539-4123
119-3, Samsung-Dong, Kangnam-Ku, FAX : 02-508-8558
Seoul, Korea

Samsung Memory Service Center
#413, Tourist Terminal Bldg., TEL : 02-701-0300
40-969, Hankangro 3-Ka, FAX : 02-702-5330
Yongsan-Ku, Seoul, Korea

SAMSUNG Semiconductor

DRAM

EDO & Fast Page Mode Module

Head Office

SEMICONDUCTOR BUSINESS SALES & MARKETING DIVISION
18th Fl., Joong-ang Ilbo Bldg.,
7, Soonhwa-Dong,
Chung-Ku, Seoul, Korea
TEL : 82-2-750-7536
FAX : 82-2-750-7502

America

SAMSUNG SEMICONDUCTOR INC.
3655 North First Street,
San Jose, CA 95134, U.S.A.
TEL : 1-408-544-4000
FAX : 1-408-544-4980

Europe

SAMSUNG SEMICONDUCTOR EUROPE GMBH
Samsung House,
Am Kronberger Hang 6,
65824, Schwalbach/Ts
TEL : 49-6196-663300
FAX : 49-6196-663311

SAMSUNG SEMICONDUCTOR EUROPE LTD.
Great West House,
Great West Road, Brentford
Middlesex TW8 9DQ, UK
TEL : 181-380-7132
FAX : 181-380-7220

Japan

SAMSUNG ELECTRONICS JAPAN CO.,LTD.
Hamacho Center Bldg.,
31-1, Nihonbashi-Hamacho, 2-Chom,
Chuo-Ku, Tokyo 103, Japan
TEL : 3-5641-9850
FAX : 3-5641-9851

SAMSUNG JAPAN CORPORATION
Osaka Office
6Fl., Crystal Tower, 1-2-27 Shiromi,
Chuo-Ku, Osaka 540-6006, Japan
TEL : 6-949-4811
FAX : 6-949-3036

Asia

SAMSUNG ELECTRONICS TAIWAN CO.,LTD
30th Fl., No.333 Keelung RD.,
Sec 1, Taipei, Taiwan, R.O.C.
TEL : 886-2-758-8320
FAX : 886-2-757-7311

SAMSUNG ASIA PRIVATE LIMITED
83 Clemenceau Avenue, #08-01,
UE Square, Singapore 239920
TEL : 65-535-2808
FAX : 65-227-2792

SAMSUNG ELECTRONICS HONG KONG CO.,LTD.
31th Fl., The Center,
99 Queen's Road Central,
Central, Hongkong
TEL : 852-2862-6900
FAX : 852-2866-1343

SAMSUNG ELECTRONICS CO.,LTD.
Shanghai Office
9th Fl., Shanghai International
Trade Centre, No.2200 Yanan(w) RD.
Shanghai, P.R.C 200335
TEL : 8621-6270-4168
FAX : 8621-6275-2975

SAMSUNG ELECTRONICS CO.,LTD.
SEMICONDUCTOR BUSINESS
Beijing Office
15Fl., Bright China Chang An Bldg.,
No.7, Jian Guo Men Nei Avenue,
Beijing, China 100005
TEL : 8610-6510-1234(0)
FAX : 8610-6510-1536

SAMSUNG ELECTRONICS CO.,LTD.
Shenzhen Office
Room 3113-15 Office Tower
Shun Hing Square
Diwang Commercial Centre, 333
Shennam Dong RD., Shenzhen, P.R.C.
TEL : 86-755-2461767
FAX : 86-755-2461715

SAMSUNG ELECTRONICS CO.,LTD.
Manila Office
2th Fl., 1535M. Adriatico Street
Malate, Metro Manila. Philippines
TEL : 63-2-526-2412~19
FAX : 63-2-528-4830

BSI REGISTERED FIRM — NATIONAL ACCREDITATION OF CERTIFICATION BODIES

http://www.samsungsemi.com

Challenge the Limits.

SAMSUNG